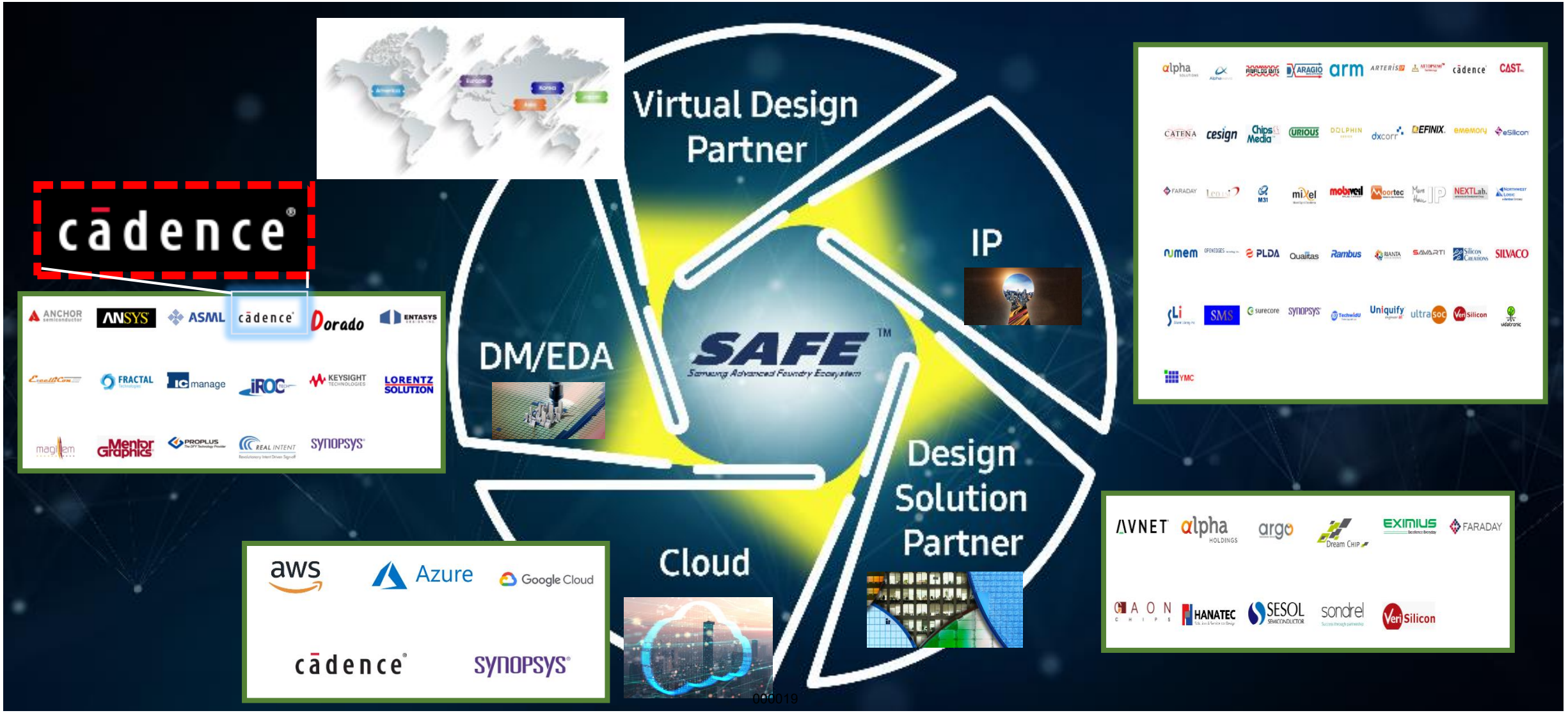
Samsung Foundry's 3D Package Solution based on Cadence Design Flow

Max Min (US)
Sungwook Moon (Korea)
Samsung Foundry

SAMSUNG

Contents

SAFE™ - Samsung Advanced Foundry Ecosystem



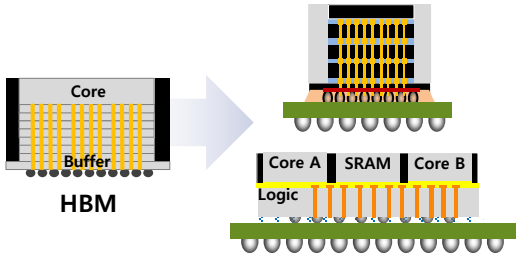
FO & 2.5D Design Flow (@Design Cadence Booth, Jan 2019)

Thursday, January 31 2:50pm – 3:30pm Great America 3	Advanced Package Design Sign-off Reference Flow View Presentation	Sungwook Moon Ph.D. and Max Min Ph.D., Samsung Foundry

Contents

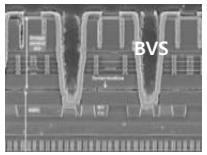
3D Integration Roadmap in Samsung Foundry

3D CoW

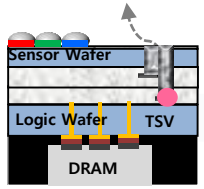


3D WoW

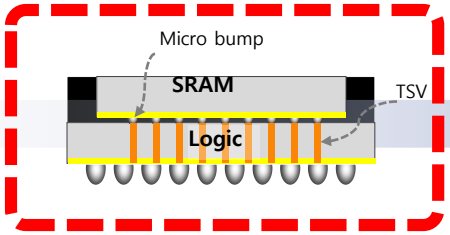
+ Oxide/Hybrid Bonding



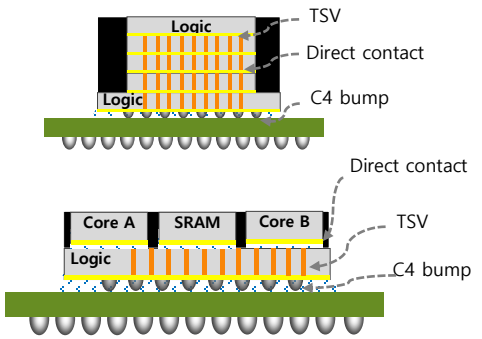
Dielectric Bonding
(WoW)



CIS 3stack `17, MP
(Sensor + Logic + DRAM)

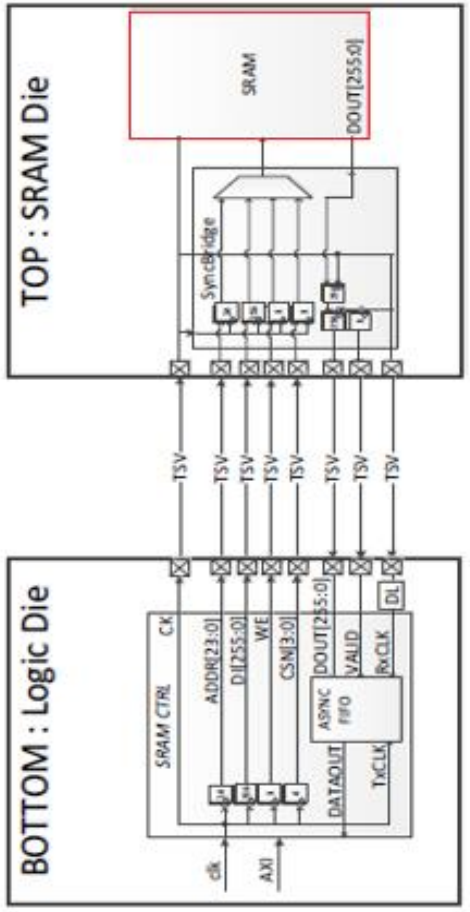


3D D2W

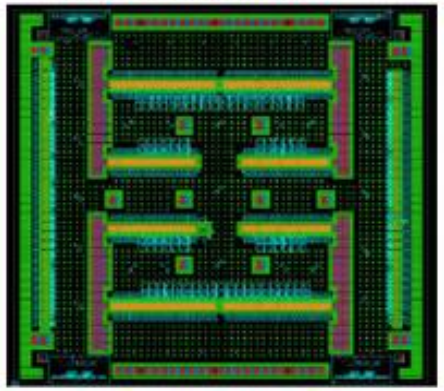


CoW : Chip on Wafer
WoW : Wafer on Wafer
D2W : Die to Wafer

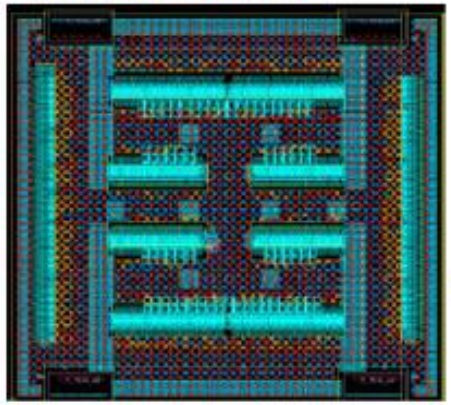
3DIC Vehicle: SAINT-S (Samsung Advanced Interconnection Technology SRAM)



TOP : SRAM Die



BOTTOM : Logic Die



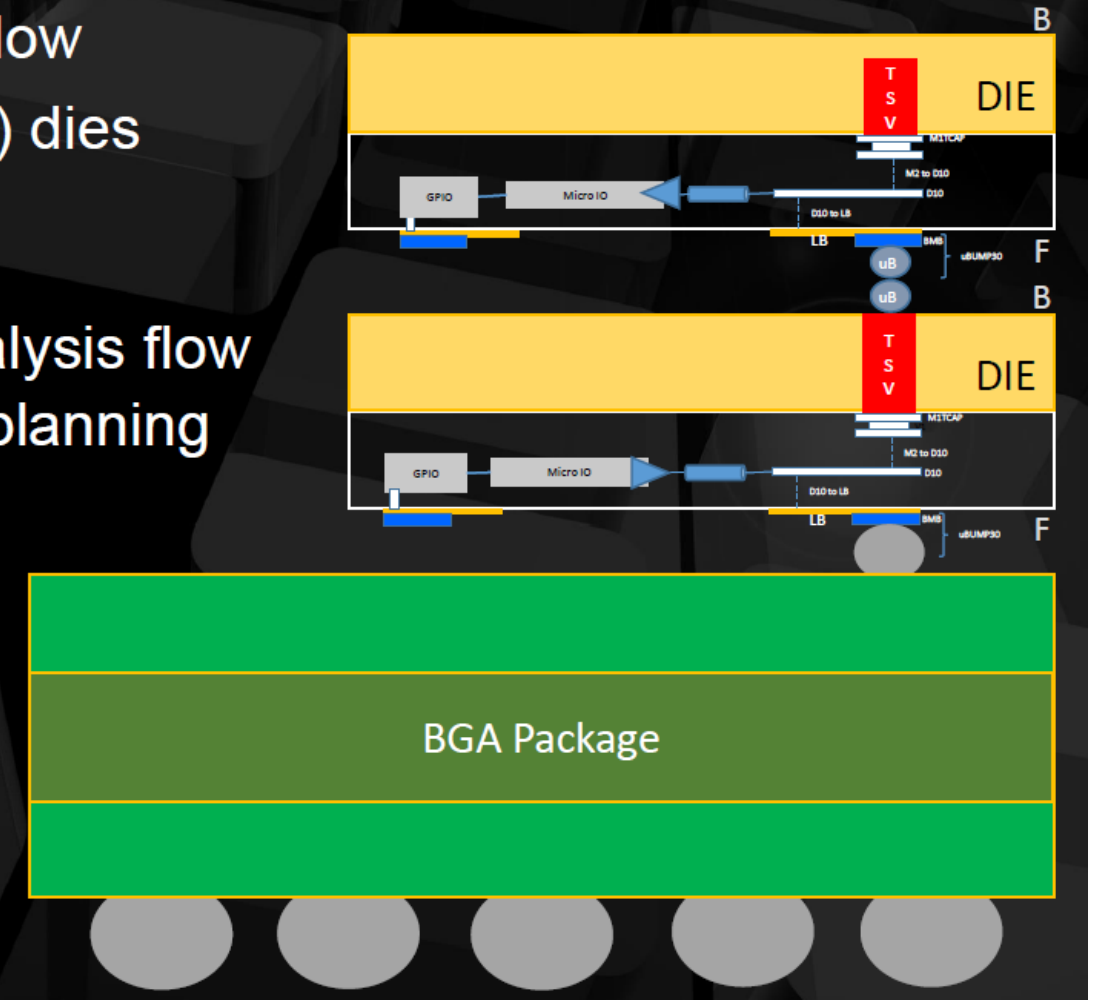
Node	7LPP
Total Density	64Mb (1stack)
Target BW	38.4GB/s
Target Latency	6 cycles (R) /2 cycles (W)
Die Size	9mm x 9mm (Top) 9.5mm x 9.5mm (Bottom)

PKG	MPGA (Micro Post Grid Array)		Stack-up Analysis SAINT-S
SRAM	# of stacks (target)		1 (~3)
	TSV	Pitch(㎛)	50
		Diameter(㎛)	4
Logic	TSV	Pitch(㎛)	50
		Diameter(㎛)	4
	Cu-pillar pitch (㎛)		125

Contents

3DIC MDI™ Reference Flow Coverage

- Samsung Foundry MDI™ 3DIC Reference Flow
- Face-to-back 3D stacking of two 7LPP (EUV) dies
  - Advanced BGA packaging
- PSI-aware multi-die package design and analysis flow
  - Cadence® OrbitIO™ for top-level design planning
  - Cadence® Innovus™ for die layout
  - Cadence® SiP Layout® for BGA package layout
  - Sigrity™/Clarity™ for electrical analysis
    - Model extraction by Clarity
    - Eye Diagram analysis with Spectre™
  - Voltus™ for multi-die IR drop analysis



Samsung Foundry MDI™(Multi-Die Integration) Design Flow

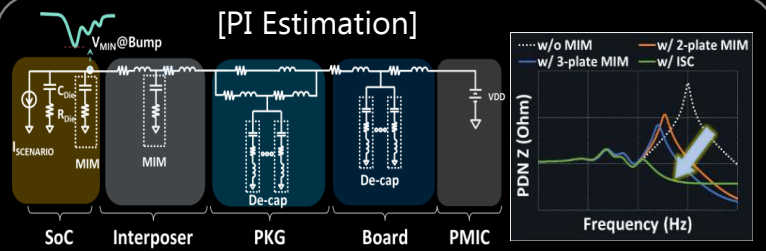
MDI design platform includes all design infra to enable HPC/AI products

System-level PSI Analysis & Design

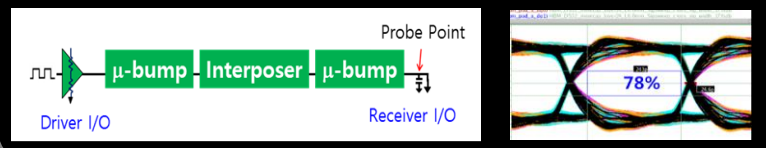
- Early-Stage System-level PSI Feasibility Analysis

Design Stage	On-chip Current Profile	Power Supply Model	Chip/PKG/B'rd Decap Model	PI Estimation Accuracy
SVP		Ideal		<+/-30%
DR1		Behavior	Parasitic Model	<+/-10%
DR2		Behavior	GDS	Reference

[PI Estimation]



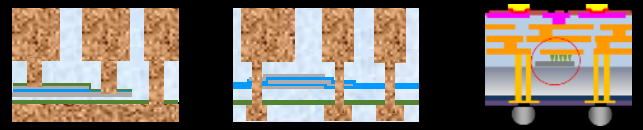
[SI Estimation]



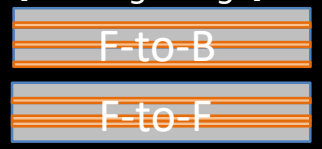
PSI-Aware Design Flow

- PI: Ultra-High Density Capacitor (MIM, ISC)
- Thermal: Temp. Distribution in Geometry
- Reliability: EM-Aware Design Flow
- PKG: Stacking Order, Bonding Method

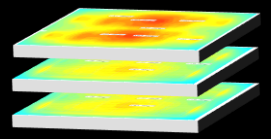
[2-plateMIM] [3-plateMIM] [ISC]



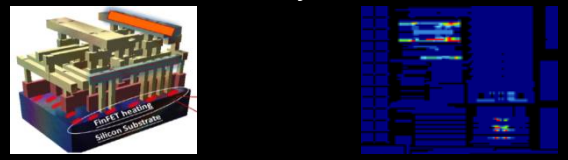
[Stacking Design]



[Thermal Analysis]



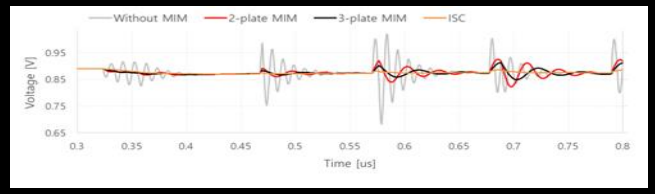
[EM Analysis]



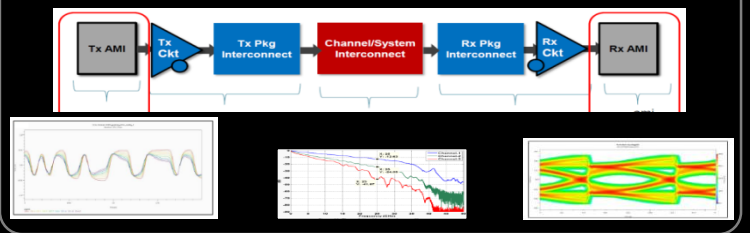
Adv. PKG Solution

- PSI Performance Estimation
- 2.5D/3D Design Optimization

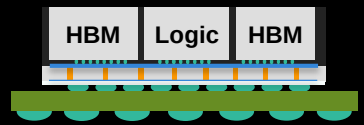
[System-level Voltage Maintenance]



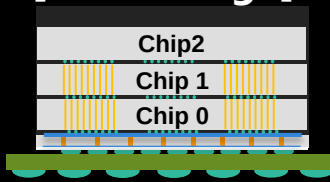
[Serdes Link Simulation]



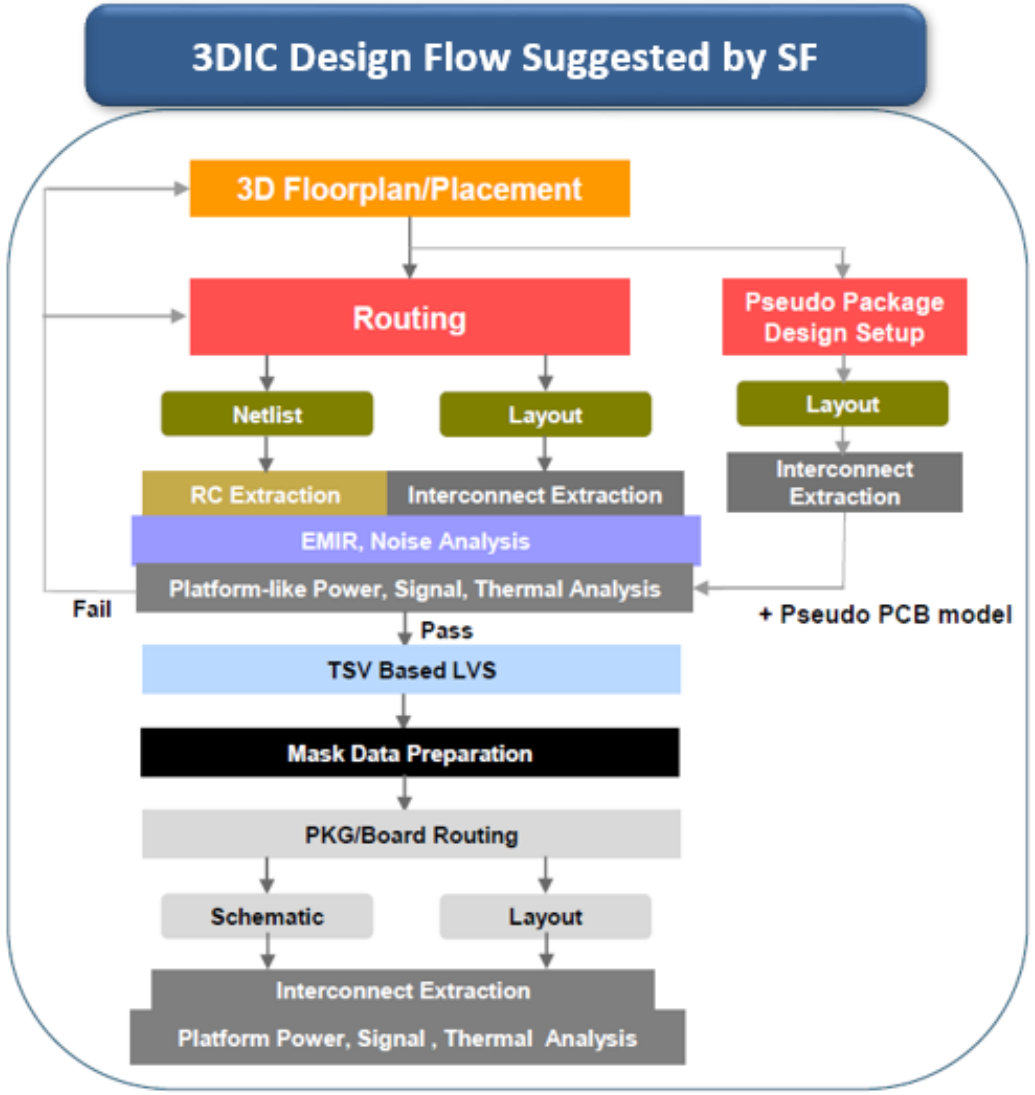
[2.5D Package]

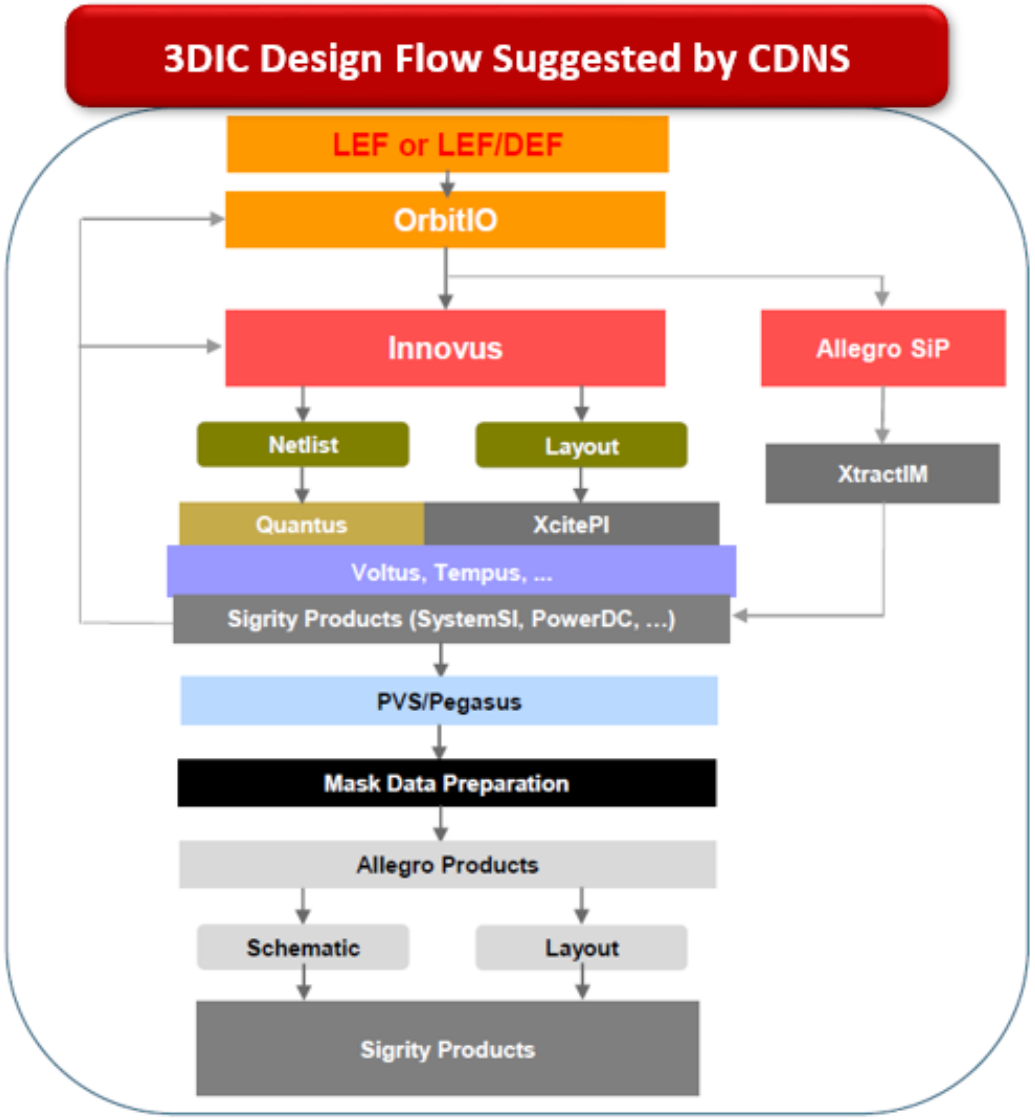


[3D Package]

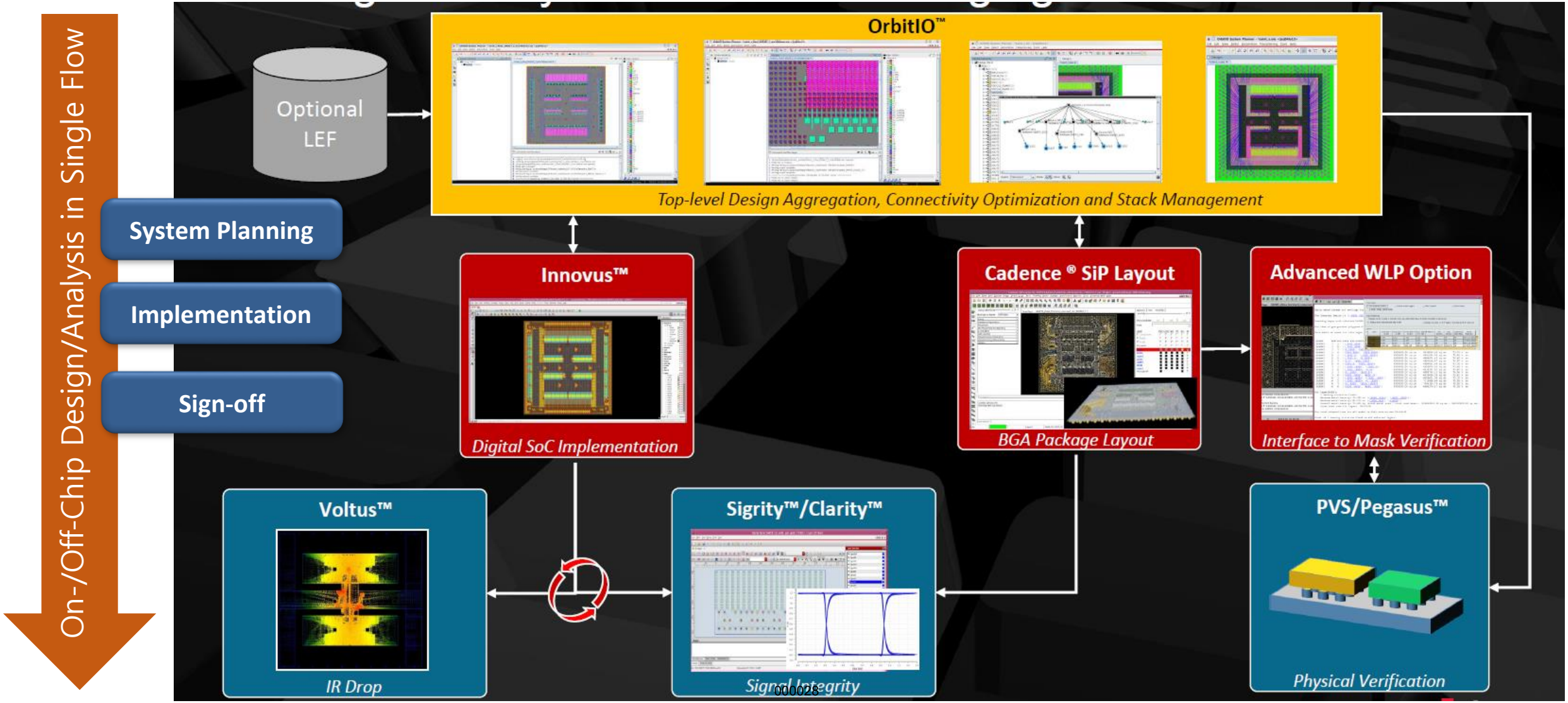


3DIC Design Flows





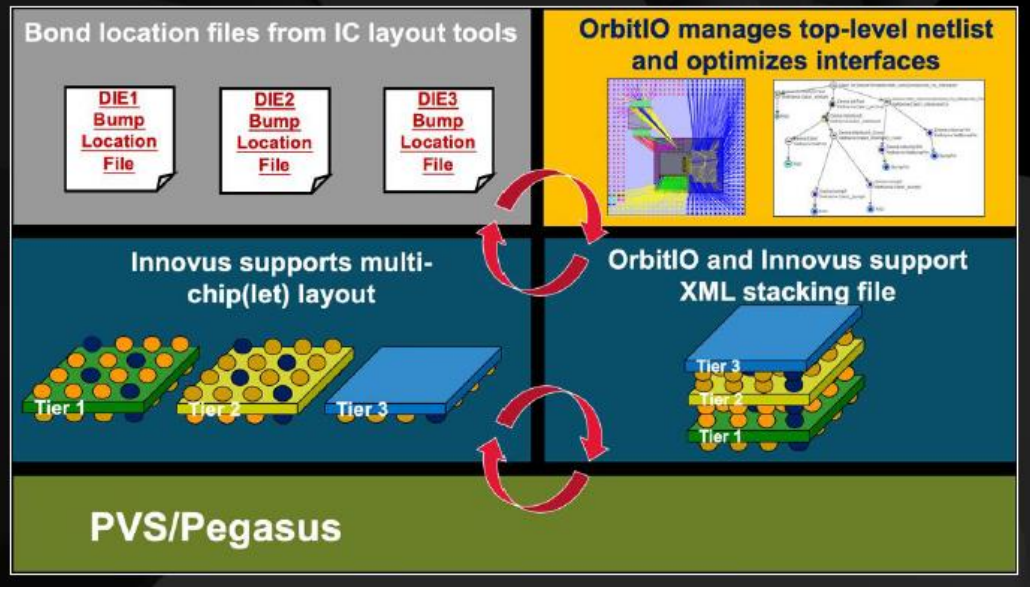
Cadence 3DIC Package Design Flow @Samsung



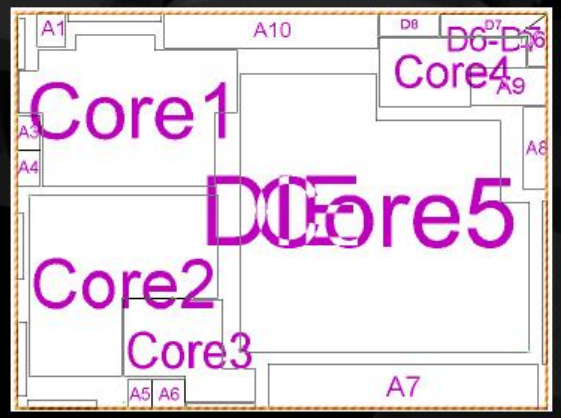
Contents

Top Level Planning and Design (using Cadence OrbitIO and Innovus)

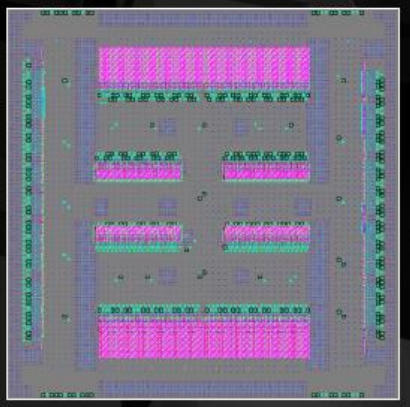
- MDI™ design planning capabilities
  - Early-phase floorplanning
    - With/without LEF
  - Bump/TSV automation
  - BGA pinout planning and optimization
  - Chip(let) stacking management



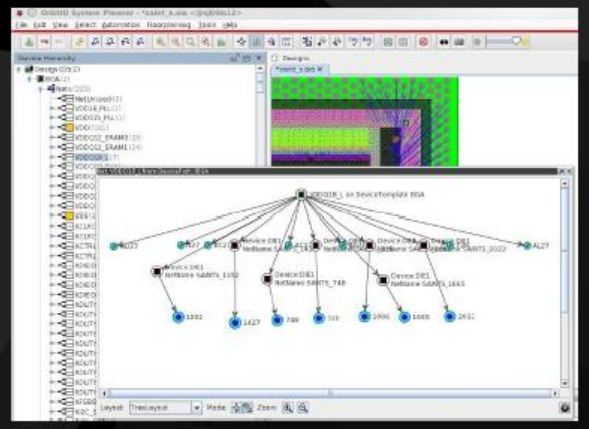
Chip-Level Floorplan



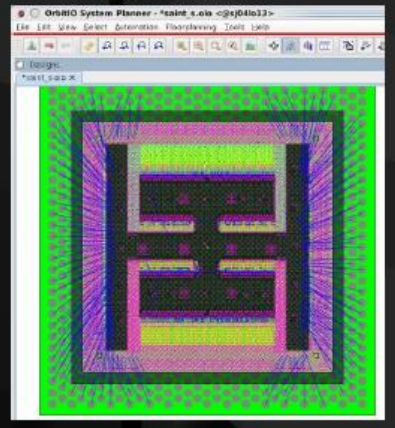
Bump/TSV Automation



Hierarchical Design and Net Management

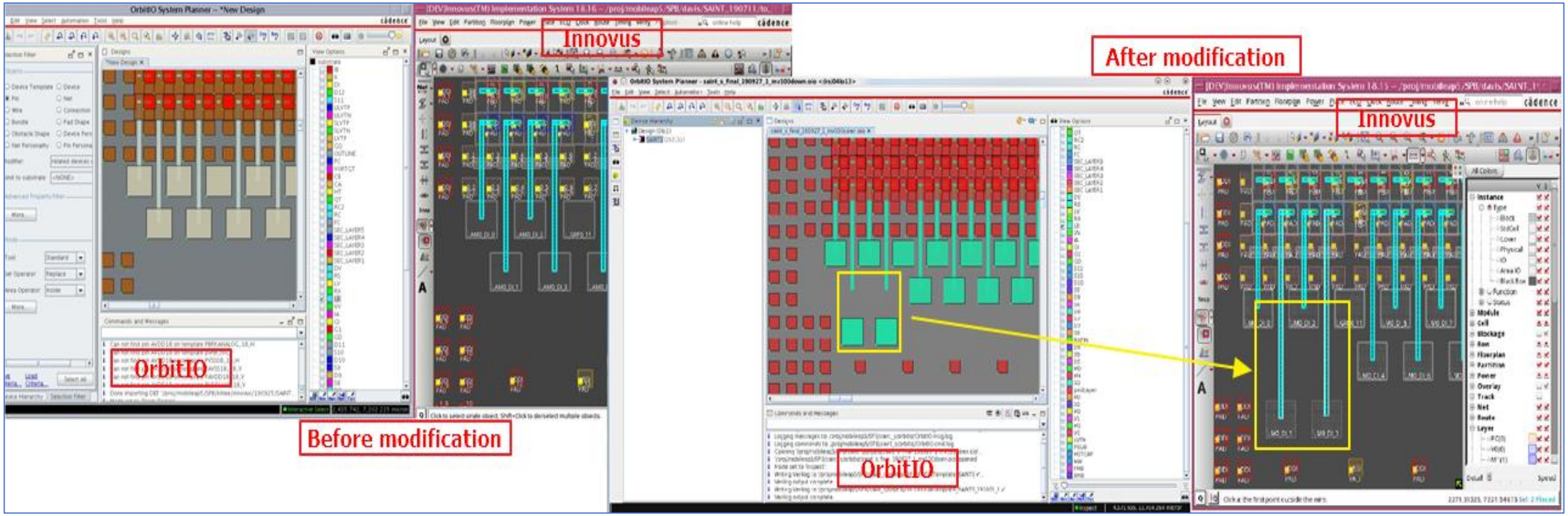


Chip-to-chip-to-BGA Interconnect Planning and Optimization



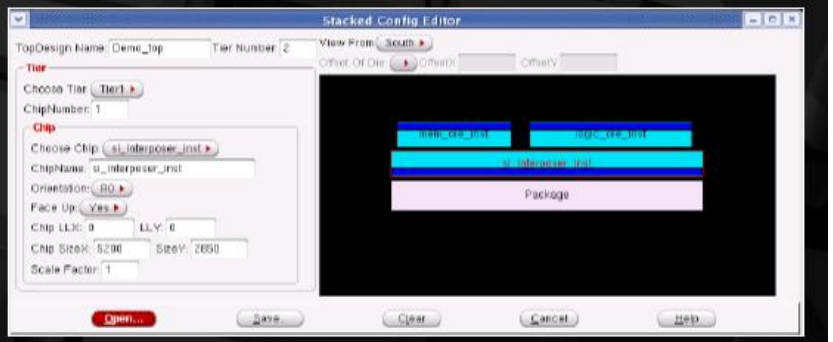
Top Level Planning and Design (using Cadence OrbitIO and Innovus)

- **Interchangeability between OrbitIO and Innovus when changing the location of TSV Cells**



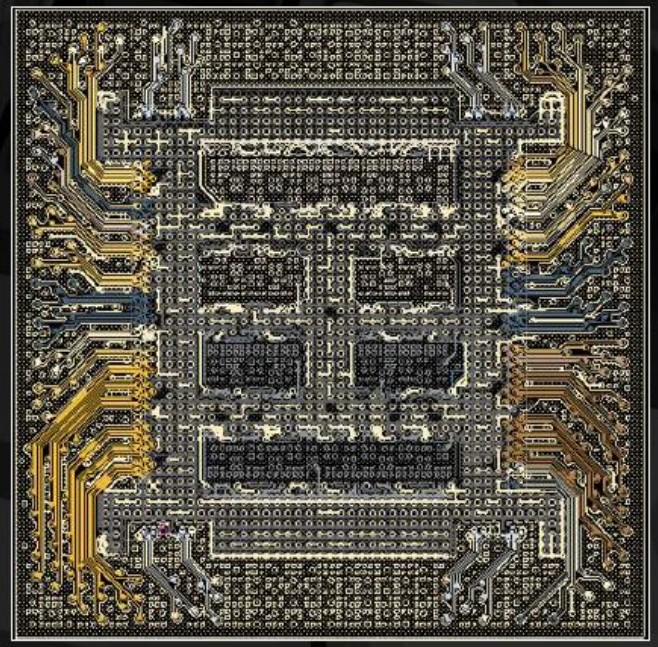
Stacked Die Design (using Cadence Innovus)

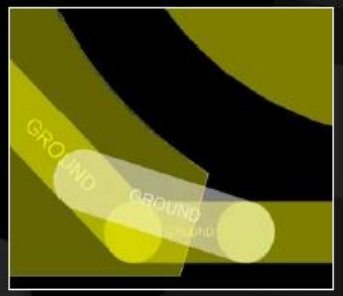
- Netlist-driven multi-die flow
  - Database 3D-aware (TSV, MB, uBump, etc.)
  - High-capacity implementation
  - Flow Based on die abstraction and bump files
  - GUI-based 3D stacking/tiering
- Seamless TSV/uBump creation
  - Specific 3D-IC commands for TSV/uBump creation, net assignment and routing
  - Built-in alignment micro-bond checks
- Advanced 45 degree auto-routing



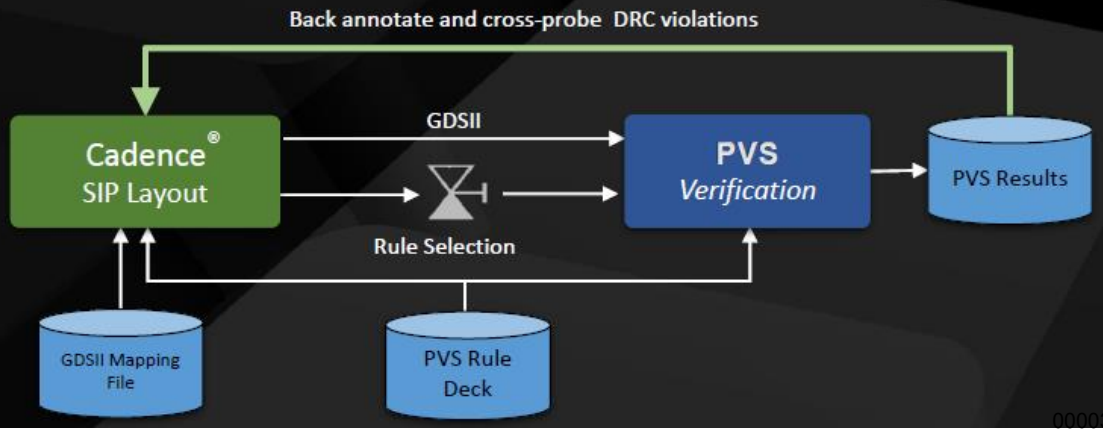
BGA Package Design (using Cadence SiP Layout)

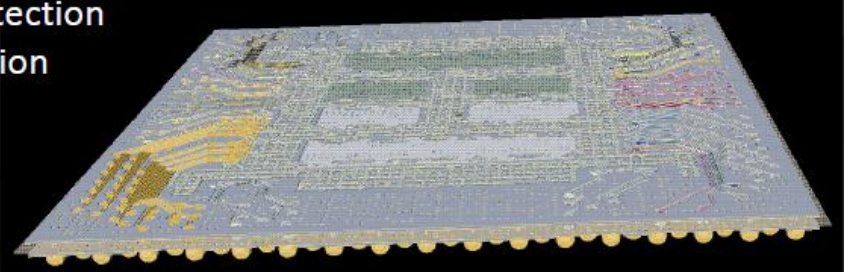
- Architected as a package/module design solution
  - Industry standard BGA/LGA design solution based on correct-by-construction architecture with real-time DRC
  - Support for all multi-chip(let) design styles
    - Bond wire, flip-chip, stacked, embedded, etc.
  - Optional support for FOWLP and silicon substrates
    - Advanced shape degassing, filleting and metal fill
    - Mask level DRC and LVS (PVS)





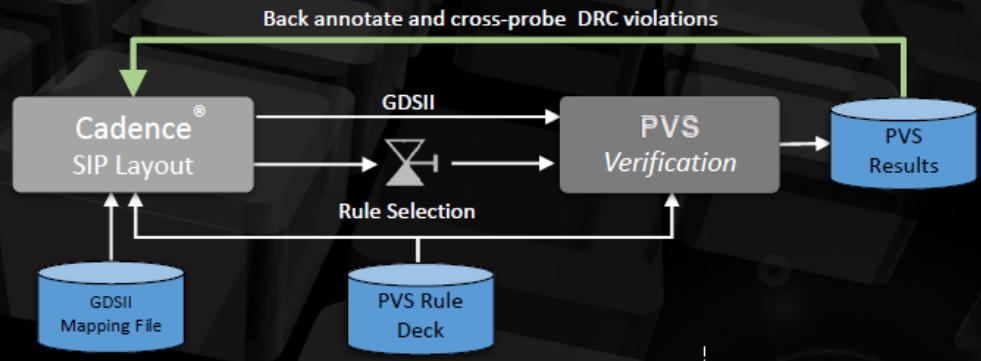
Acute Angle Detection and Correction

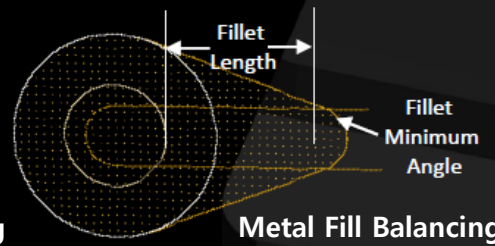




Physical Verification (using Cadence SiP Layout, PVS, Pegasus)

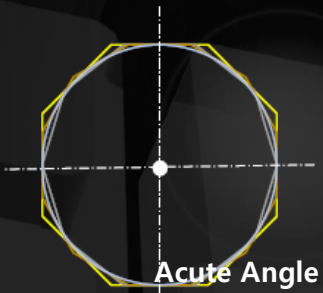
- Automatic pad degassing
  - Metal density balancing to meet manufacturing needs
  - Large pads, such as BGA balls, are too big to be solid metal
- Advanced filleting and acute angle identification with automatic coverage
  - All required to improve yield
- Progressive metal outgassing
  - Allows for additional, smaller patterns of holes in regions where density is still too high after initial degassing
- Advanced metal fill (balancing)
- Mask-level (GDSII) output data
  - Advanced arc vectorization
- Bidirectional interface with mask-level signoff tools
  - Works across MS Windows and LINUX



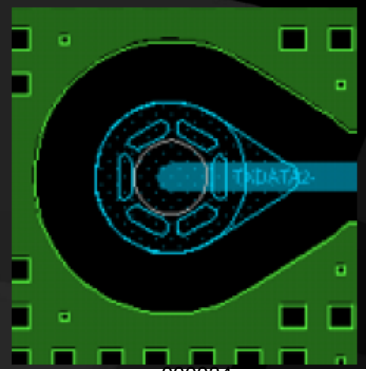


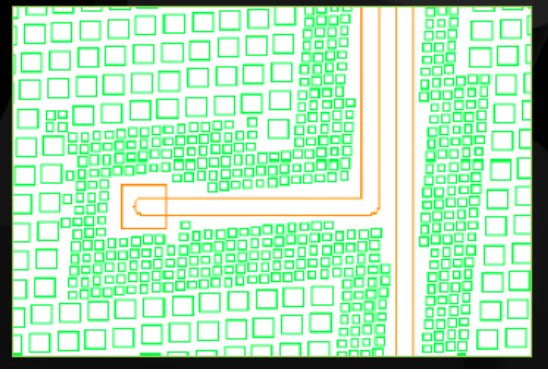
PAD Degassing

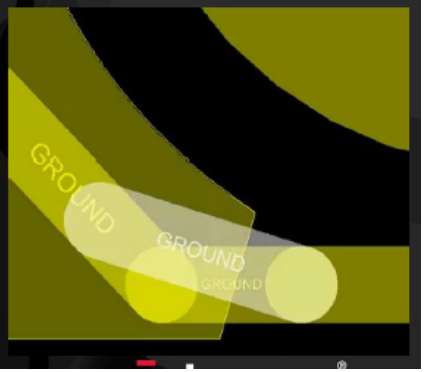
Metal Fill Balancing



Acute Angle Filling

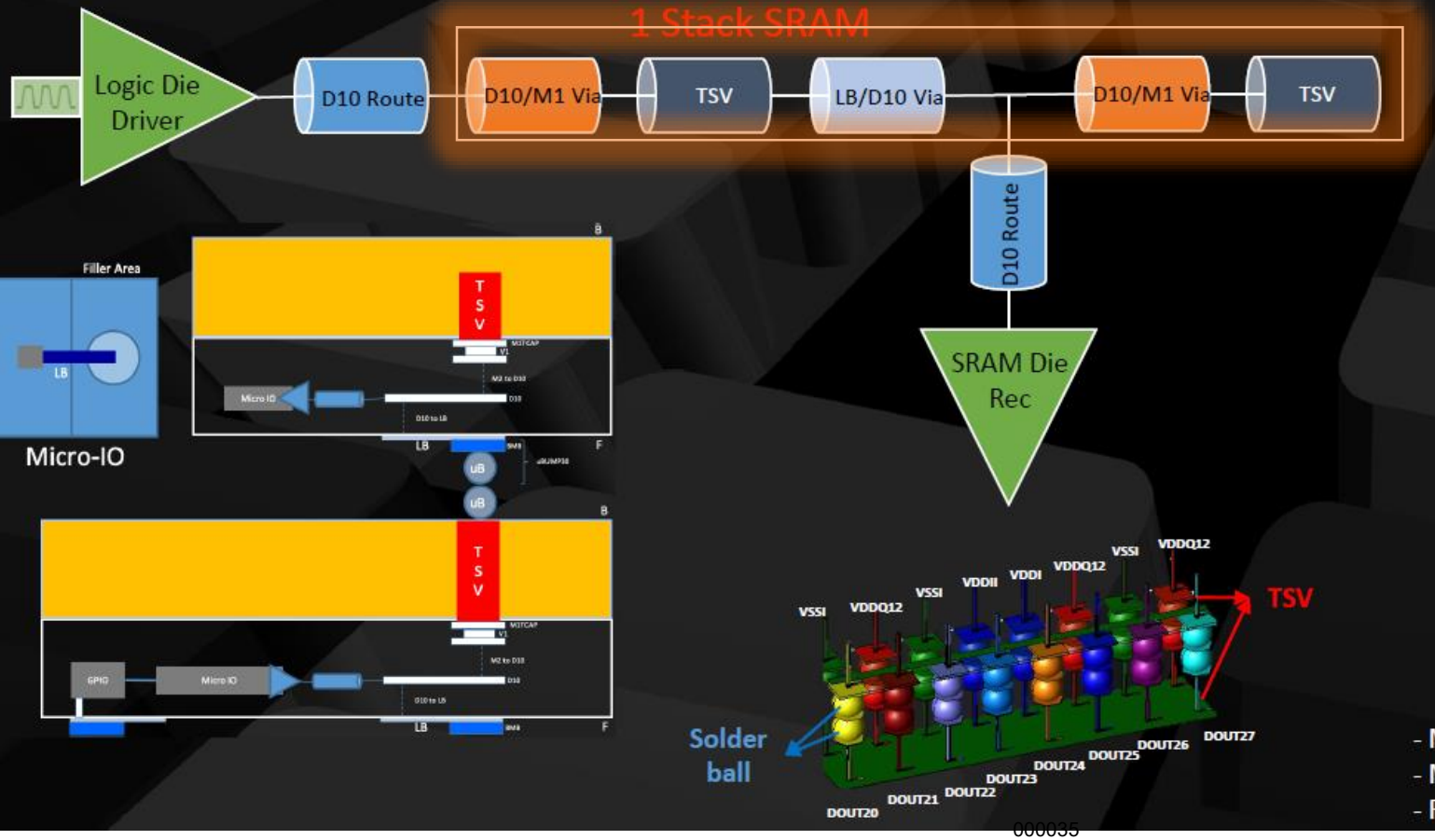


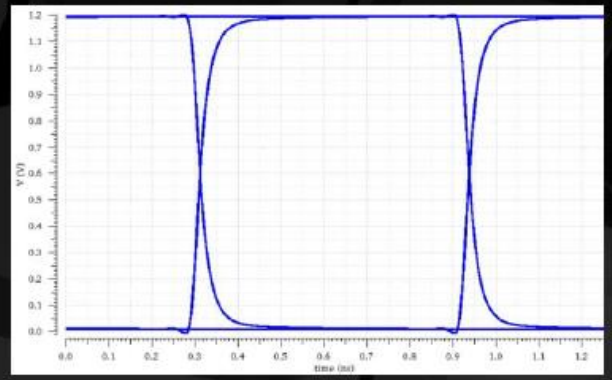


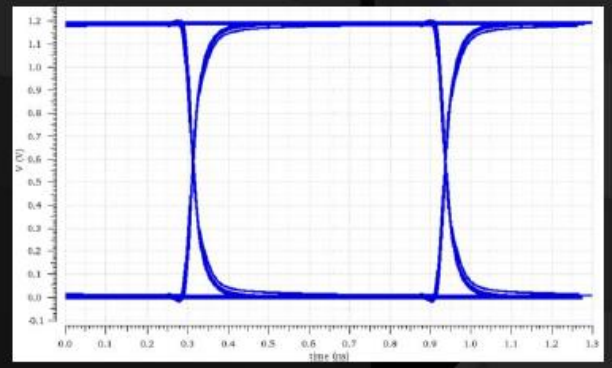


Signal Integrity for SRAM Interface (using Cadence Sigrity)

- Signal improvement and design flow verification through OrbitIO's optimization
  - Eye diagram analysis of two conditions – With and without crosstalk



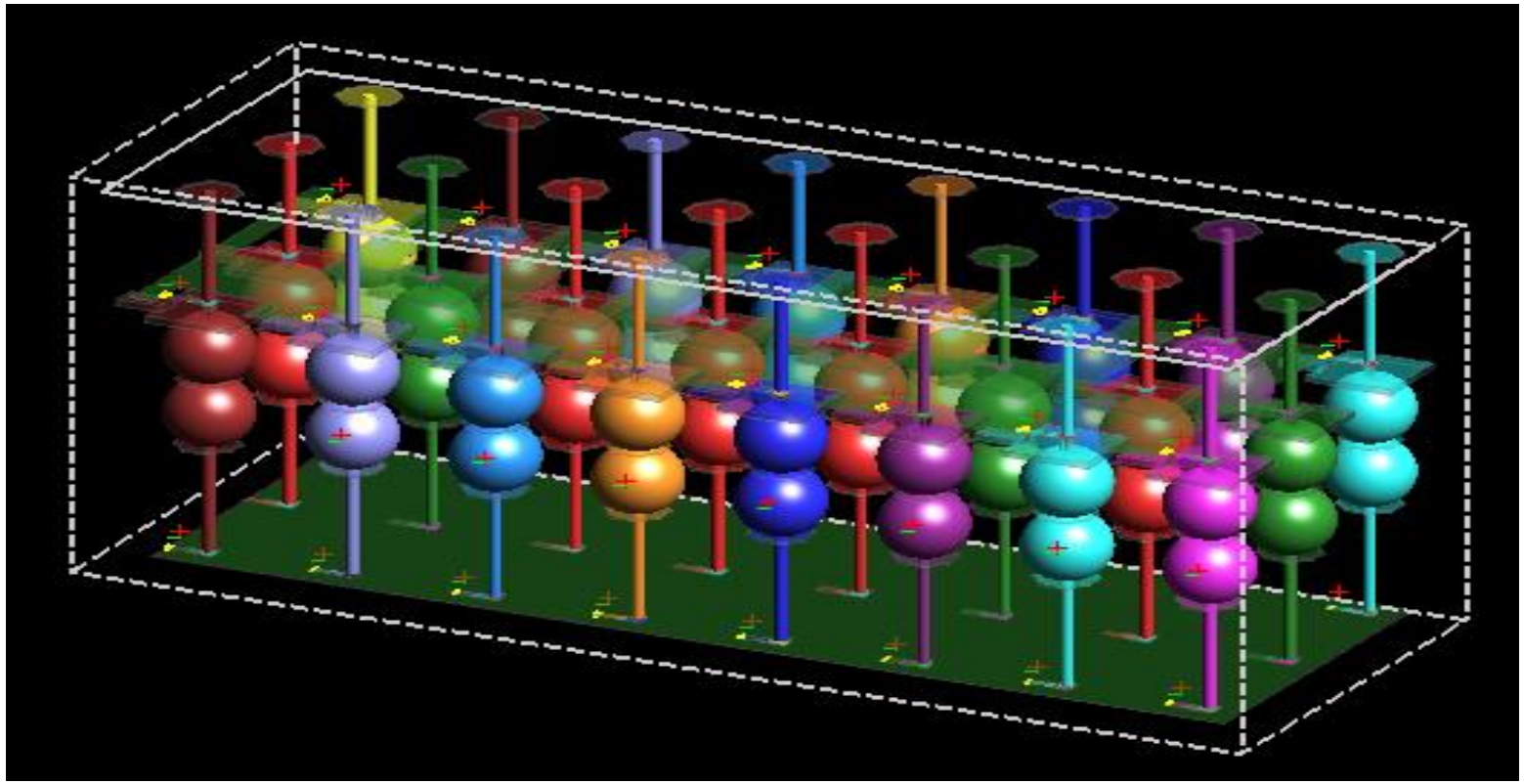


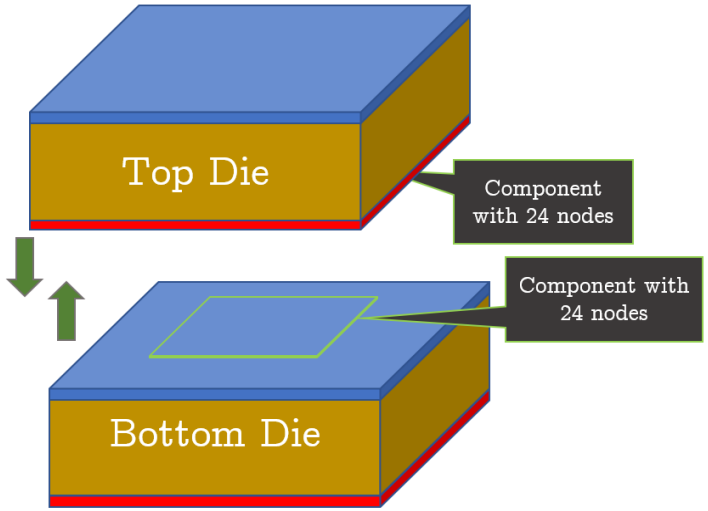


- Measurement Voltage: 0.4 V ~ 0.8 V (V_ref=0.6V +/- 0.2V)
- Measured at receiver IO model #4 (PAD)
- Frequency: 800MHz / Pattern

Modeling of Die Bonding + TSVs (using Cadence Clarity)

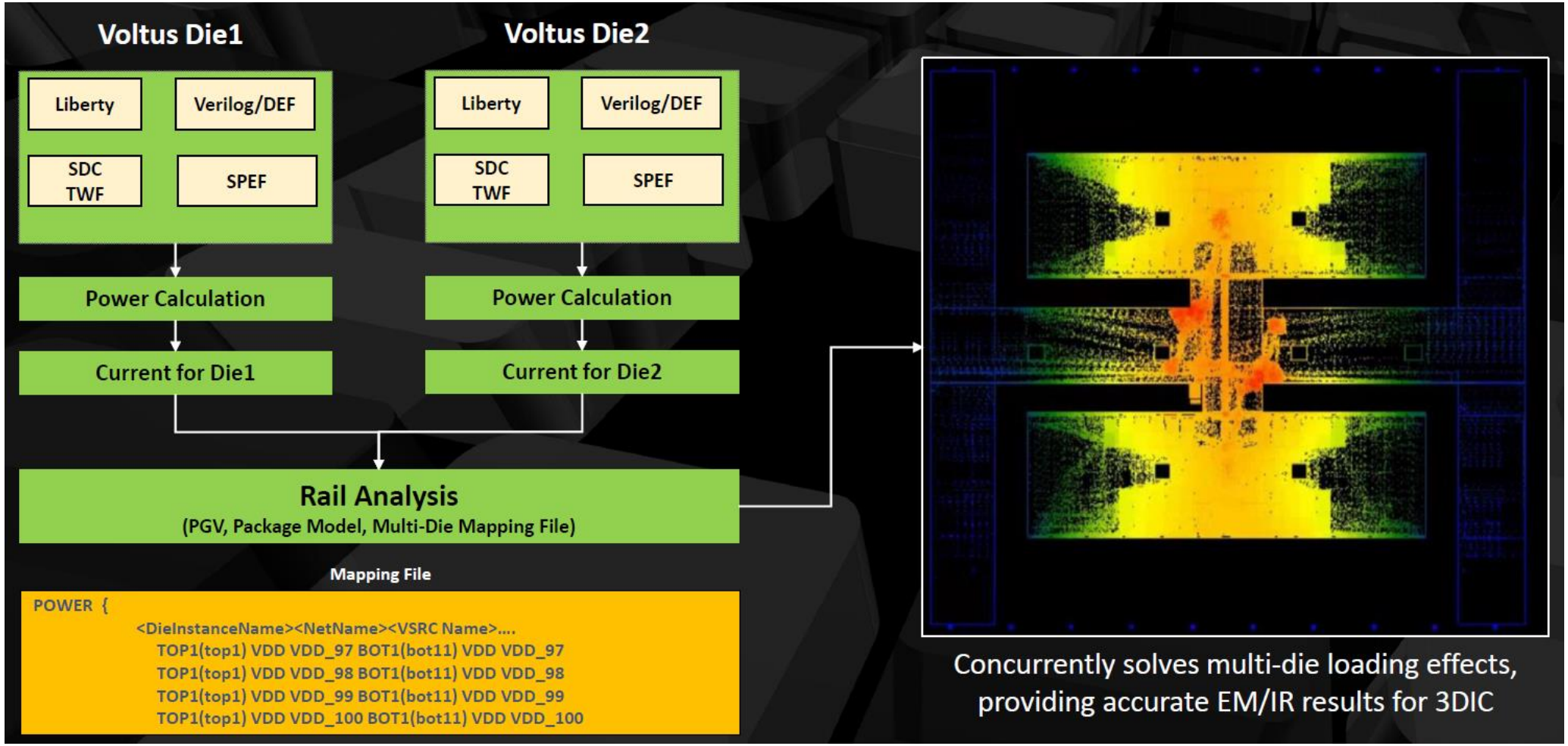
- **Modeling of die bonding area with TSV is the key feature for 3D stacked IC integration**





IR Drop (using Cadence Voltus)

- **Showing up the effect on stacked dies when changing the hot spots in each die**



Acknowledgement

The author would like to acknowledge Cadence team for fruitful discussion and support of this work.

Thank you!

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