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Thermal Management Implications for Heterogeneous Integrated Packaging
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Thermal Engineering
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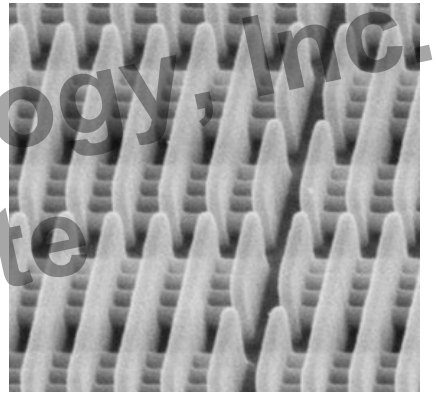
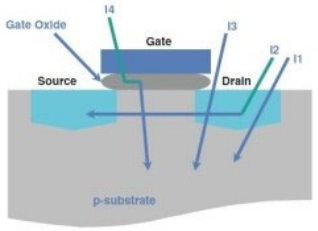
Outline

1. Power Dissipation in Semiconductors
2. Heterogeneous Packaging
3. Trends in High Performance Computing
4. HI Thermal Challenges and Solutions
5. Thermal Enhancement Implications

Power Dissipation in Semiconductors

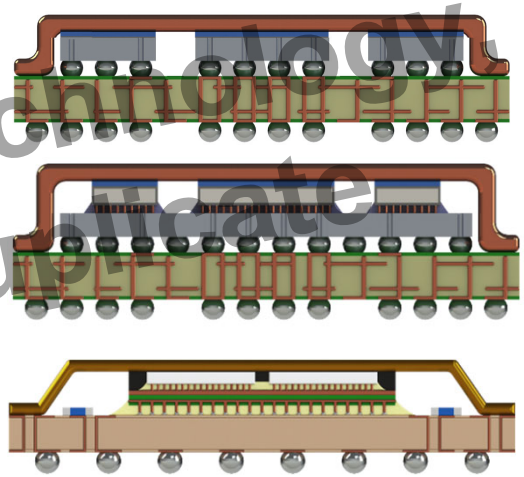
- Dynamic power
  - Switching power when charging or discharging capacitances
- Short circuit dissipation
  - Power dissipated by short-circuit connection between the supply voltage and the ground at the time the gate switches state
- Static power (leakage)
  - Result of unwanted subthreshold current in the transistor channel when it is turned off





Heterogeneous Packaging

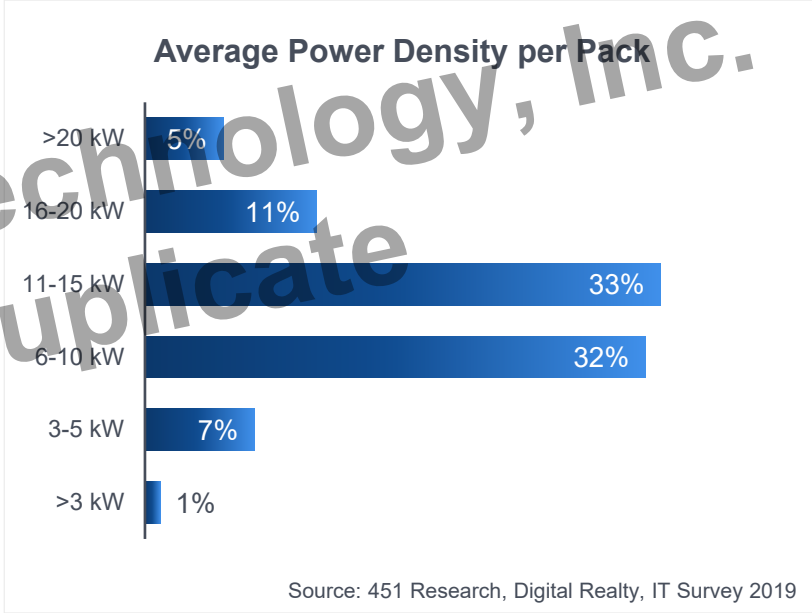
- Today, node shrink is no longer keeping pace with Moore's law
- Monolithic SoCs are becoming less economically viable
- HI is the breakdown of SoC functionality into individual chiplets or modules
- Numerous packaging approaches for heterogeneous integration



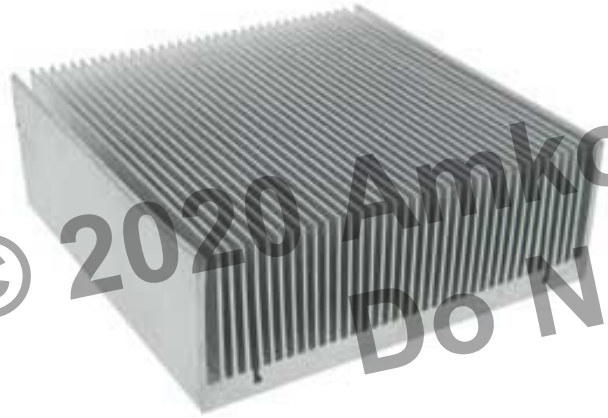
Trends in High Performance Computing

Power Density Trends in High Power Computing

- Tremendous growth in hyperscale data centers and machine learning AI
- Power per package is increasing, could exceed 1000 W in future
- Die power density >0.5 W/mm^2
- Sink-to-ambient thermal resistances <0.05°C/W

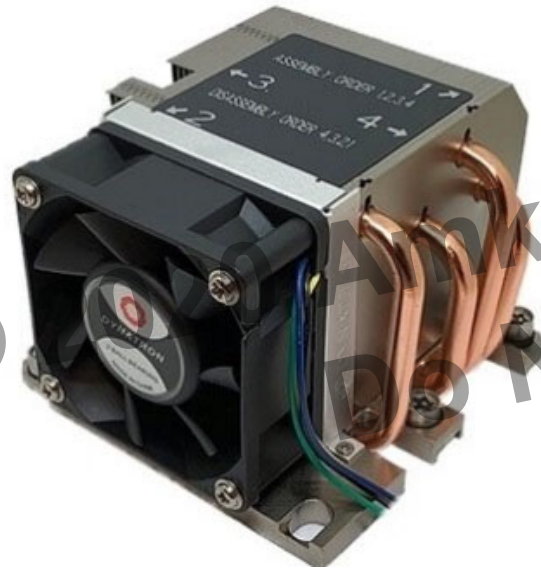


System Cooling Solutions



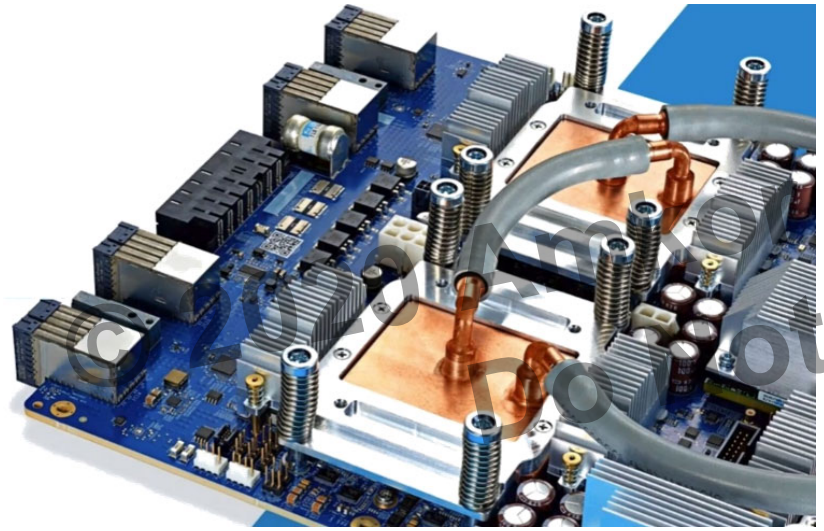
- Passive heatsink cooling
  - **<10 kW per rack**
  - Fans not directly mounted to heatsink, but to rack itself
  - Needs a lot of open rack space
  - Heatsinks are less efficient because they suffer flow bypass

System Cooling Solutions



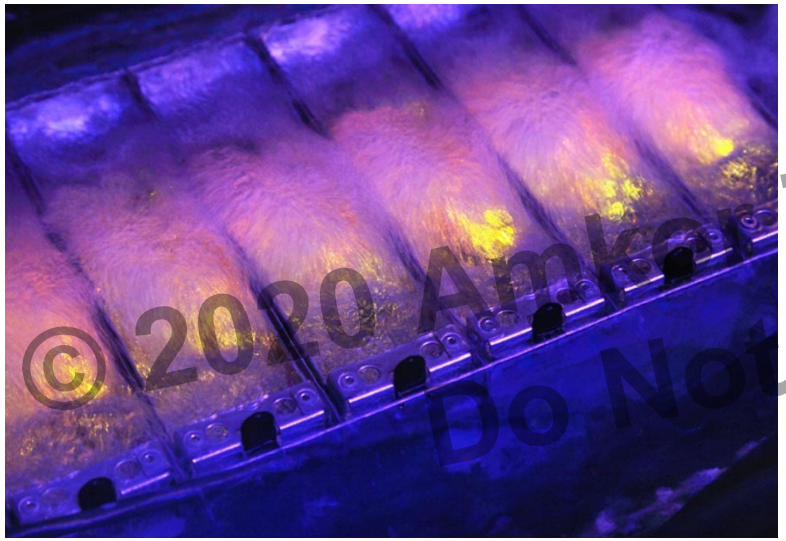
- Passive heatsink cooling
  - **10-15 kW per rack**
  - Offers better performance by directly attaching fans, therefore mitigating flow bypass between the heatsink fins
  - Often uses 2-phase closed loop liquid cooling devices

System Cooling Solutions



- Indirect liquid cooling
  - **>15 kW per rack**
  - Cooling fluid enclosed in plumbing
  - Can be very compact, utilizes less rack space
  - Does not suffer temperature gradient through rack height
  - Open compute project

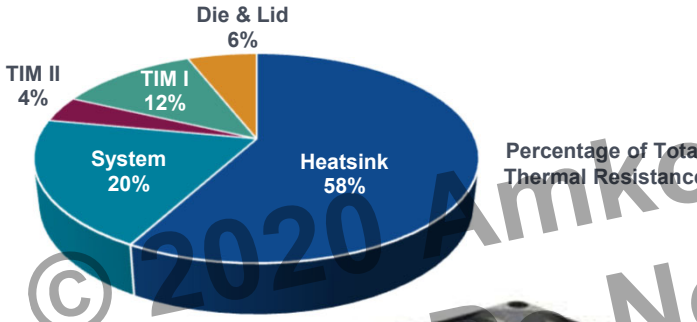
System Cooling Solutions



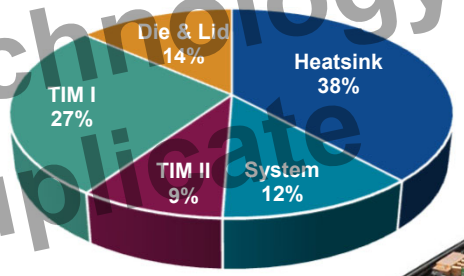
- Liquid immersion cooling
  - **>20 kW per rack**
  - Entire system submerged in dielectric fluid
  - Can operate in single phase or 2-phase depending on fluid
  - Requires new infrastructure
  - Open compute project

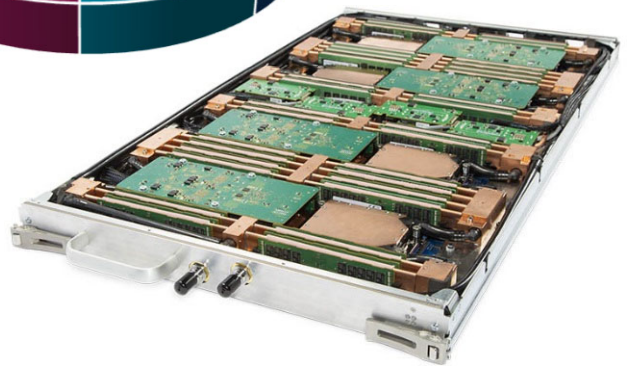
Contribution of Package

Air Cooled System



Advanced Cooled System (such as liquid cooling)

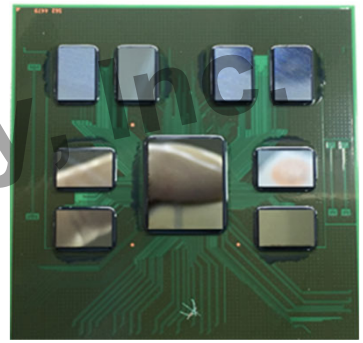


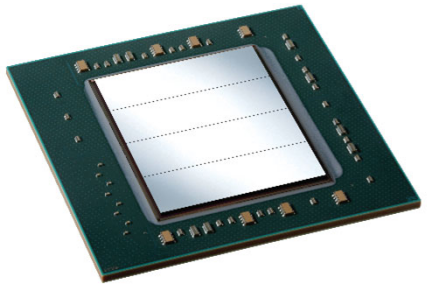


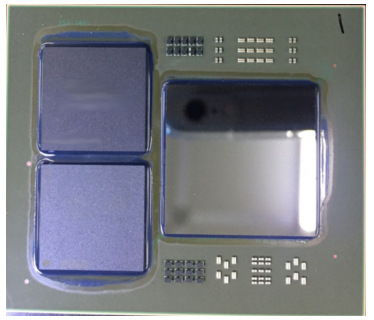
Thermal Challenges and Solutions

Traits of a High-Power Heterogeneous Package

- High I/O count → large body size
- Large total surface area of chiplets or components
- Highly non-uniform power density
- Different materials interfacing heat spreader
- Different component heights



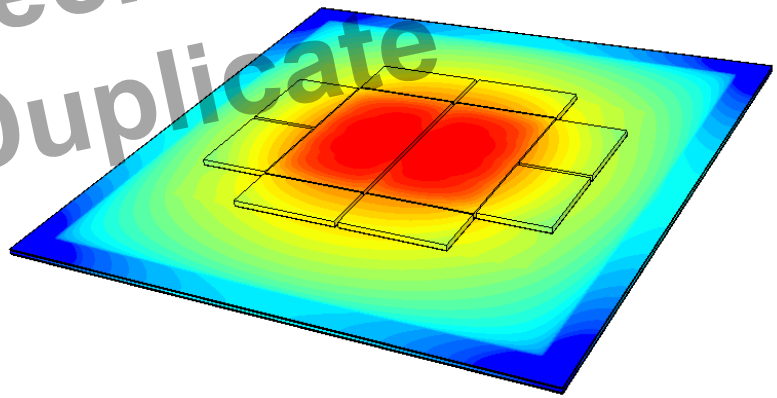




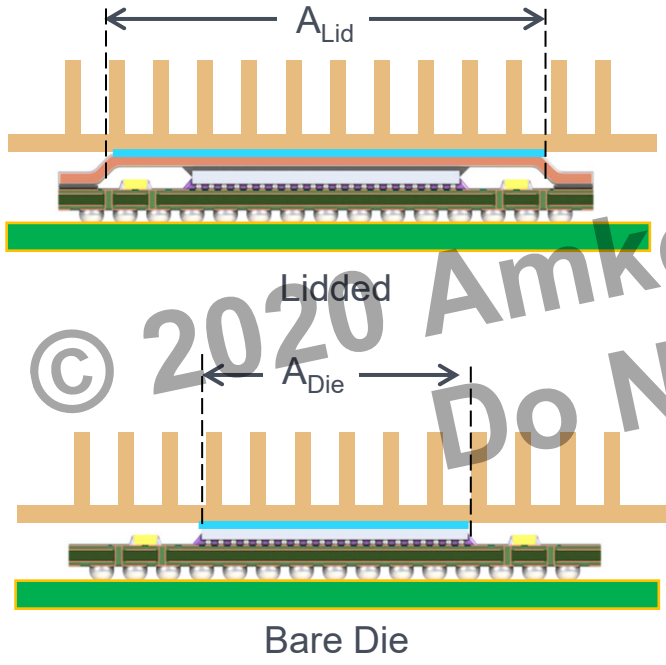
Thermal Considerations for HI Packaging

- Bare die or lidded
- Lid thickness
- TIM I
- Die layout
- System cooling solution
- TIM II
- Power map

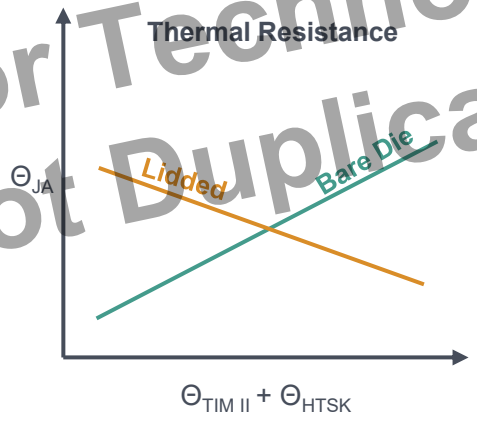
OSAT Focus

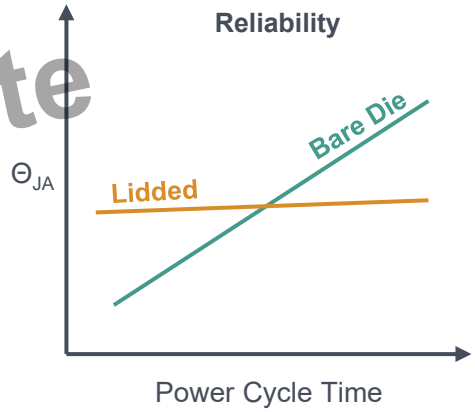


Bare Die vs Lidded Tradeoffs



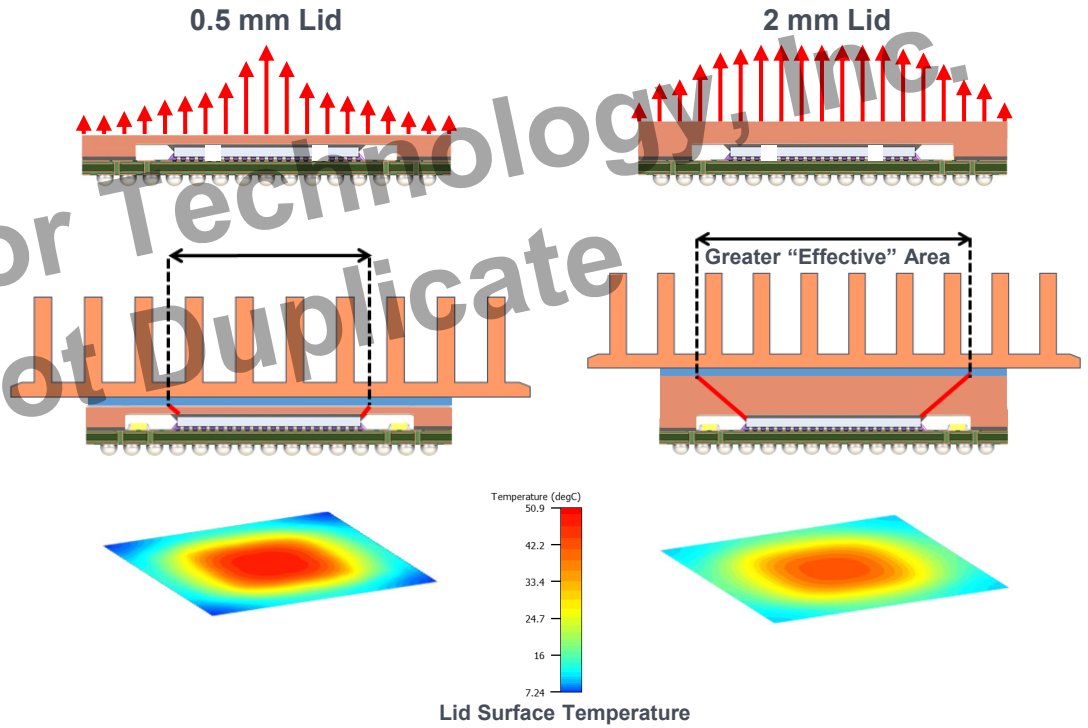
$$\Theta_{JA} = \frac{T_J - T_{AMB}}{P} = \Theta_{JC} + \Theta_{TIM\ II} + \Theta_{HTSNK}$$





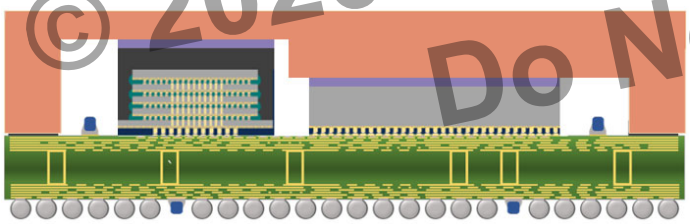
Heat Spreader Thickness

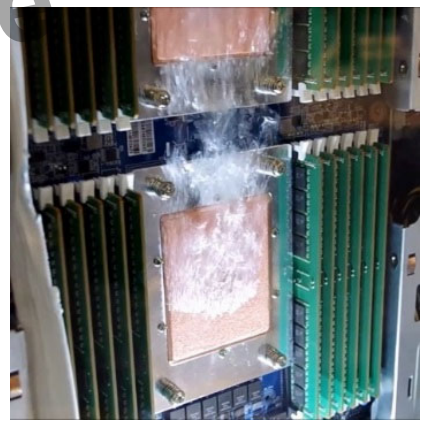
- Highly non-uniform power distribution can benefit from thick lids
- Uniform heat distribution on lid offers best case for heatsink "efficiency"
  - TIM II resistance is effectively reduced due to area, R = BLT / (k*A)



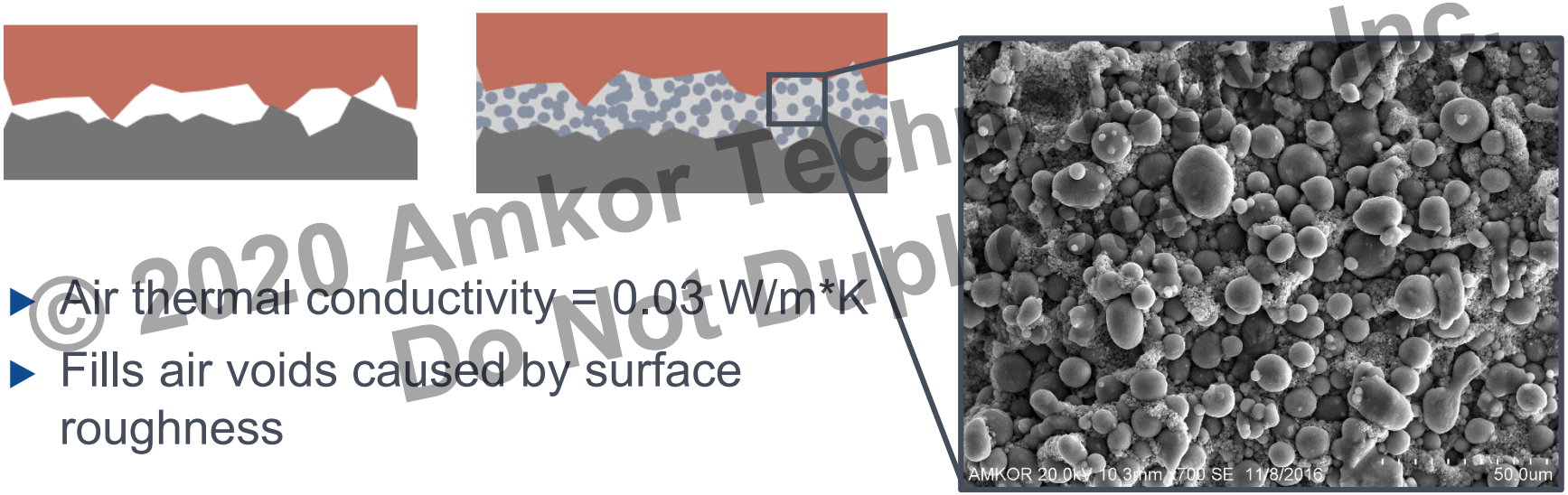
Additional Benefits of Heat Spreaders

- Protect silicon
- Compensate for different height components
- Increased nucleation sites in immersion cooling if surface roughened





Thermal Interface Materials



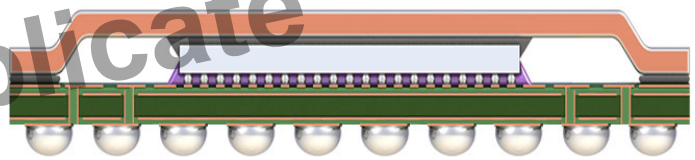
- Air thermal conductivity = 0.03 W/m*K
- Fills air voids caused by surface roughness

What Affects TIM Resistance in a Package?

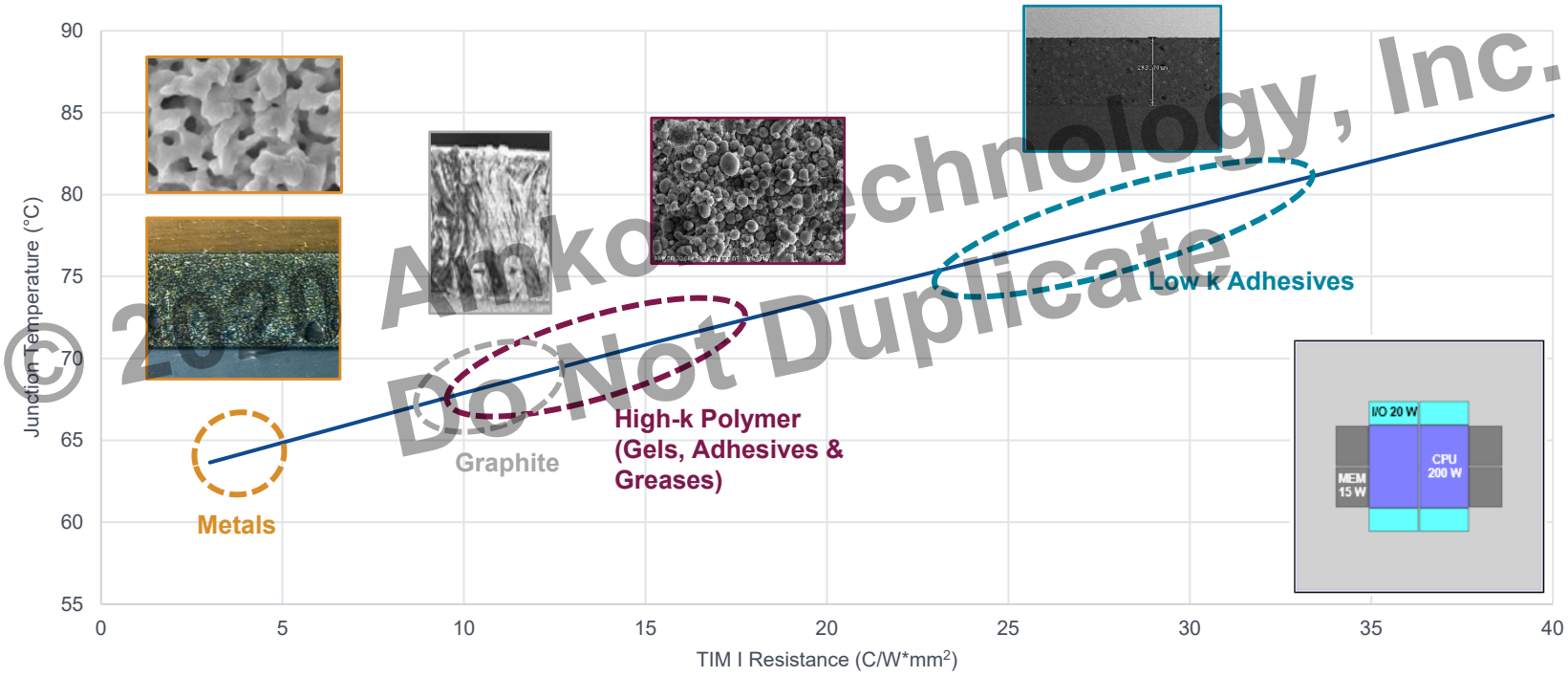
$$R_{TIM} = \frac{BLT}{k * A} + R_{Contact}$$

- **Bondline Thickness**
- **Thermal Conductivity**
- **Contact Resistance**

- Filler Particle Size/Density
- Filler Particle Conductivity
- Package Warpage
- Stress State and History
- Lid Attach Process
- Cure Condition
- Clamping Pressure
- Lid/Die Surface Roughness
- Surface Wettability
- Adhesive/Cohesive Bonding

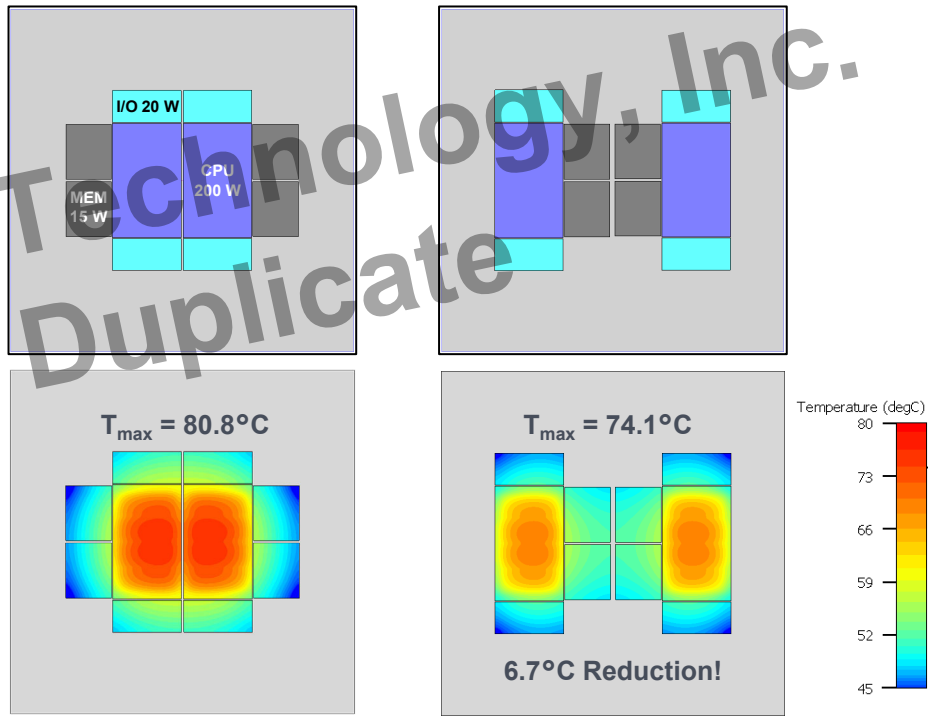


TIM I Effect on Large MCMs



Component and Chiplet Organization

- Spacing between high power die can significantly impact temperatures
- Design for thermal performance may be achievable while maintaining electrical performance
- High power die should still not be placed too near package corners



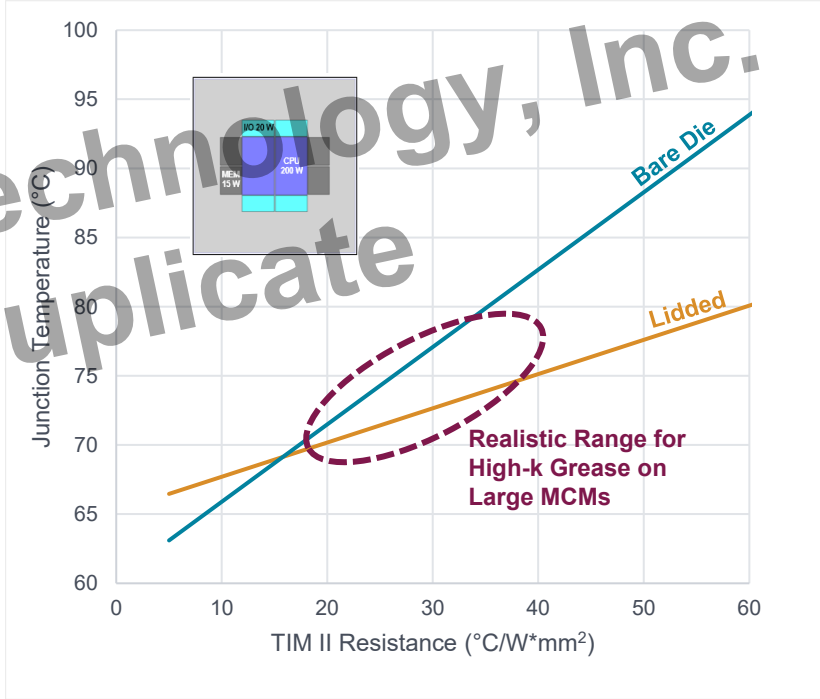
System Integration

TIM II Effect on Bare Die vs Lidded

- Surface area in contact with heatsink is much smaller for bare die
- TIM II conductivity with bare die must be much higher to be equivalent to lidded due to surface area

  $R = BLT/(k*\mathbf{A})$

- Large MCMs require high clamping force to achieve adequate pressure on TIM II (P = F/A)



Heatsink Mounting

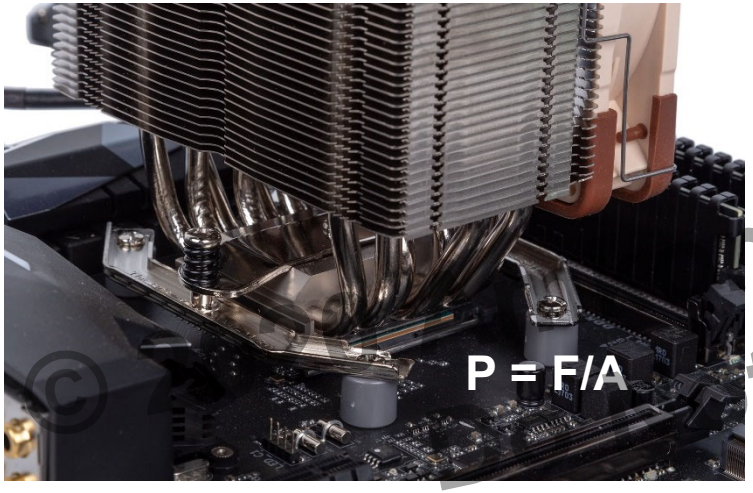
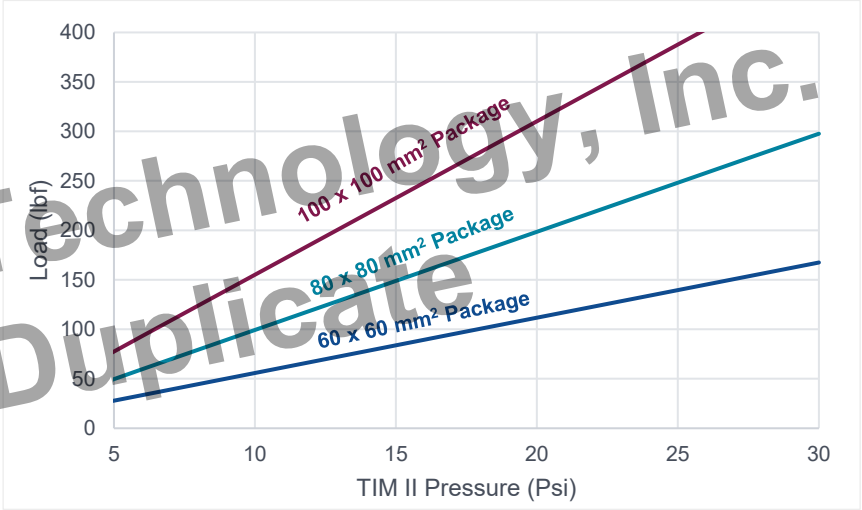


Image Source: Bit-Tech Reviews

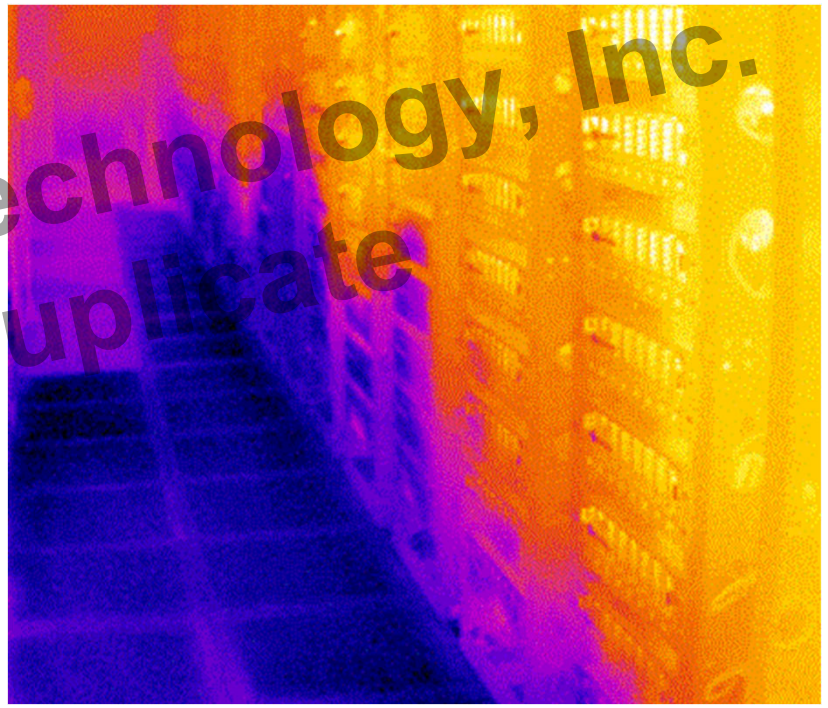


- TIM II requires adequate pressure for low thermal resistance
- Load can be significant for large packages

Implications of Thermally Enhancing a Package

Implications of Thermal Enhancement

- Improved Theta JC offers
  - Lower junction temperature, longer operating life
    - Rule of thumb: for every 10°C increase, life is reduced by half
  - Can operate device at higher power



Implications of Thermal Enhancement

- Improved Theta JC offers
  - Decreased cooling system requirements
    - Smaller heatsinks
    - Lower airflow
  - Can increase ambient temperature, reducing cooling system workload
    - $T_j - T_{amb}$ is decreased due to ΘJC
    - 1°C increase in ambient results in ~2% cooling cost savings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