

Get MOoRE out of the Package

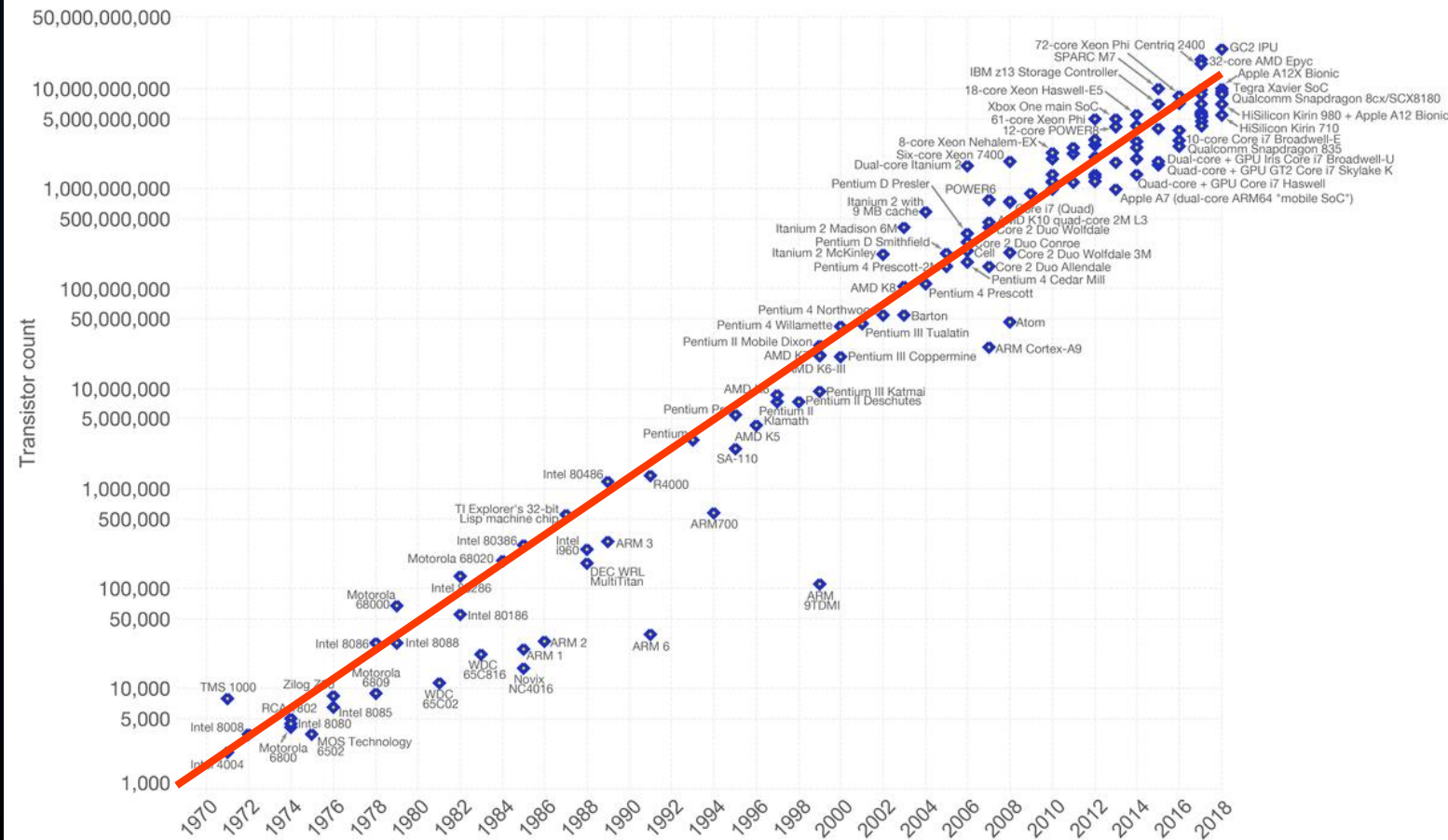
IMAPS Program:

- *“Integration”: 46x*
- *“HETEROGENEOUS”: 19x*
- *“Chiplet”: 10x”*

Interpretations of Moore's Law

Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.



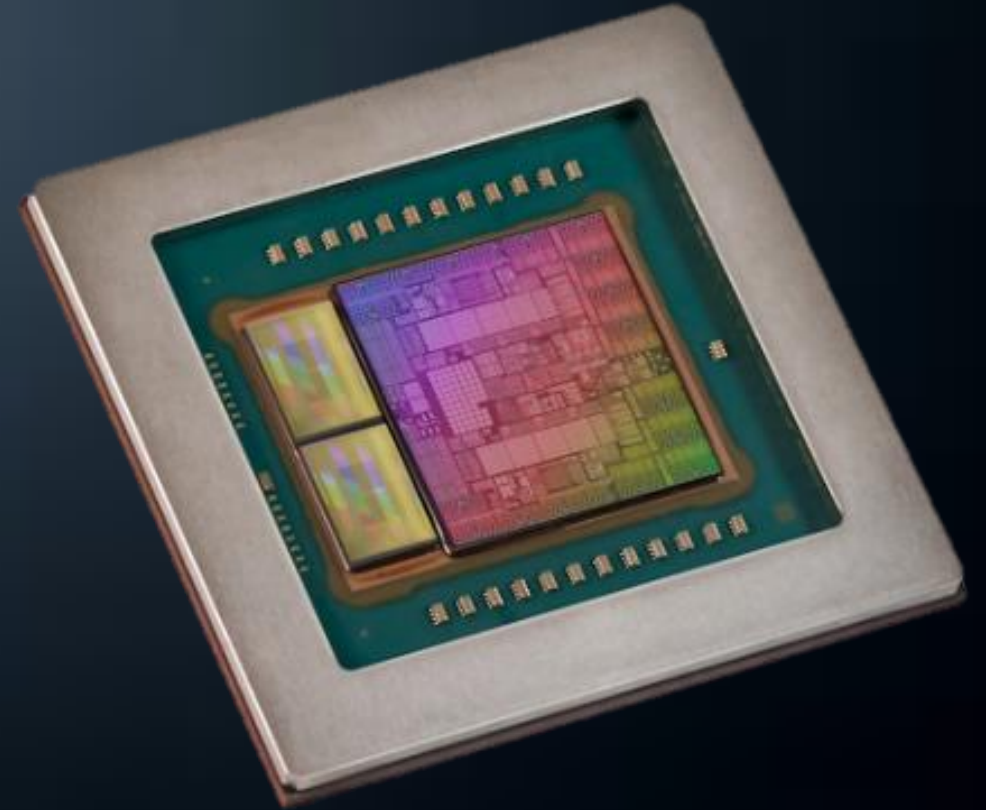
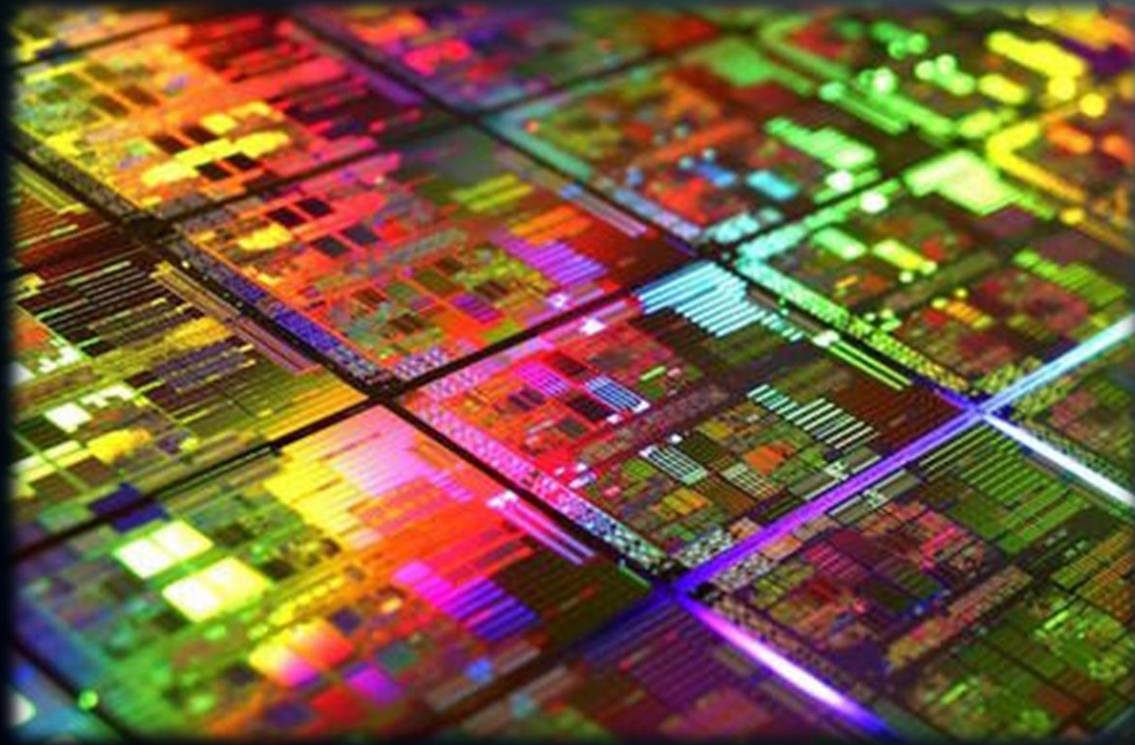
Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

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- Is it Technology Scaling?
- Is it Economic?
- Is it Performance?
- Is it Function?
- Is it an Observation?
- Is it all of the Above?

- Or does it not matter?

Products are Modules, not Chips



What Do Next-Generation Products Need?



**Wireless / 5G
Infrastructure**



Compute



Networking



What Do Next-Generation Wireless Products Need?

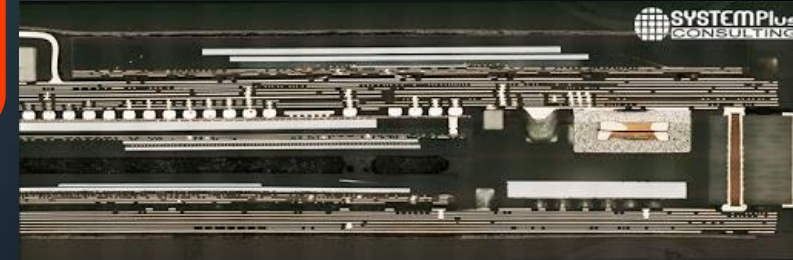


Wireless / 5G Infrastructure



Handheld

- Ultimate density requirements
- Memory integration
- RF Integration
- Next Gen for Power & Perform.
- Cost



Wireless Infrastructure

- Antenna (array)
 - RF integration
 - Power
 - Cost
 - Small Area
 - Thermal

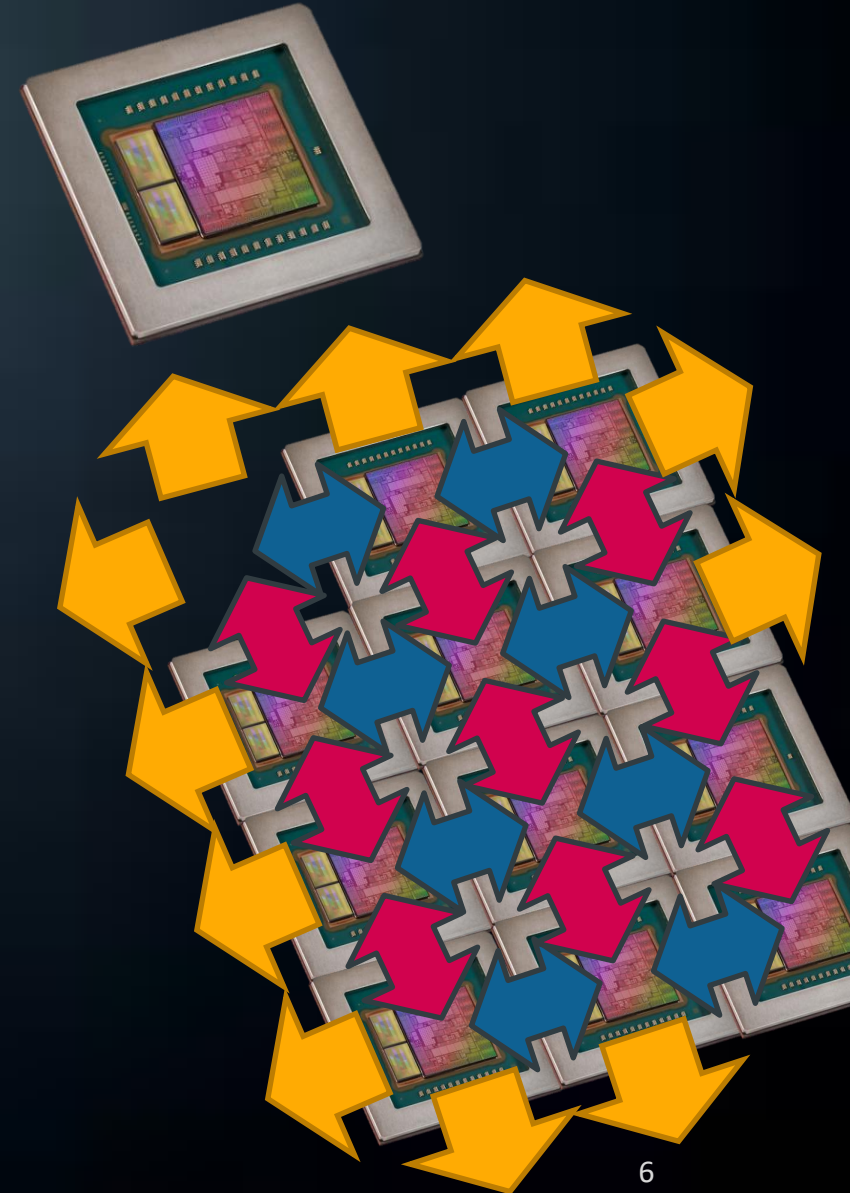
- Baseband
 - Modularity
 - Power
 - Cost
 - Thermal

What Do Next-Generation Compute Products Need?

- Performance
 - Next Gen Technology
- Power efficiency
- Cost
- Memory bandwidth
- Scalable compute systems with high C2C bandwidth
 - Drives huge bandwidth between chips
 - (e.g. CHIPS, Cerebras)

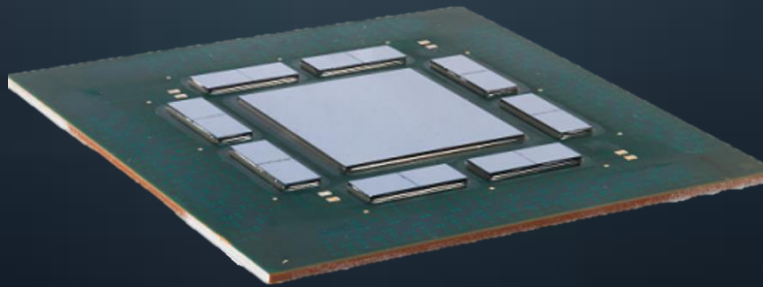


Compute



What Do Next-Generation Networking Products Need?

- More Si Area than can fit in a reticle
- More bandwidth
 - Between chips
 - Off-module
- Larger package
- Lower package loss
- Huge amount of power
 - Coupled with HBM integration



Marvell Falcon 12.8T Switch



Networking



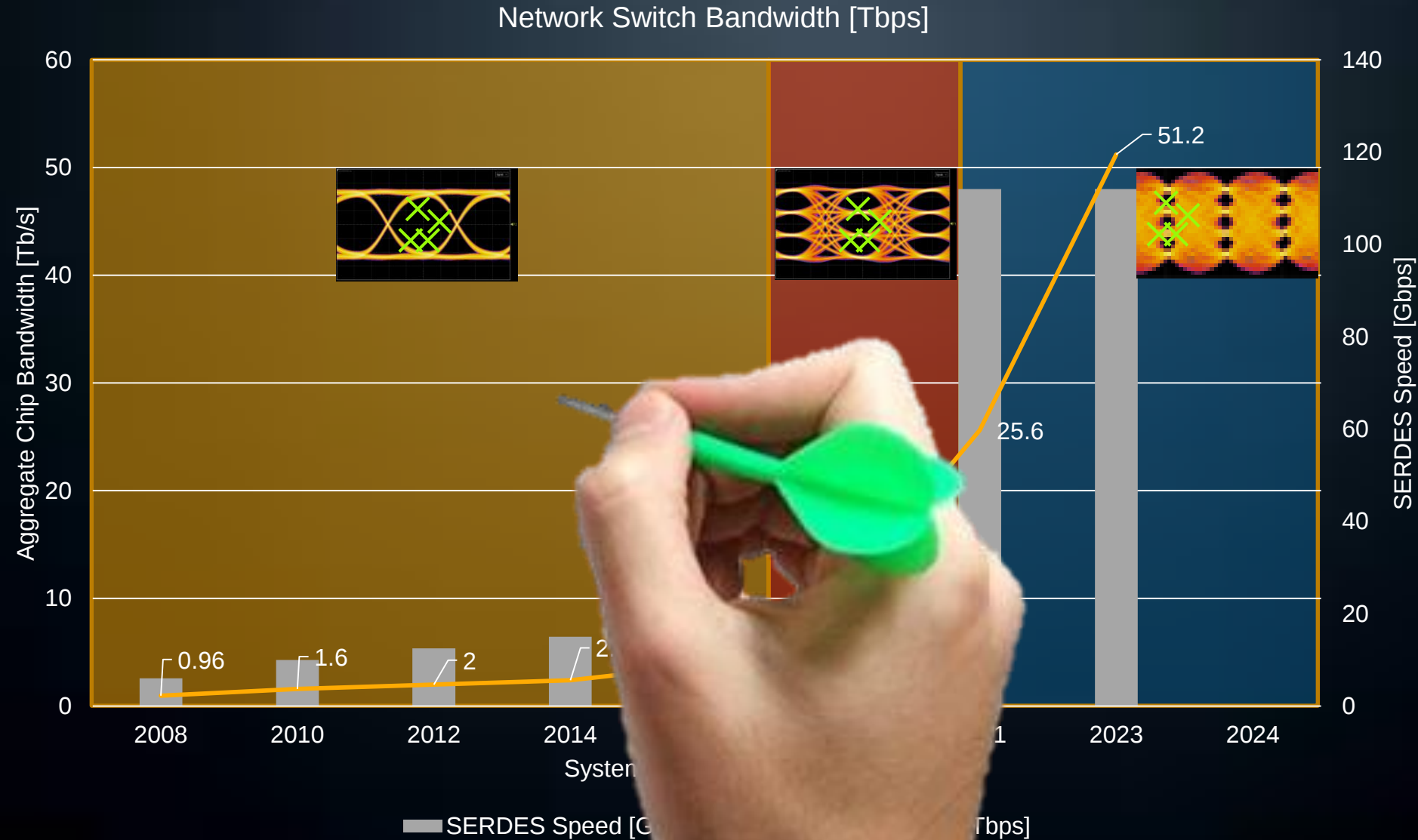
Forget about the Chip

Get MORE out of the Package

OK... but More WHAT?

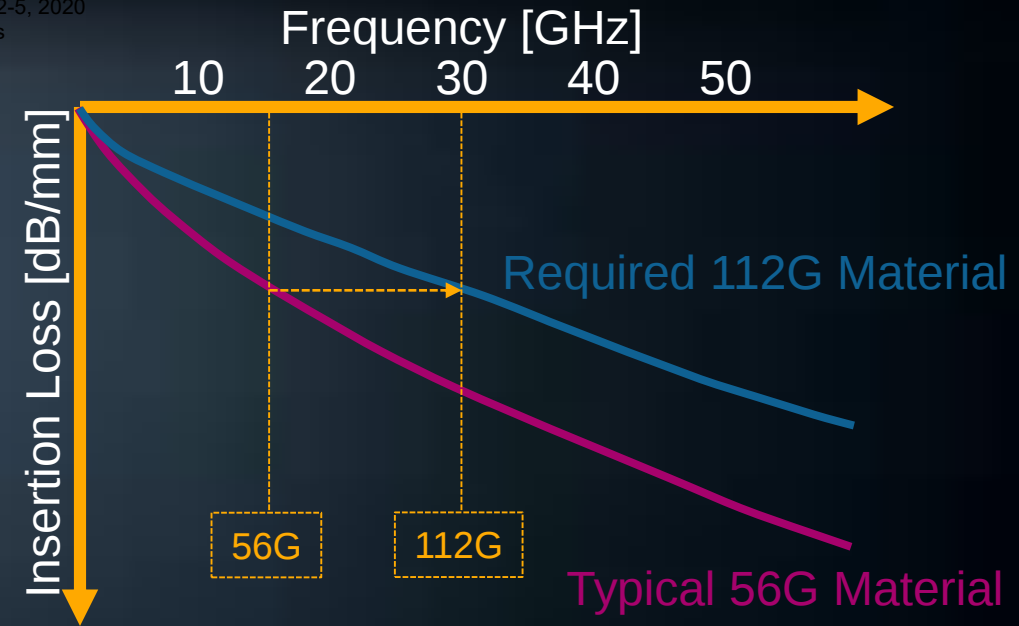
- Get more data out of the package
- Get more functionality out of the Package
- Get more cost out of the package

Get more Data out of the Package: Network Switch Roadmap

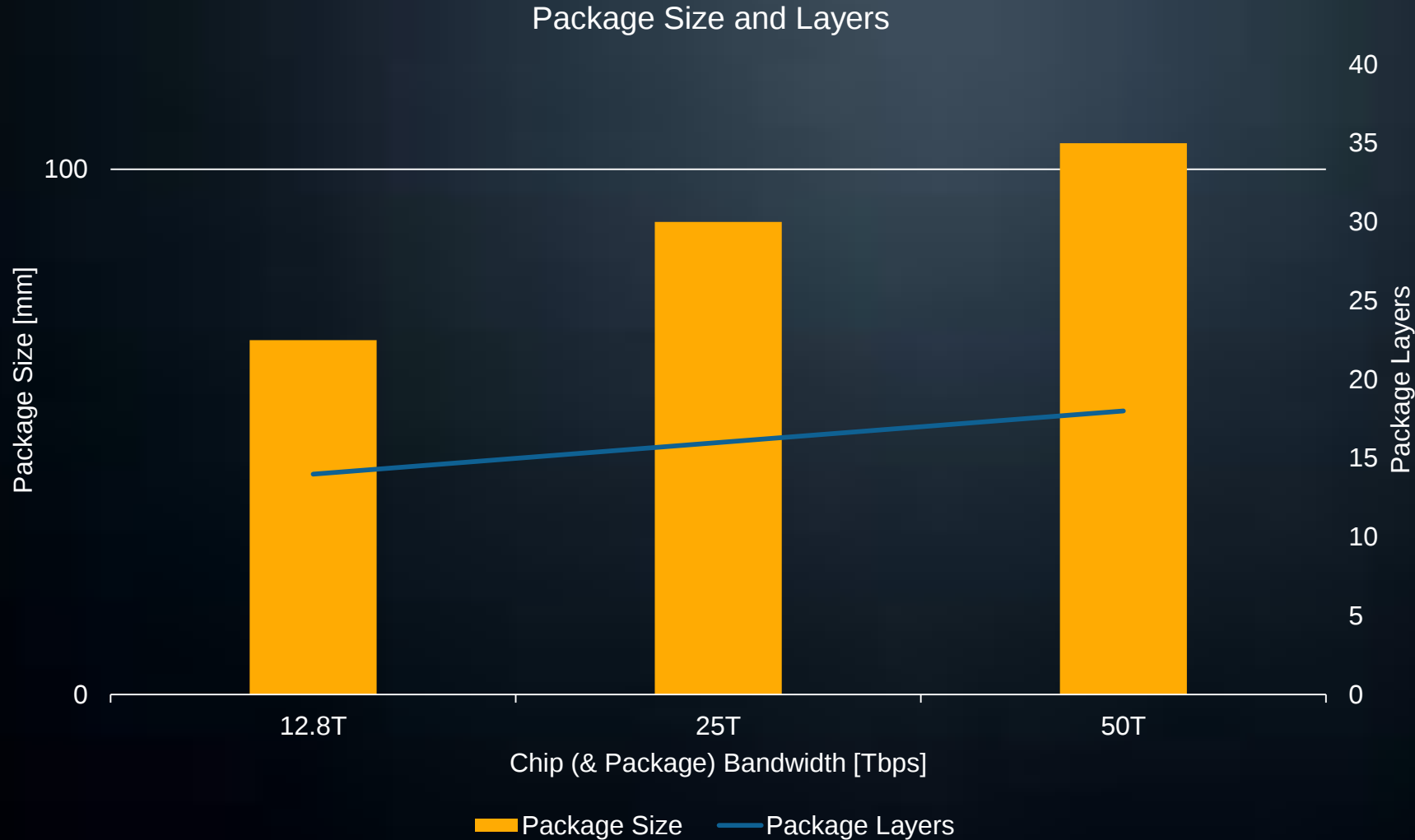


What happens at 112G?

- Insertion loss doubles (relative to 56G)
 - But Package IL Budget doesn't increase
 - Need 2x better package materials
- Signal Integrity drives extra BGA Isolation
 - BGA area needed for 4 lanes of SERDES
 - More SERDES lanes per Chip
 - → Package Size grows
- Many SERDES lanes → many wires
 - Drives more build-up layers



50T Switch – What kind of Package does it Need?



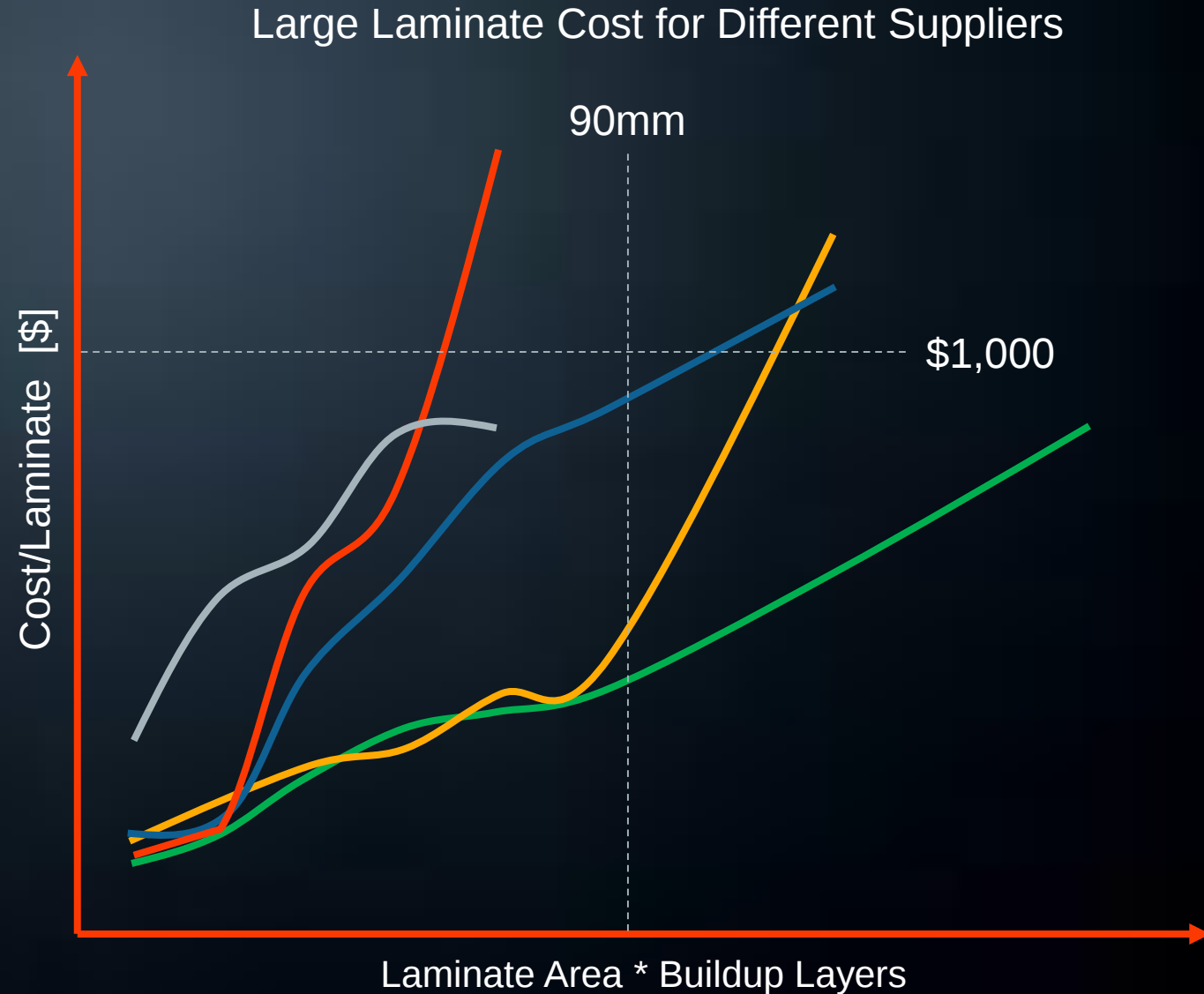
- Significant increase in package size and complexity

Large Laminate Cost

Large Laminates will be in products within the next 2 years, BUT:

- Cost is very inconsistent
- Cost is very high
- Not many suppliers supporting very large sizes

➔ Appears that laminate suppliers are hedging their bets

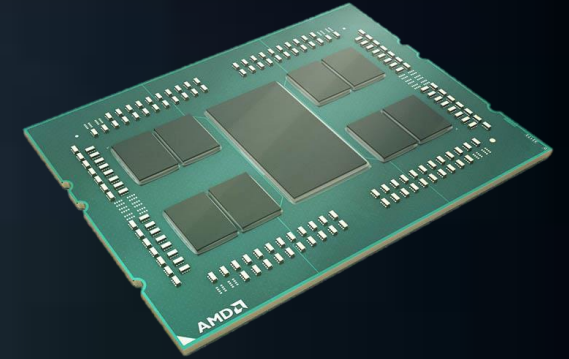


Get More Function out of the Package

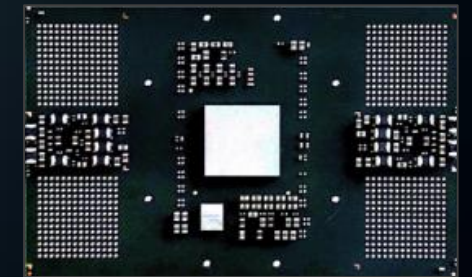
- Different functions don't always want to be on the same chip
 - IO Function
 - Schedule
 - Modularity
 - Analog and RF content
 - Technology fit
 - Modularity
 - DRAM
 - Technology fit
 - Cost



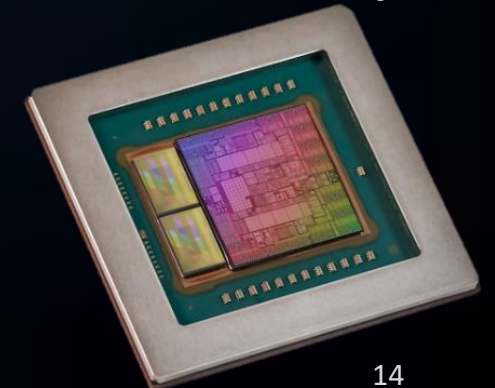
AMD Epyc 2 Rome



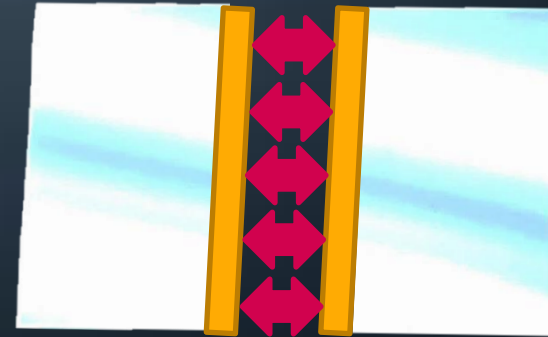
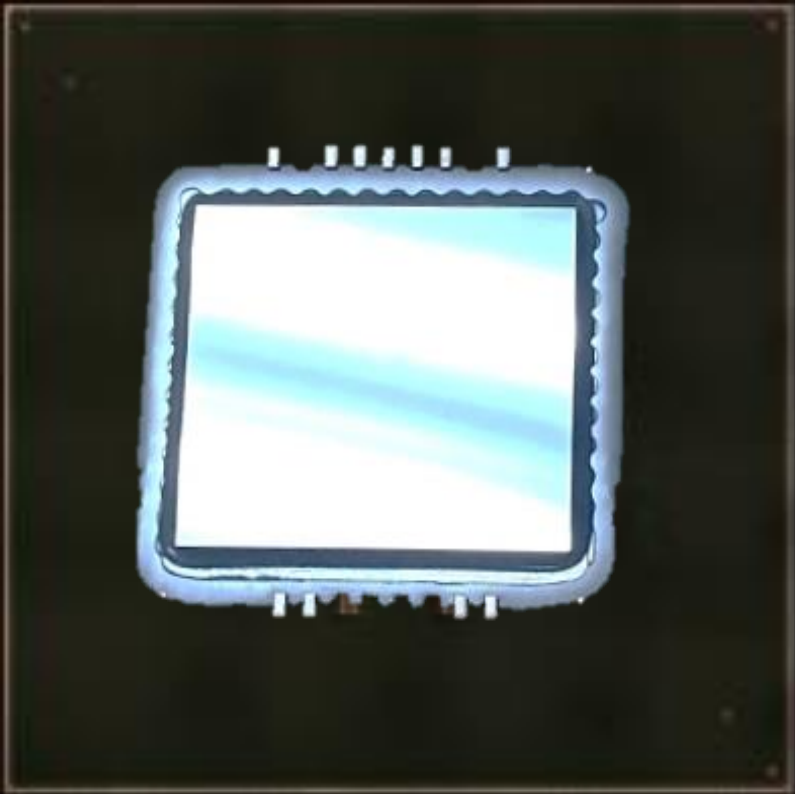
Data Converters



HBM Memory

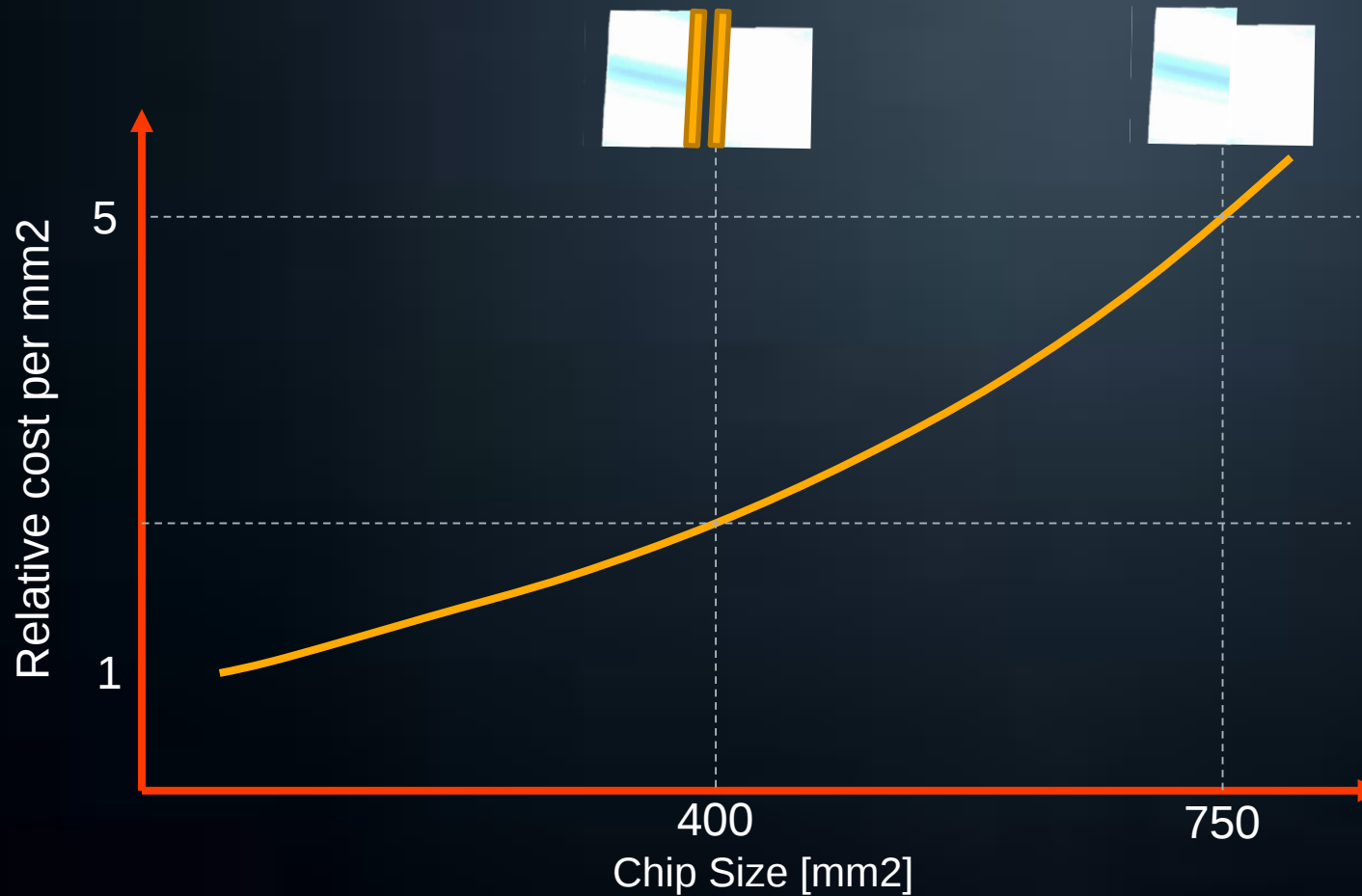


Get More Cost out of the Package



- Chip-to-Chip interface is required
- ➔ Chip partitioning actually increases the total Silicon Area

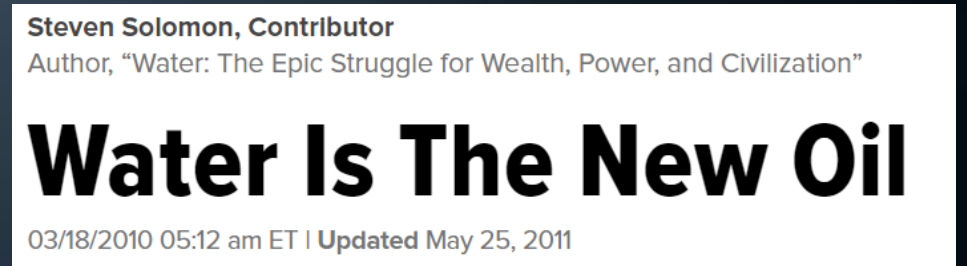
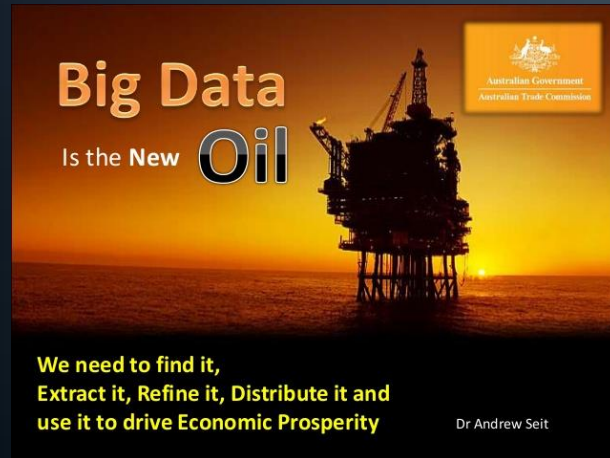
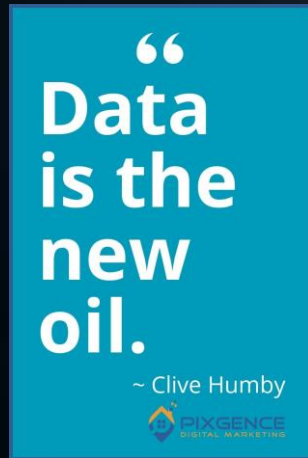
Cost of Yield Curve – Mathematical



- Large die yield poorly
 - → high cost per mm²
- Smaller die yield significantly better
 - → much lower cost per mm²

What about that Chip-to-Chip Interface

Let's try an analogy:



Data = New Oil

Water = New Oil

Data = Water

Some Water (or Coke) – i.e. Some Data



Small pipe works well

A lot of Water – i.e. A Lot of Data



Small pipes don't work so well

A much bigger pipe is needed for a lot of Data



- A huge amount of water/data typically requires a much bigger pipe

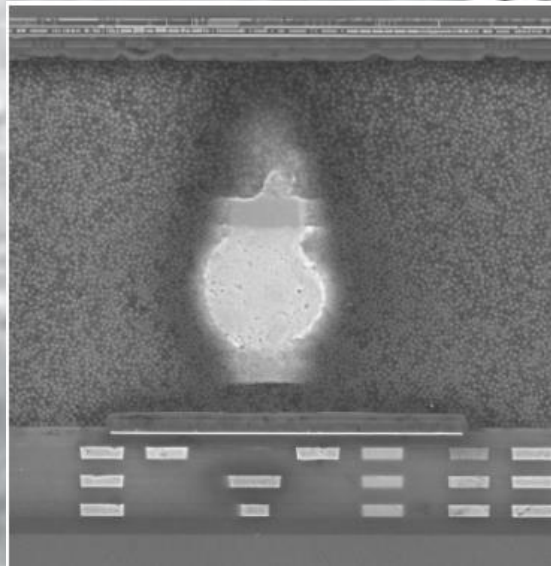
Chip-to-Chip Interfaces

- Several proposals exist for generic interfaces
 - Each of them have Pro's and Con's
 - It is unclear if the industry will corral behind just one of them

Interface	112G XSR	OCP "BoW"	Parallel, e.g. AIB
Analogy			
Signal Speed	112 Gbps	5 - 32 Gbps	2 - 5 Gbps
Standard	OIF	OCP (ODSA) Proposal	Open Standard (Intel)
Package Technology	Standard	Standard / Advanced	Very Advanced

Wiring Comparison

Silicon Interposer



Laminate



1x1

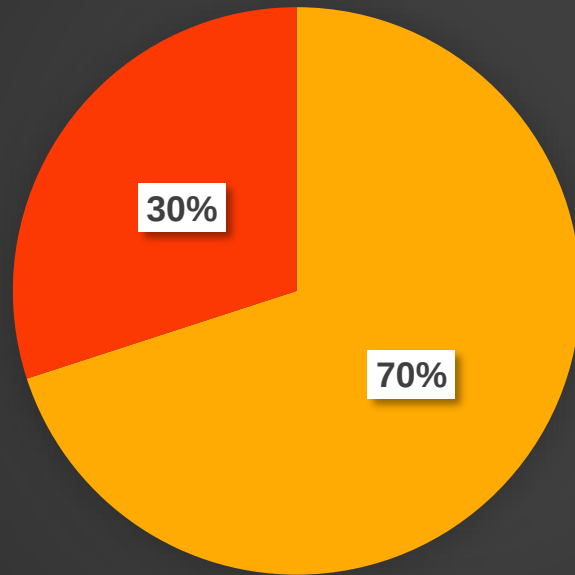
20 x 15

75um Human Hair (average)

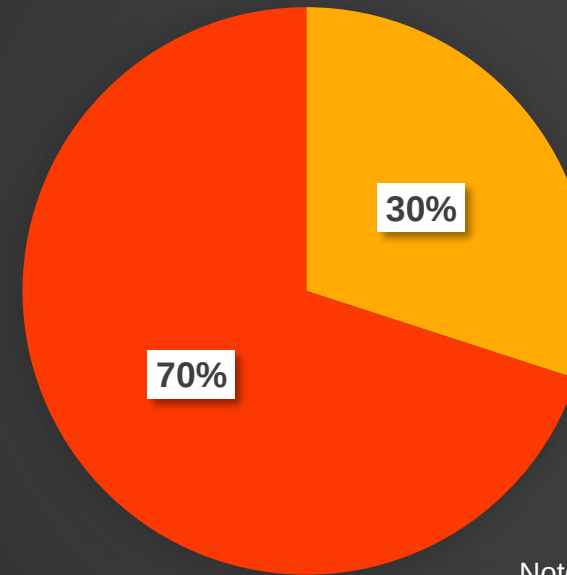
Cost-Evolution of Chip vs. Package



Traditional ASIC SCM



The New ASIC World



■ Chip Cost
■ Package Cost

Note: Extreme case, not average

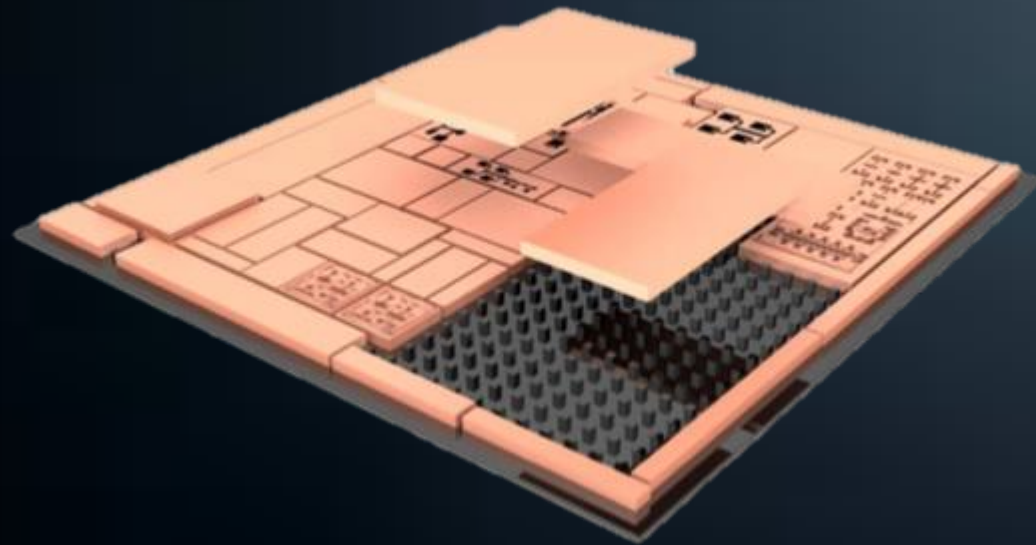
- Package cost on complex products can now far outweigh chip cost
- Interface definition is what drives one package technology (and cost) vs. another

Hard vs. Valuable

Value generally keeps increasing as things get harder



Standards, Chiplets, Open Access

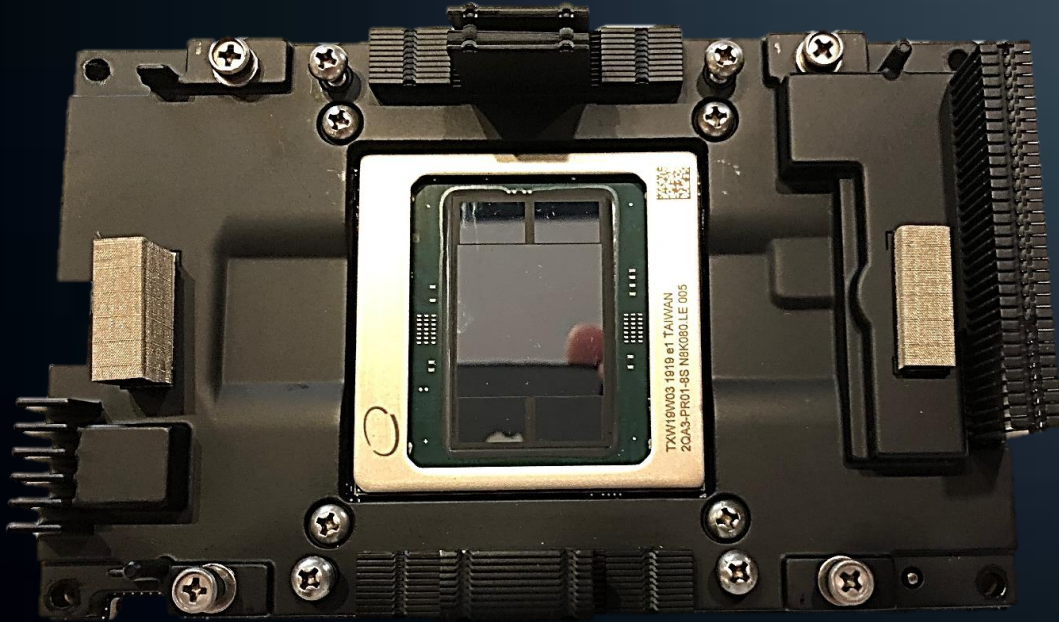


Semiengineering

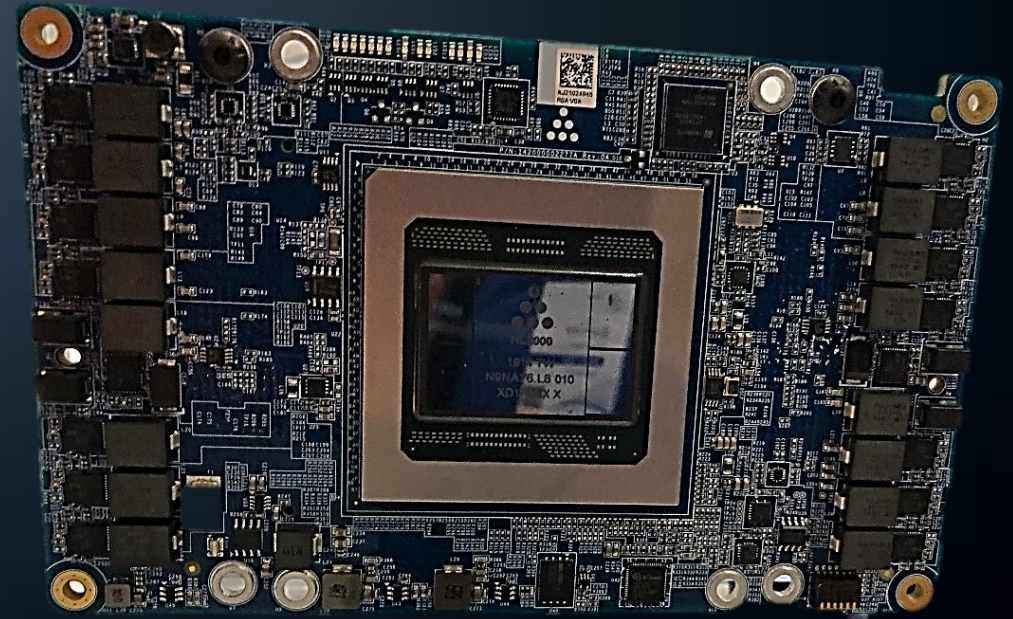
- Chiplets offer many significant advantages
 - Transition to chiplets has begun, and will continue to gain momentum
- But also harbor significant challenges
 - Drives new business models
 - Cost, yield and ownership considerations
 - Commodification of really “hard stuff”

OCP Open Accelerator Module

Intel “Nervana”
(TSMC based)



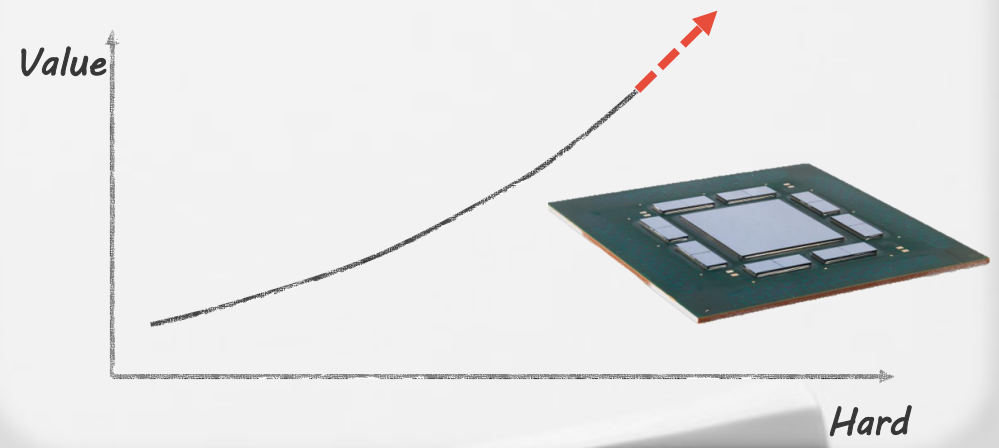
Pin-compatible Accelerator from
“Habana”



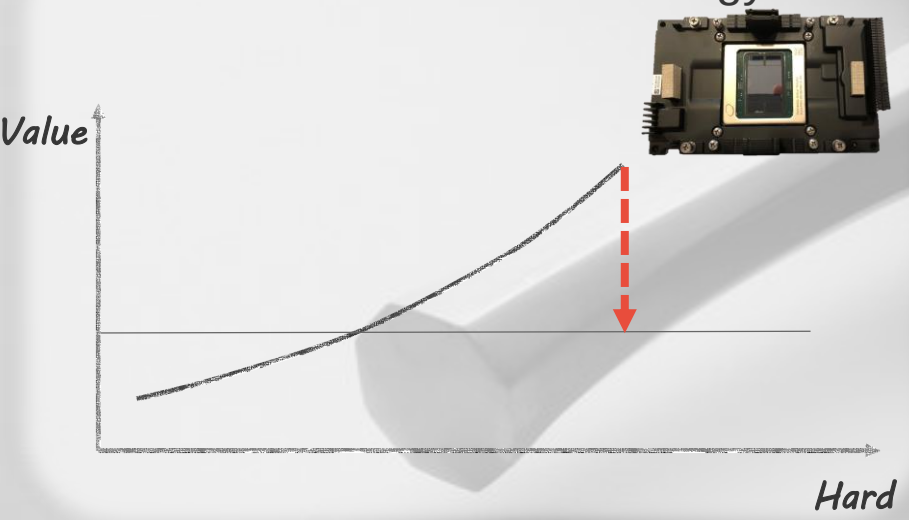
- AMD, Baidu, nVidia also providing compatible cards

The Double-Edged Sword of Standards

Technology Evolution & Revolution



Commodification of Technology



A typical Meeting Agenda in the Semiconductor World

Up to ~2017:

Agenda

- Chip Size
- Chip Performance
- Chip Color
- Chip Taste
- ...
- *(Packaging) - if time allows*

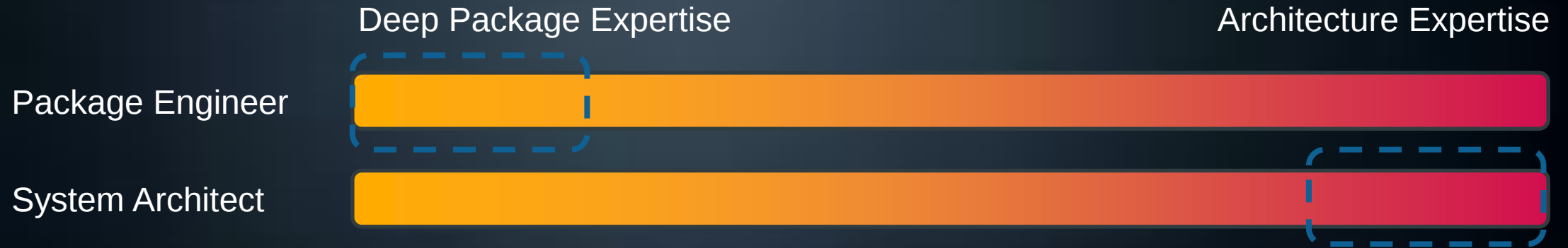
Now:

Agenda

- Chip Size
- Chip Performance
- *Packaging & Integration*
- Chip Color
- Chip Taste

The Sweet Spot for Integration

Status Quo

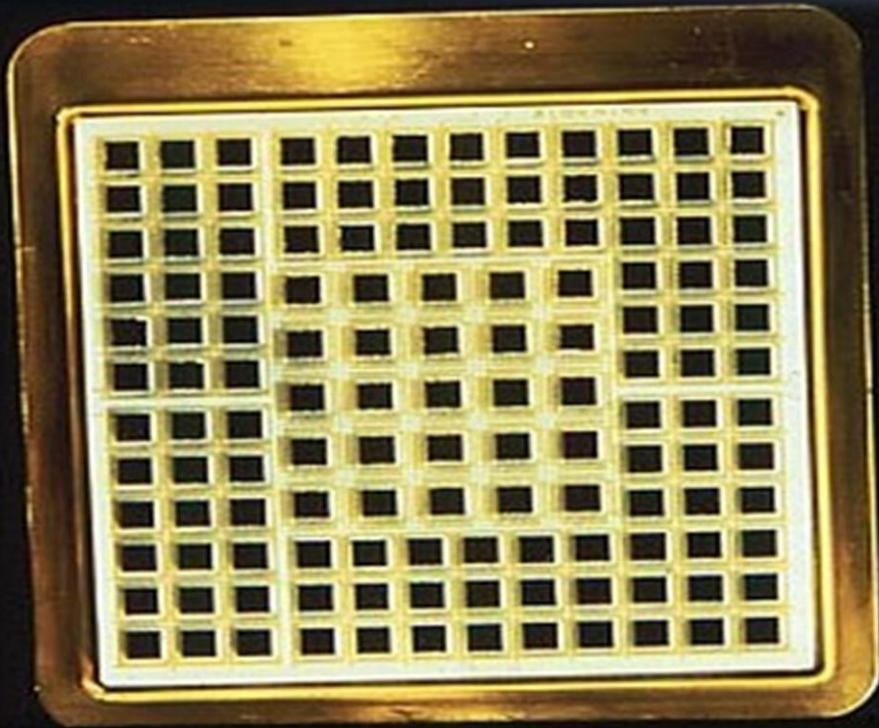


Sweet Spot



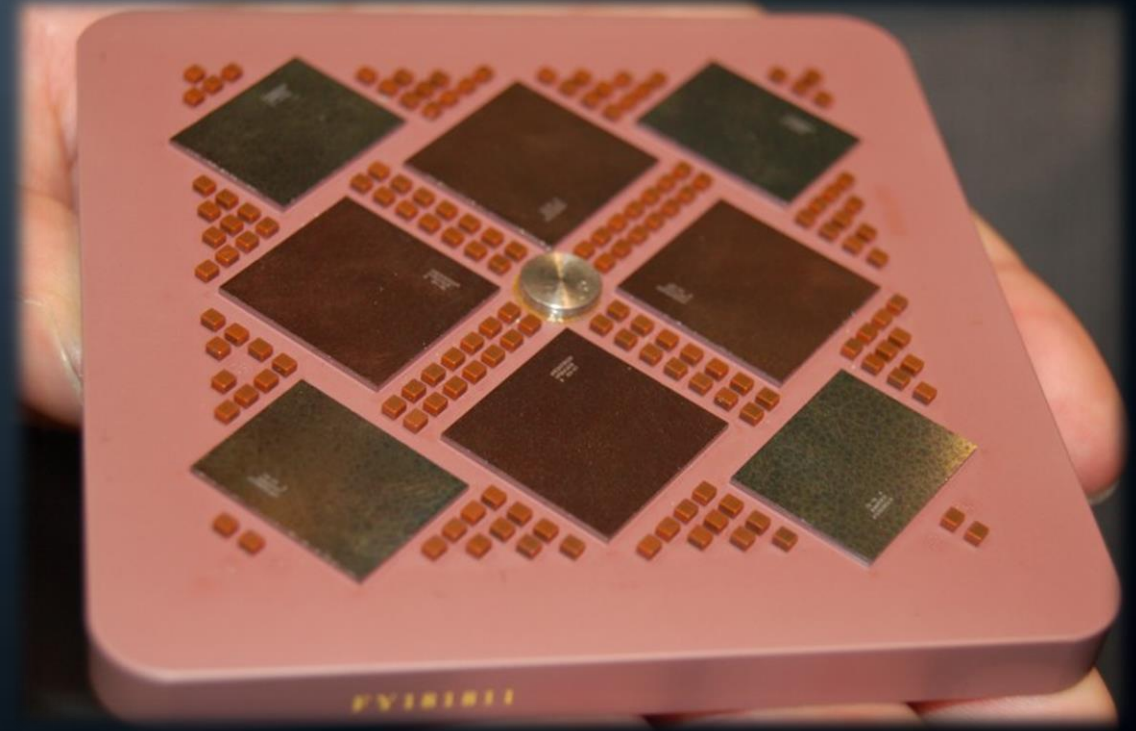
Is this new?

IBM 3081 Logic Module



Introduced in 1980

Google Search for “Multi-chip Module” (IBM Power 5)



Launched in 2004

Call to Action

- What does Packaging have to Deliver?
 - Do all the things the chip can't
 - Talk to the outside world
 - Integrate content that doesn't want to be on one piece of Silicon
- What do we (as Packaging Engineers) have to become Experts in?
 - Understand what products need
 - Translate what products need into package technology requirements
 - Execute Development and Know the Trade-offs

M A R V E L L[®]