Integrated Packaging Technologies for High-Performance Computing Systems: Challenges and Opportunities

Max Min

Package and SI/PI Architect

March 5, 2020

IMAPS Keynote, Samsung Foundry

SAMSUNG

Contents

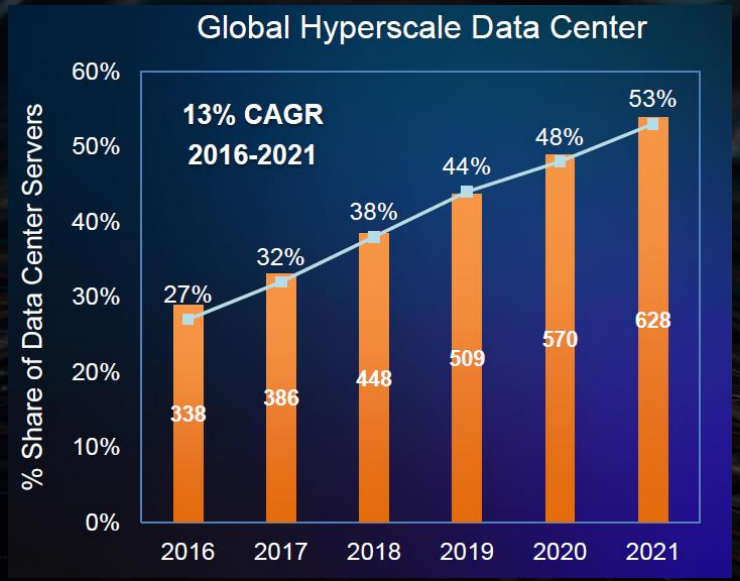
- Big Data
- Toward “Beyond Moore’s Law”
  - Handy Memories
  - Nearby Decaps
  - Challenges
- Summary

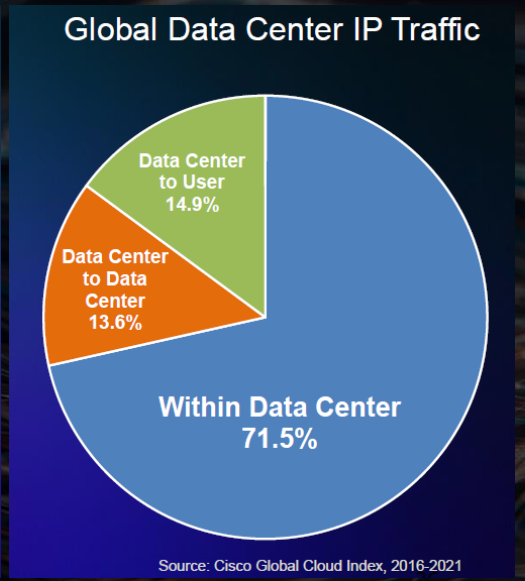
SAMSUNG

Increasing Demands on the Clouds

Regional data centers and content delivery networks, both of which brought internet infrastructure closer to the users.

Deploying infrastructure needs to **go beyond regional deployment and operation**, and also be deployed more locally.





SAMSUNG

Q: Big Data! What we need?

A: Technologies for big data **processing**!

Let machine  do the work with **AI**!

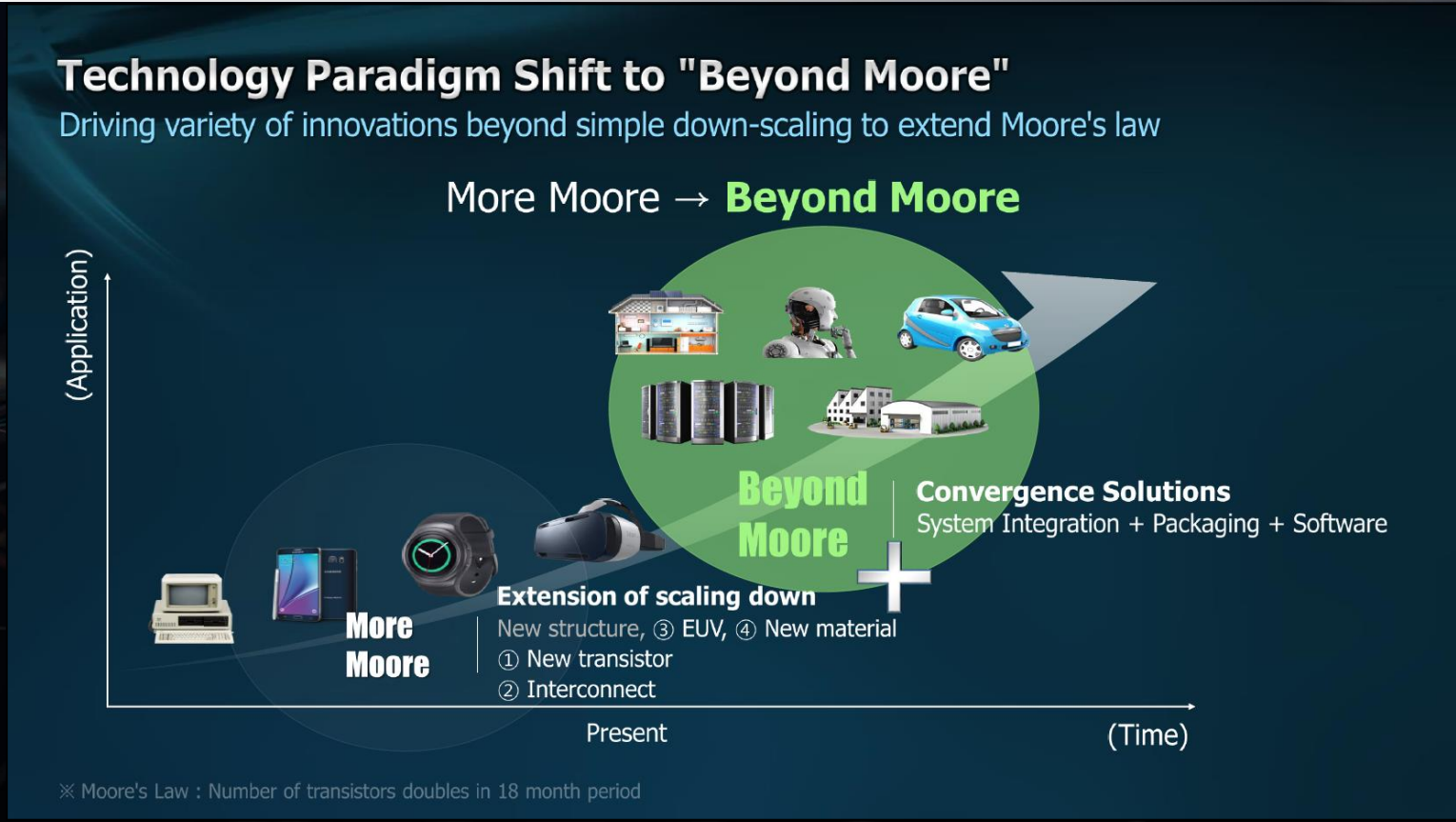
Kakao Talk (messenger) "Busy" Emoticon

SAMSUNG

- Toward “Beyond Moore’s Law”

SAMSUNG

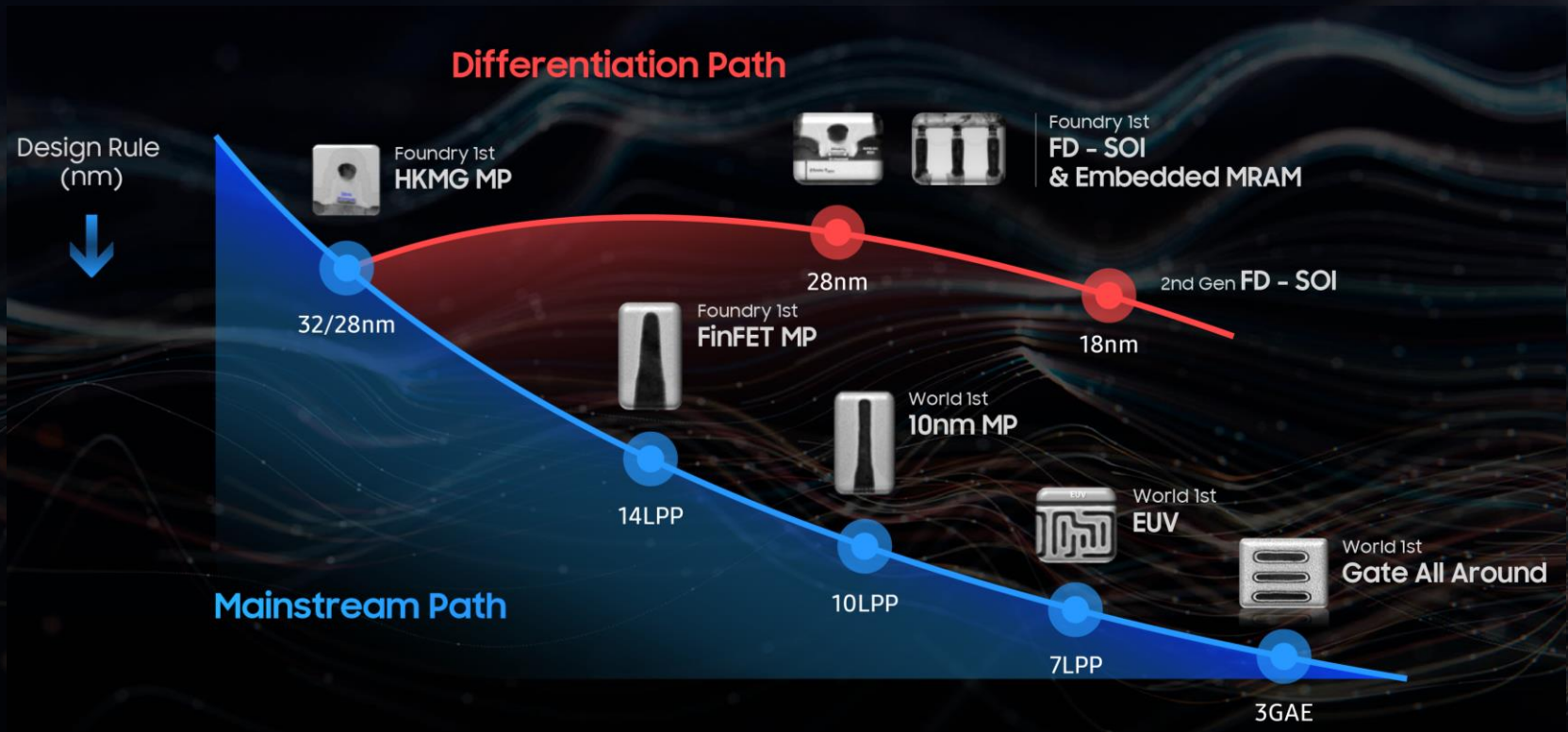
"Beyond Moore's Law"



Source: 2018 IEDM Keynote presented by ES Jung (President of Samsung Foundry)

SAMSUNG

Silicon Technologies for More Moore

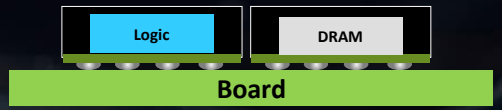


Samsung Foundry, Long History of Proven Silicon Technology

SAMSUNG

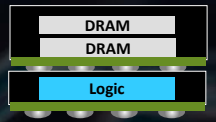
- Toward “Beyond Moore’s Law”
  - Handy memories by Advanced Package Solutions

Handy Memories on X



DDR

On board

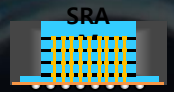


LPDDR

On package

HBM

On interposer



SRAM

On silicon

Mobile — PoP/SIP/Fanout Technologies

HPC/AI — 2.5D/3D/Chiplet Technologies

Memory integration near the logic innovates the packaging technology

SAMSUNG

System Memory Bandwidth Trend

Mobile BW

25 GB/s → 30 GB/s → 35 GB/s → 45 GB/s

LPDDR

Smart Phone

100 GB/s → 100+ GB/s

Edge Computing

HPC/AI BW

384 GB/s → 432 GB/s → 672 GB/s → 768 GB/s

HBM (3D)

1 TB/s → >2 TB/s

AI Training

DDR

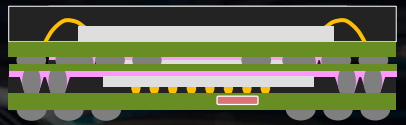
AI Inference

Memory bandwidth drives package platforms

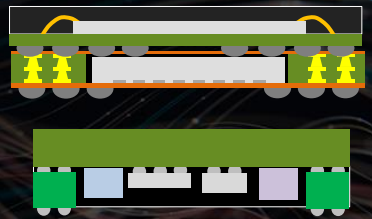
SAMSUNG

PoP/Fanout/SiP Packages : LPDDR

PoP ※ Package on Package
<50GB/s (x64)



FO-PoP ※ FanOut-PoP
100GB/s (x128)



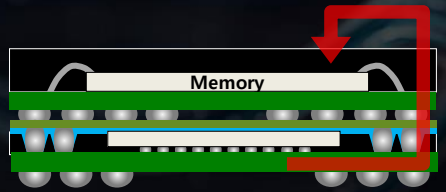
5G Module (Antenna in Package)

FO-SiP ※ FanOut-SiP
>200GB/s (x256)

SAMSUNG

FO-SiP with Extreme Bandwidth

PoP



VS

FO-SiP

Thickness
Up to
↓ 40%
vs PoP

Thermal Resistance
Up to
↓ 40%
vs PoP

Eye Opening
(@8Gbps)
Up to
↑ 400%
vs PoP

Memory Bandwidth
Up to
↑ 400%
vs PoP

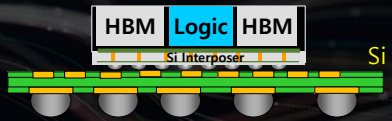
Ultimate performance, but area penalty and new memory requirement

SAMSUNG

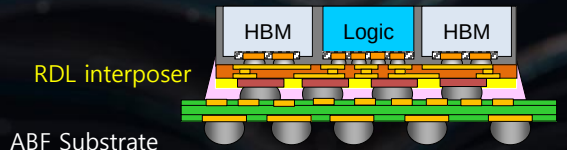
2.5D Packages : HBM

I-Cube

High Performance



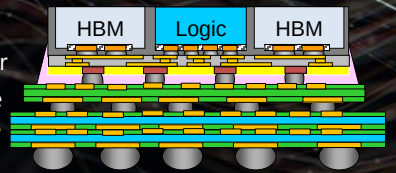
Si interposer
ABF Substrate



RDL interposer
ABF Substrate

R-Cube

+ Cost Effective



Interposer
ABF Substrate
HDI Substrate

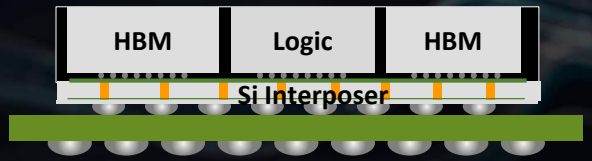
H-Cube

+ Cost Effective

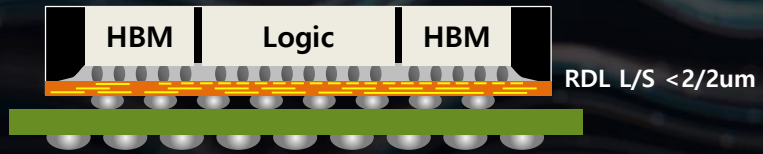
SAMSUNG

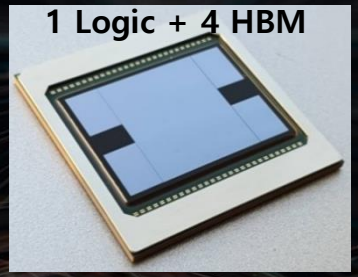
2.5D I-Cube and R-Cube

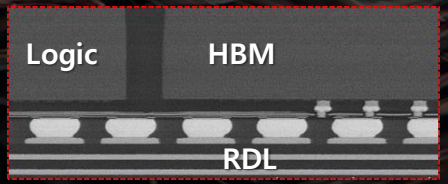
2.5D I-Cube

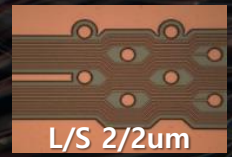


2.5D R-Cube





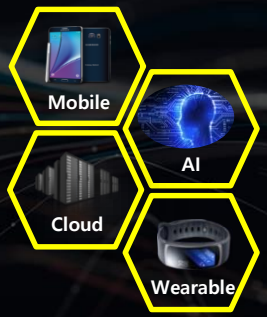




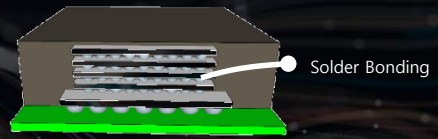
8HBM can be integrated into a 85x85mm2 MIoS package

SAMSUNG

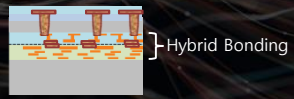
3D Packages



CoW (Chip on Wafer)



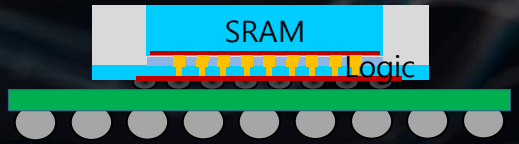
W2W (Wafer to Wafer)



D2W (Die to Wafer)

SAMSUNG

3D SRAM Package Qualified

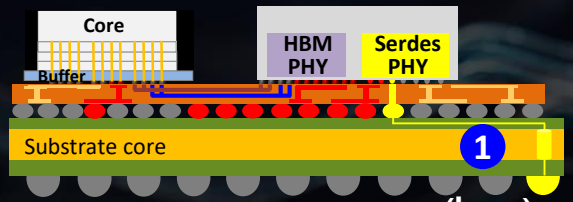


Test item		Conditions	Result
Pre-con		MSL3, 192h	Pass
	TC(B)	-55~125℃, 300cyc	Pass
		-55~125℃, 700cyc	Pass
		-55~125℃, 1kcyc	Pass
	uHAST	130℃/85%RH, 96h	Pass
		130℃/85%RH, 168h	Pass
HTS		Ta = 150℃, 500h	Pass
		Ta = 150℃, 1000h	Pass

3D SRAM package was qualified

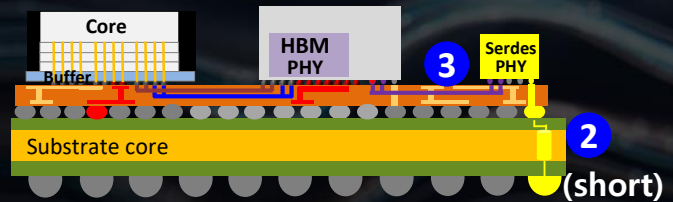
SAMSUNG

Chiplet Packages

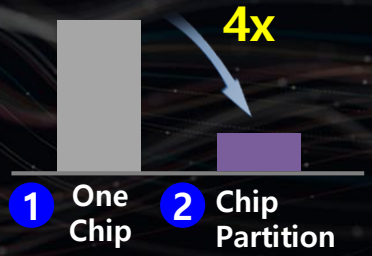


Single Logic Chip

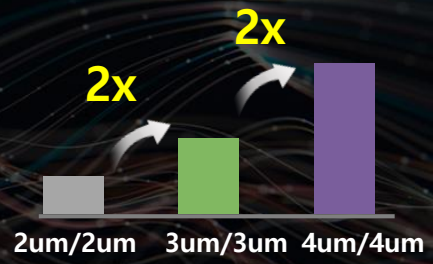
VS



Logic Chip Partitioning



Signal loss



3 Allowable Max Speed

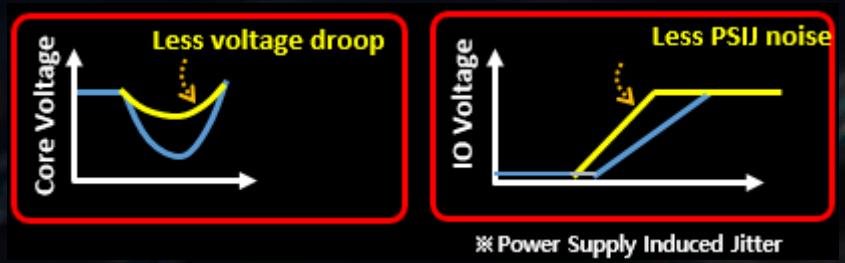
Serdes chiplet allows shorter signal length

SAMSUNG

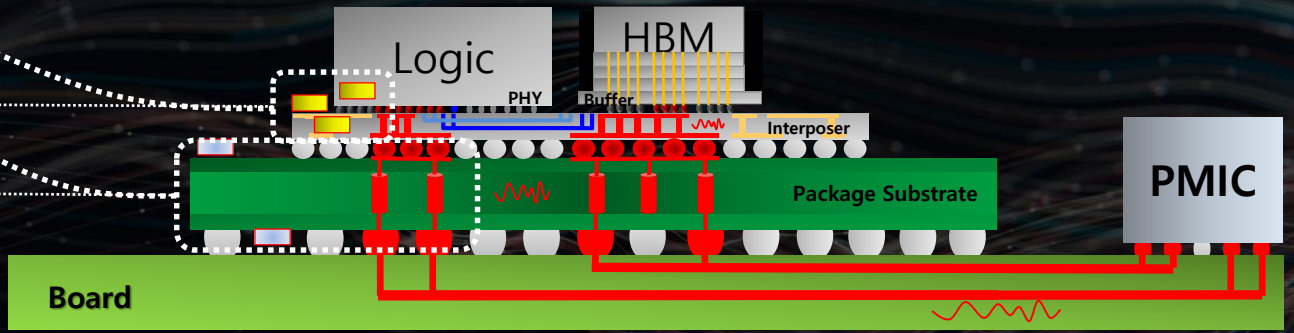
- Toward “Beyond Moore’s Law”
  - Nearby Decaps by Advanced Decoupling Capacitors

SAMSUNG

Nearby Decaps on X



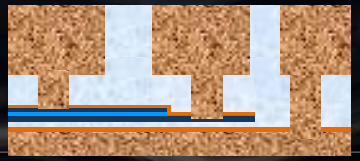
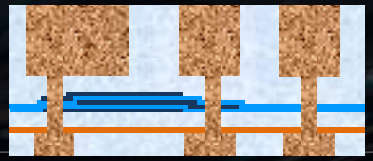
- **MIM** (Metal Insulator Metal)
- **ISC** (Integrated Stacked Capacitor)
- **EPS** (Embedded Passive Substrate)

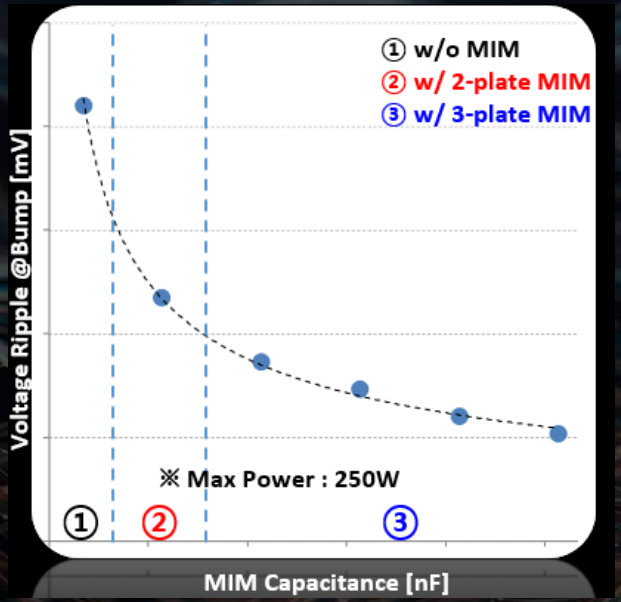


Decoupling capacitor integration near the transistor reduces the noise

SAMSUNG

MIM (Metal Insulator Metal)

	2-plate MIM	3-plate MIM
Structure (Concept)		
MIM Capacitance	20nF/mm^2	40nF/mm^2
Position	On-chip & Si-interposer	On-chip & Si-interposer

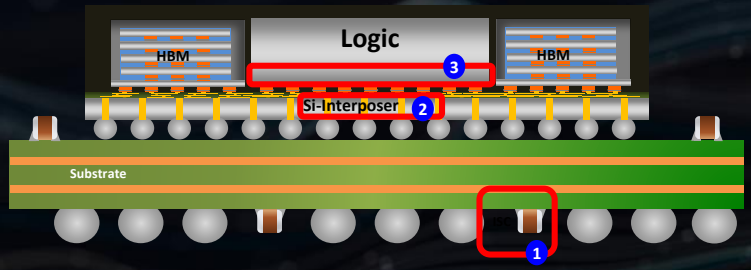


MIM provides high-frequency electrons

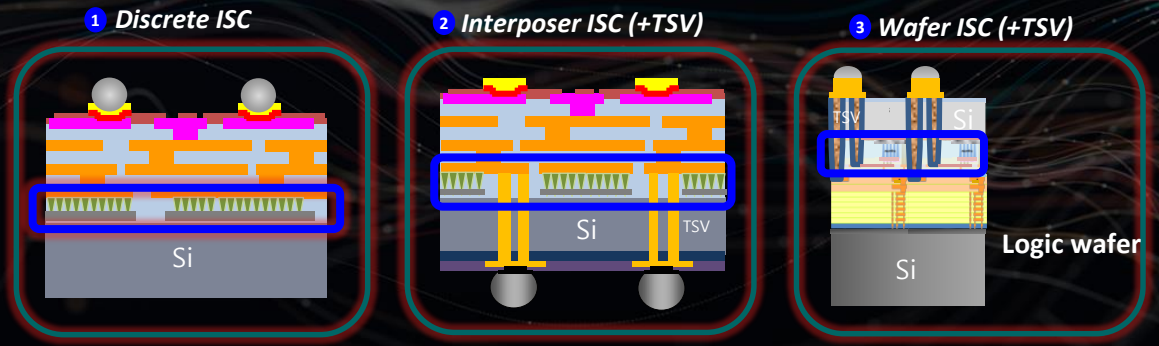
SAMSUNG

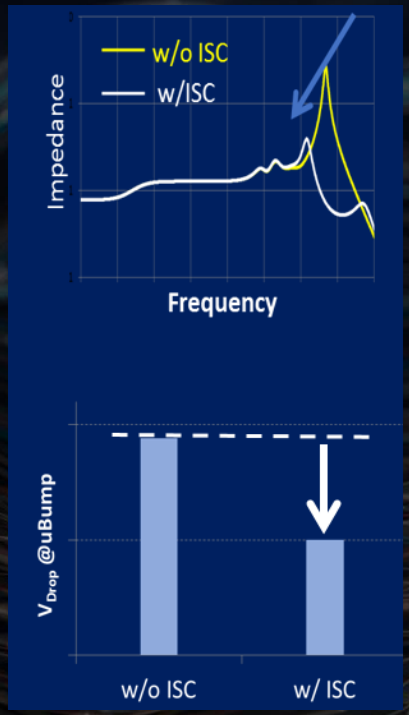
ISC (Integrated Stacked Capacitor)

- Thin, light and high capacitance (300nF/mm2)



- 3 ISC types

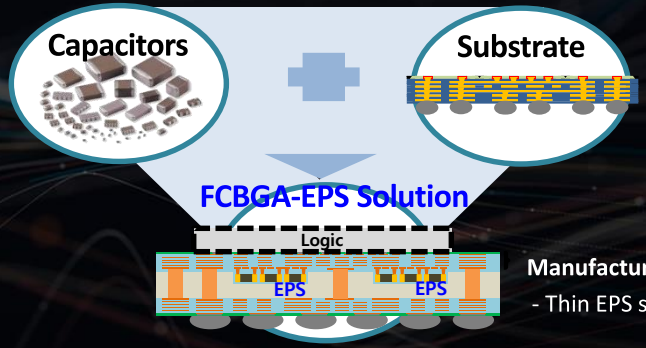




ISC provides mid/high-frequency electrons

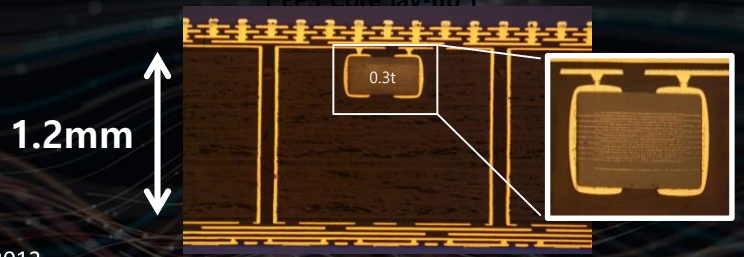
SAMSUNG

EPS (Embedded Passive Substrate)



Manufacturability

- Thin EPS shipped since 2012



- + ISC
- + R/L/C
- + Bridge
- + PMIC

EPS provides mid/low-frequency electrons

SAMSUNG

- Toward “Beyond Moore’s Law”
  - Challenges : Electrical, Thermal, Mechanical

SAMSUNG

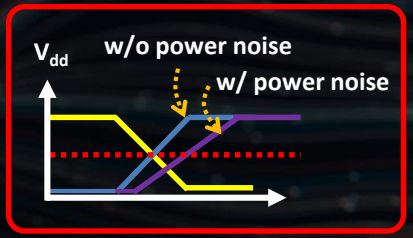
Electrical Challenges

1 IR Drop

2 Crosstalk Noise

3 Signal Degradation

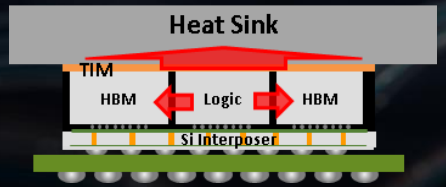
4 Power Supply Induced Voltage Noise (PSIJ)

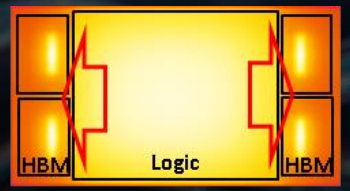


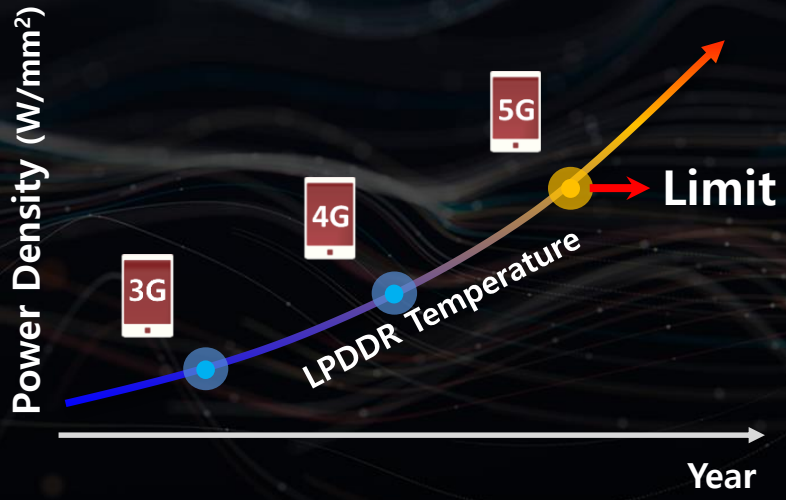
Early SI/PI feasibility, SI/PI-aware signoff & Function validation

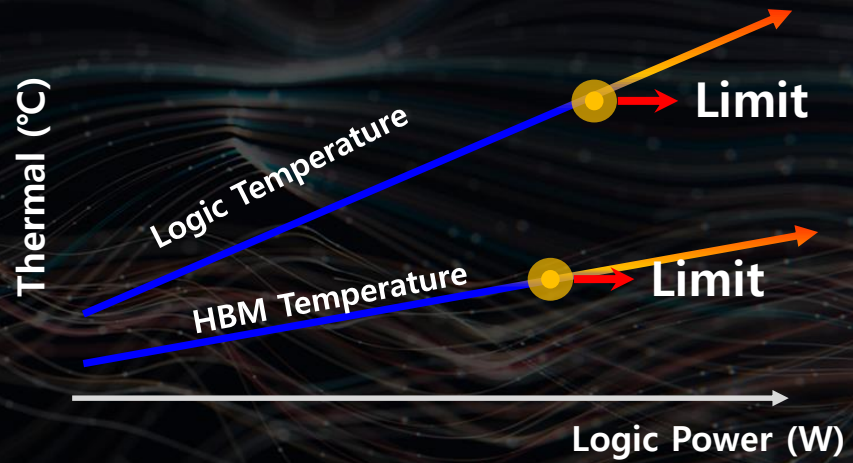
SAMSUNG

Thermal Challenges





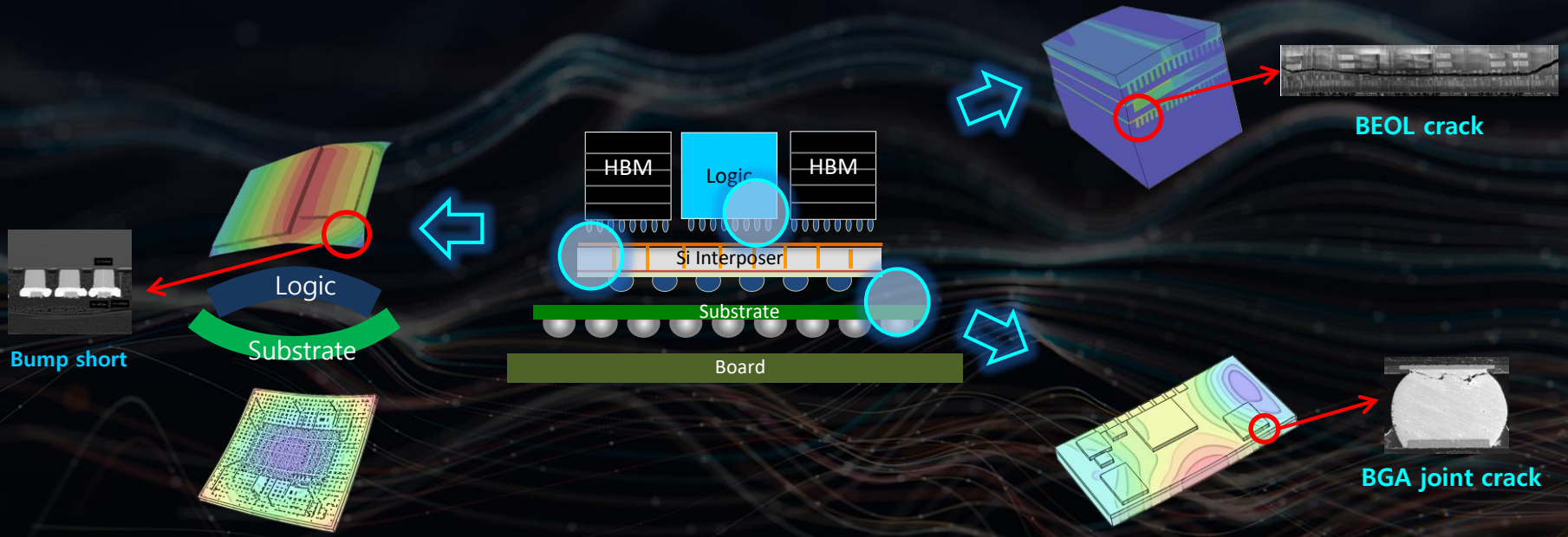




Early thermal feasibility & TTV validation

SAMSUNG

Mechanical Challenges



Early mechanical feasibility & MTV, CPI, BLR validation

SAMSUNG

Summary

For Big Data Era, the HPC/AI system needs

- Handy Memories by Advanced Package Solutions
- Nearby Decaps by Advanced Decoupling Capacitors
- Early SI/PI/Thermal/Mechanical Feasibility & Validation