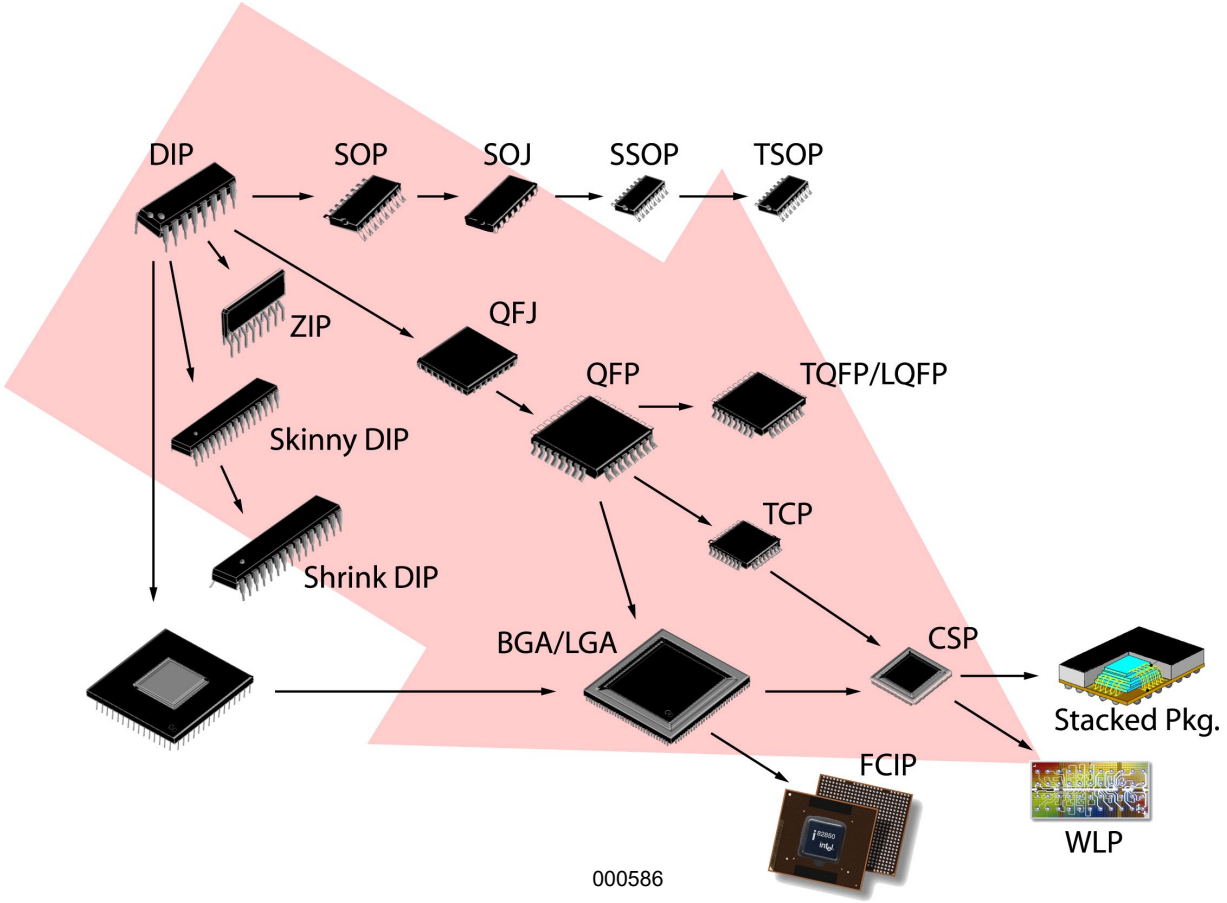
Interconnect Transitions and the Challenges Ahead

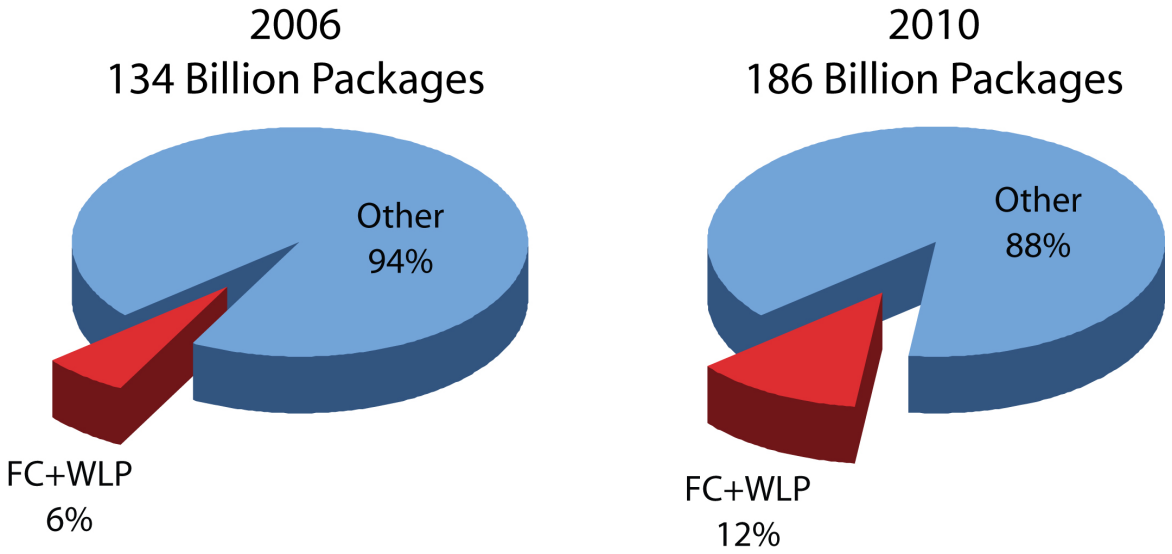
E. Jan Vardaman, President and Founder

TechSearch INTERNATIONAL

Industry Has Seen Many Changes in Packaging and Assembly



Wire Bond Still Accounts for Most of IC Package Interconnect
Advanced Packaging (FC & WLP) Show Higher Growth



Source: IC Insights and TechSearch International, Inc.

- **Wire bond remains the work horse**
  - Established infrastructure
  - Lower relative cost with proven reliability

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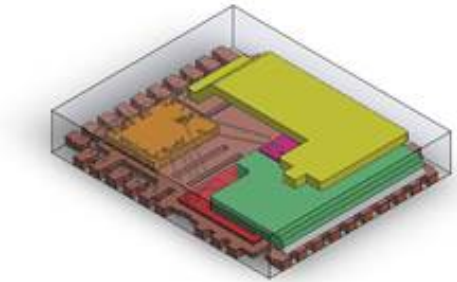
Cu Clip Packages

- **Advantages of Cu Clip include**
  - Lower resistance and lower inductance (clip instead of wires)
  - Higher current carrying capabilities
  - Provides increased power density and efficiency at higher switching frequencies
  - Improved thermal management
- **Applications**
  - PCs
  - Servers in data centers
  - Automotive especially electric cars
- **QFN/DFN format increasing popular, but also TO, SO, LGA/BGA**
  - Driver + 2 FETs referred to as DrMOS
  - Side-by-side or stacked
- **Materials and OSATs key to expansion**
  - Customization and dedicated production lines

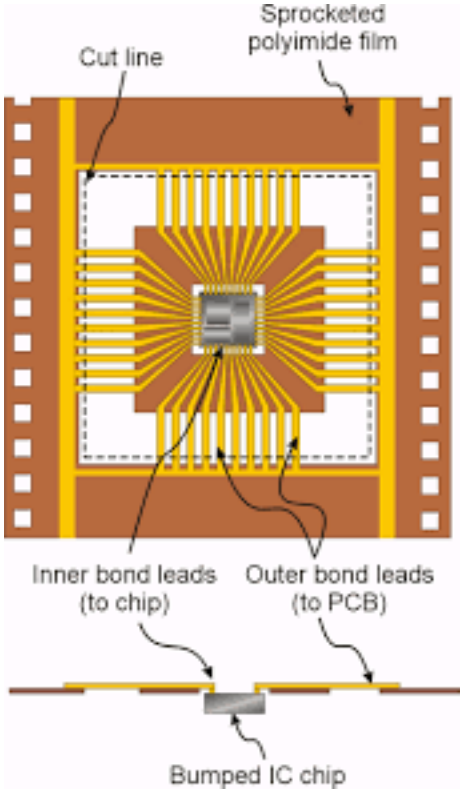
Cu Clip QFN
Module 2 FET + Clip + Controller



Source: UTAC.

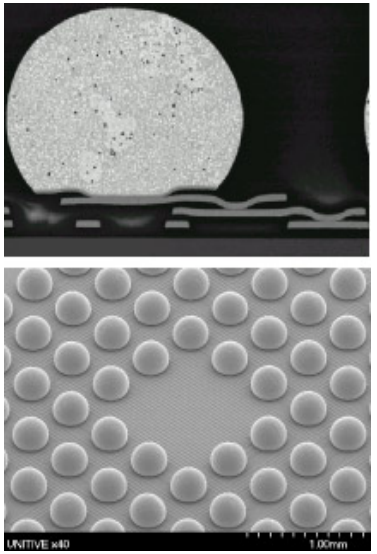
Tape Automated Bonding

- **Tape automated bonding (TAB)**
  - Gold bump
  - Flex circuit (TAB tape)
  - Replaced by lower cost laminate substrates for IC packages
  - Infrastructure for TAB was not well-established
- **Chip-on-Film (COF) and Chip-on-Glass (COG)**
  - Lots of driver ICs still using
  - Gold bump



History of Flip Chip Adoption

- **Early IBM bump was Cu ball introduced in 1960s by IBM**
- **Same era as Cu post with solder**
  - Citizen Watch
  - Automotive electronics at Delphi and Denso
- **Mainstream adoption, outside of captive options required:**
  - Industry infrastructure development
  - Introduction of a high-volume application to provide economies of scale to lower the cost of the technology
- **Barriers to adoption in early days**
- **Widespread adoption of FC driven by**
  - Substantial improvements in industry infrastructure and process maturity
  - Availability of EDA tools and the ability to design area-array instead of peripheral layout to take full advantage of the technology
  - LSI Logic's assembly technology transfer to OSATs
  - Couple with volumes driven by Intel's adoption of flip chip on laminate substrates

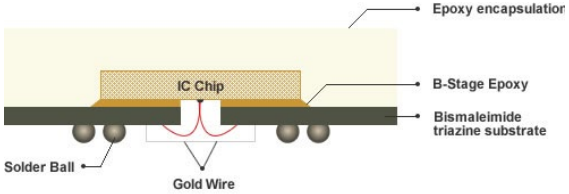


Source: Amkor.

Shift in Memory Packaging and Interconnect Changes

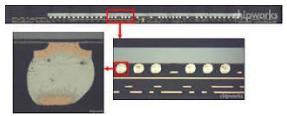
TSOP

FBGA



Structure of FBGA

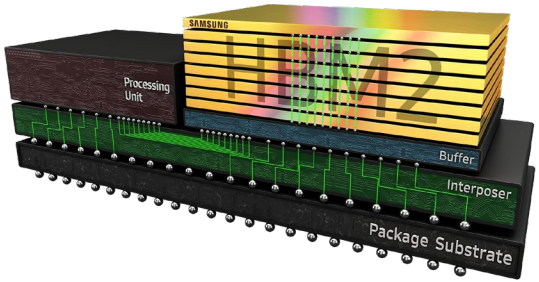
Wire Bond



Flip Chip

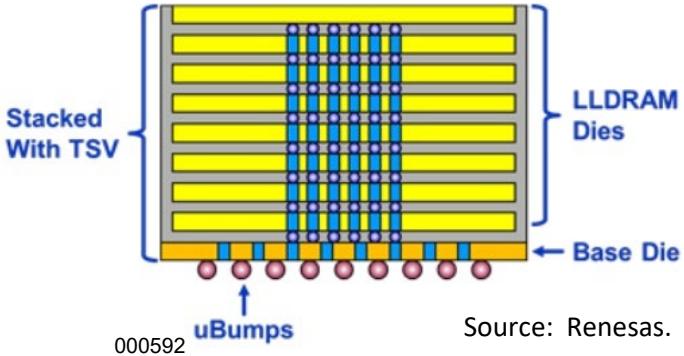
High Bandwidth Memory

- **Advantages**
  - Higher bandwidth
  - Lower latency
  - Lower power consumption
- **Micro bumps used to connect die**
- **Suppliers**
  - Samsung (HBM)
  - SK Hynix (HBM)
  - Micron (future HBM)
  - Renesas (Low-latency HBM)



Source: Samsung.

Source: Chipworks.



Source: Renesas.

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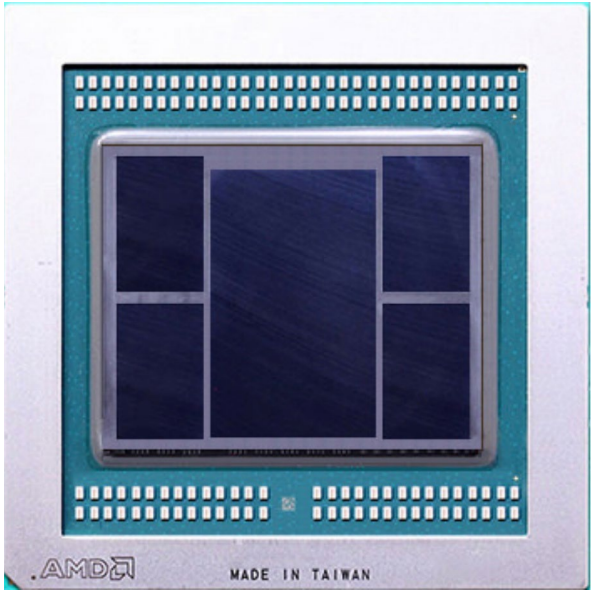
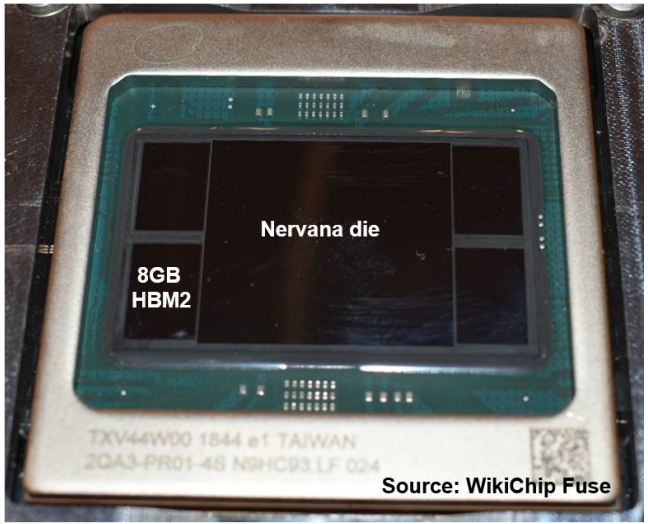
Many Examples of HBM on Si Interposers

AMD's Vega 20



Source: AMD.

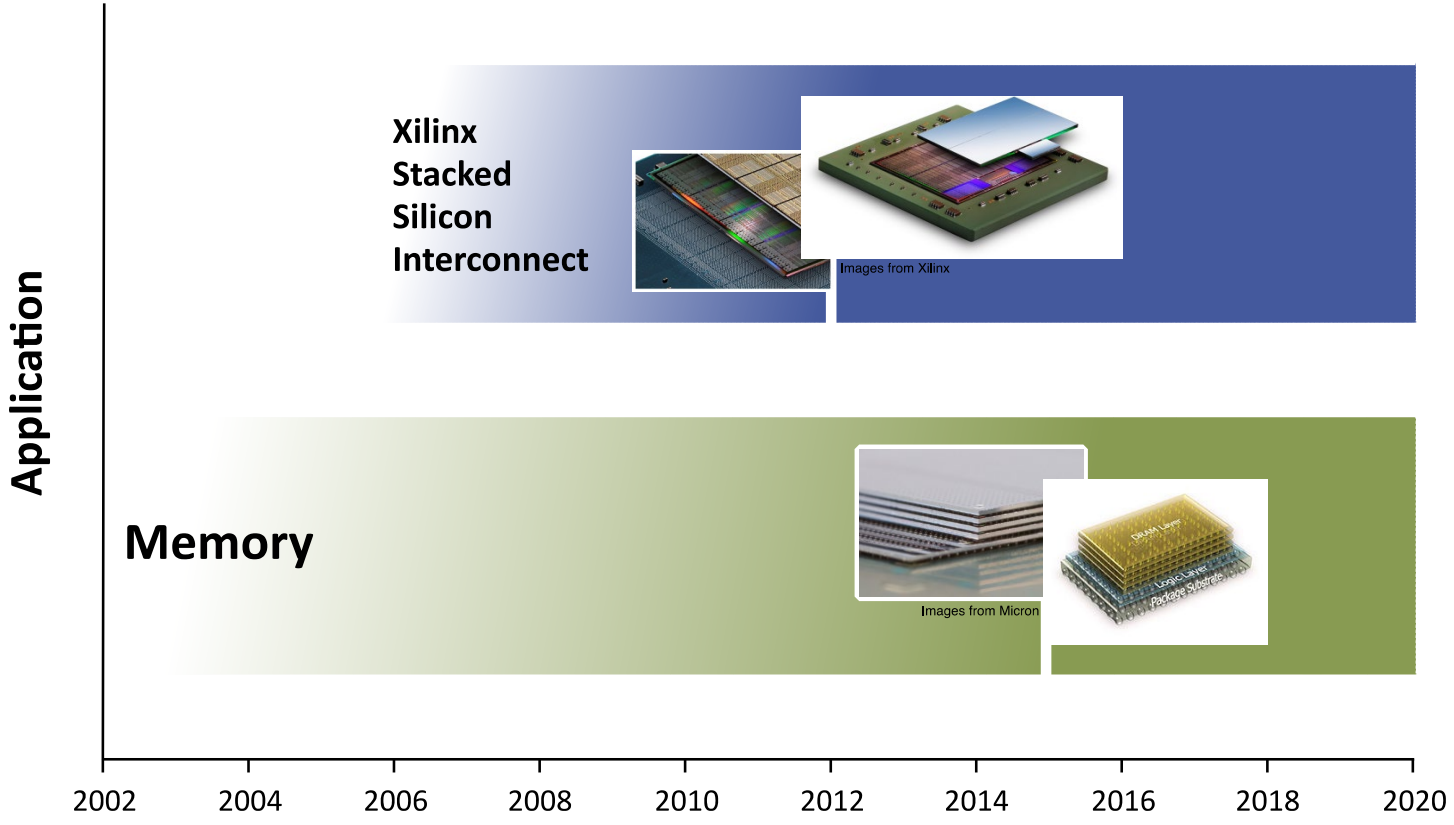
Intel Spring Crest



Huawei Ascend 910

Source: Huawei

Packaging Changes Take A Long Time!



Source: TechSearch International, Inc.

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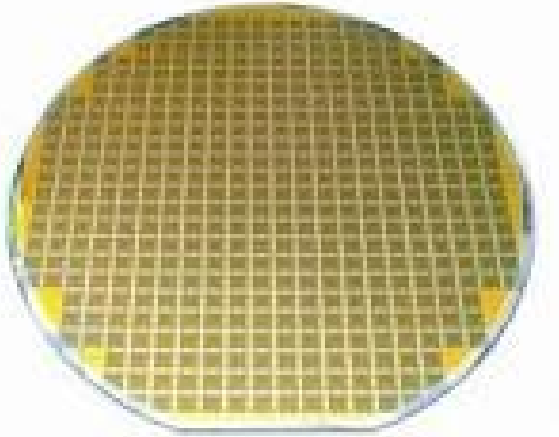
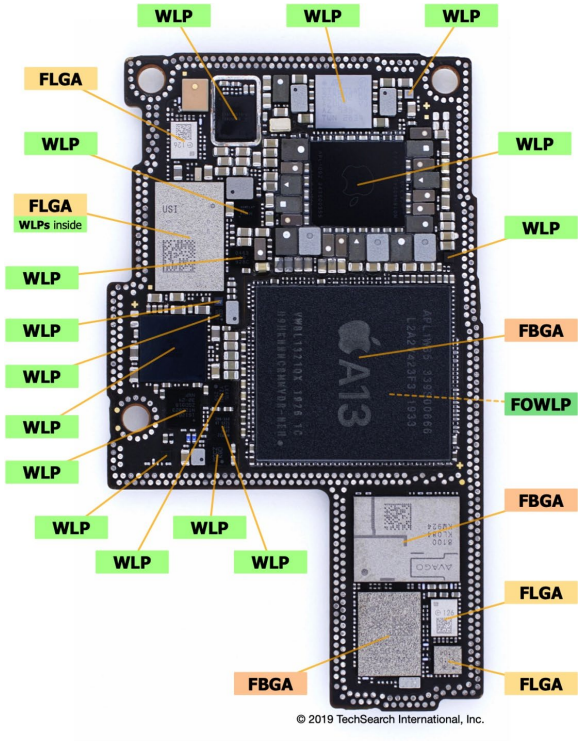
New Age: Increased Processing at the Wafer Level

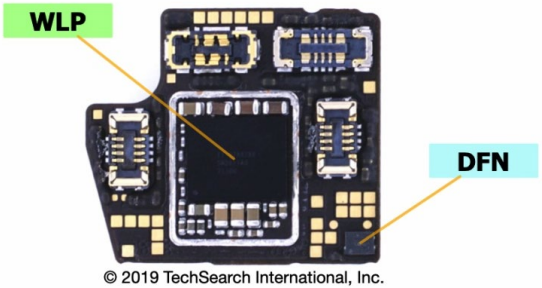
- **Driven by miniaturization demands**
- **Traditional process wafer is processed and sent to assembly facility for singulation, assembly, and test**
- **Tape and reel required to transport device to EMS for board level assembly**
- **New model for packaging**
  - Some wafers stay at the foundry for packaging and assembly
  - Some OSATs install wafer processing equipment to create package on the wafer

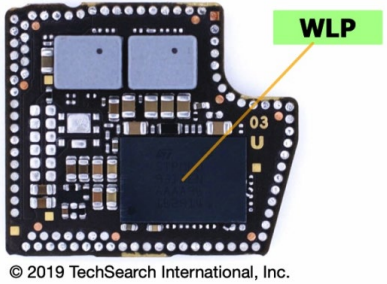


Fan-in WLPs: Driven by Smartphones to be Major Package

- **First iPhone, introduced in 2007 contained 2 fan-in WLPs**
- **The iPhone 11 Pro Max, introduced in 2019 contains 74 fan-in WLPs**
  - Includes lightning cable, earbud, and boards
  - Includes small capacitors and diodes
  - Plus one Fan-out WLP







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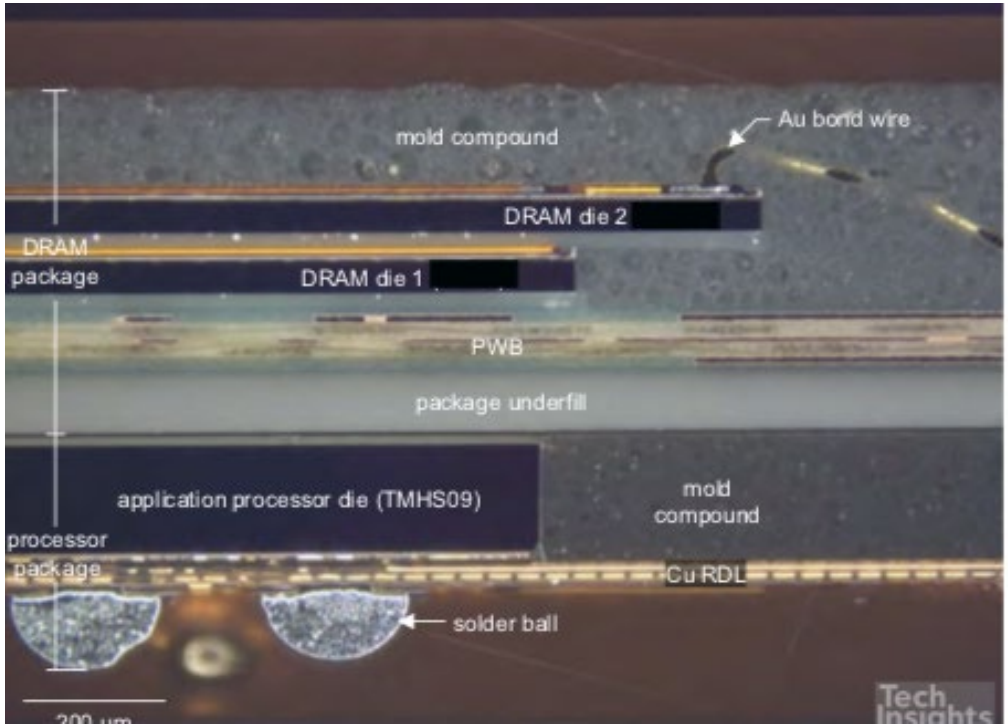
Fan-Out WLP: A Disruptive Packaging Technology

- **No substrate**
  - Thin-film metallization used for substrate (can go below 5µm L/S)
  - No traditional laminate substrate (most application processors had been using laminate substrate with flip chip bump interconnect)
  - No traditional underfill
  - Removes substrate supplier as design partner
- **Infrastructure changes**
  - All packaging can take place at the foundry
  - Assembly can also take place at OSAT but uses a non-traditional OSAT assembly line
  - Requires IC/package co-design



Courtesy of TechInsights.

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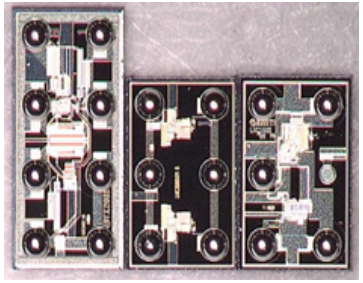
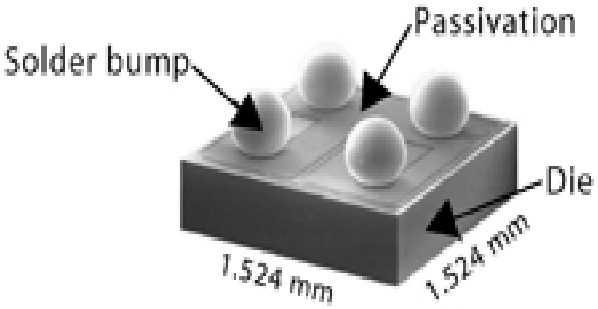
What Was Required for WLP Strong Growth?

- **Product driver: Smartphones!**
- **Process developments**
  - Improvements in materials and process, especially to achieve higher pin counts, larger body size, and smaller diameter solder balls
  - Improvements in reliability
  - Test and inspection developments
  - Introduction of Deca's M-Series technology
- **Infrastructure**
  - Investments ($) in capacity
  - Multiple suppliers of fan-in WLP packaging services
  - Internal production operations
  - TSMC's entry into FO market
  - Multiple EMS provides that could use the tape and reel format



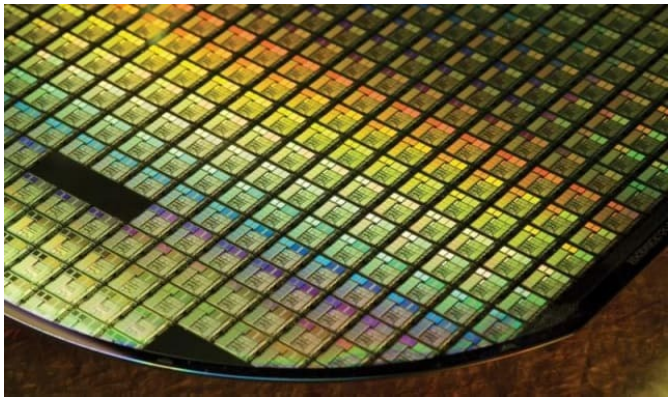
Source: Texas Instruments.



Source: International Rectifier.

What's Next? 3D Integration with Hybrid Bonding

- **In production for Image sensors and MEMS**
  - Sony since 2007
  - MEMS
- **TSMC's SoIC and WoW**
  - System on Integrated Chip (SoIC) 3D stack using CoW process to handle <10µm bond pitch between chips
  - Two-die stack face-to-face (F2F) and a three die stack
  - Use of hybrid bonding
- **Intel's Foveros expected to use hybrid bonding in the future**
- **Memory with hybrid bonding**
  - YMTC in China
  - Others considering for HBM



Source: TSMC.

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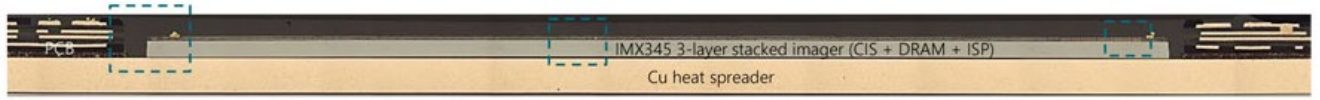
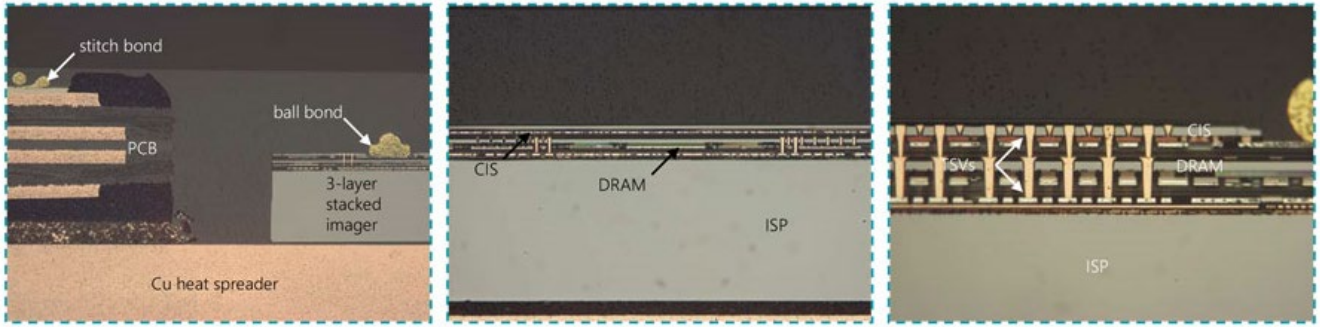
000599 Source: TSMC.

Sony's 3D Stacked Image Sensor



Package Cross-Section – Optical (Annotated)

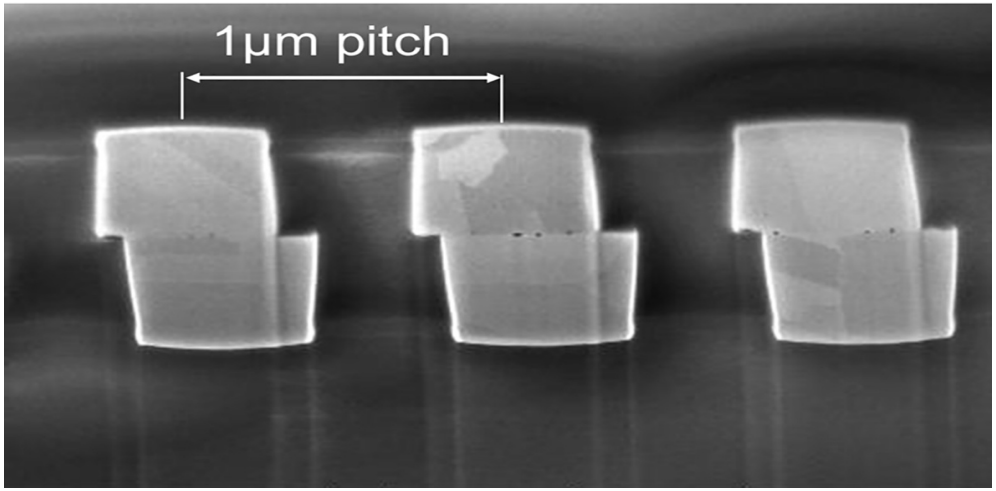


IMX345 Die Stack – Optical

Images courtesy TechInsights.

- **CMOS image sensor die, DRAM die, and signal processor in a 3D stack**

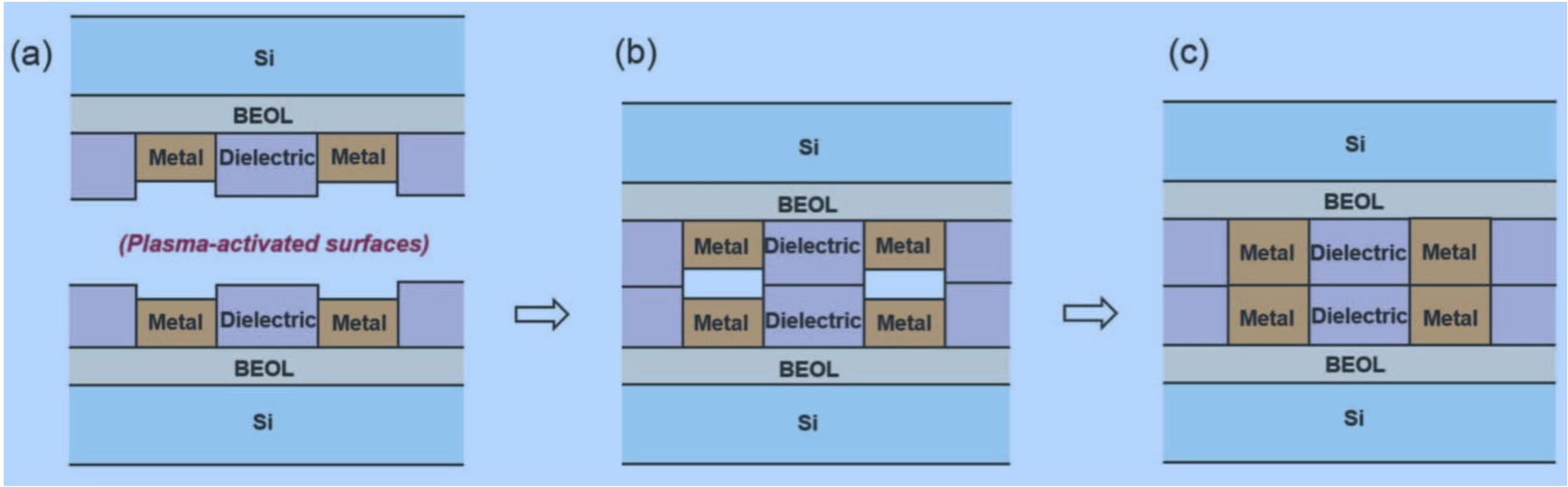
Wafer-to-Wafer Direct Hybrid Bonding with 1µm Pitch



Source: CEA Leti.

- **CEA Leti has conducted extensive research in direct hybrid bonding**
  - Demonstrated wafer-to-wafer direct hybrid bonding with 1µm pitch

Direct Bond Interconnect

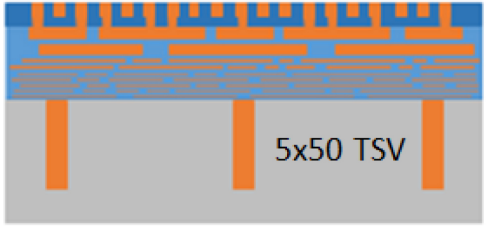


Source: Xperi.

- **Use CMP to create flat surface and slight recessed metal surfaces, cleaned and plasma-activated (or wet chemistry)**
- **Surfaces brought into contact, dielectric surfaces bonded together at room temperature**
- **Batch annealing (metal expands more than dielectric and becomes internally pressurized so metal-to-metal bonding accomplished under this temperature and internal pressure)**

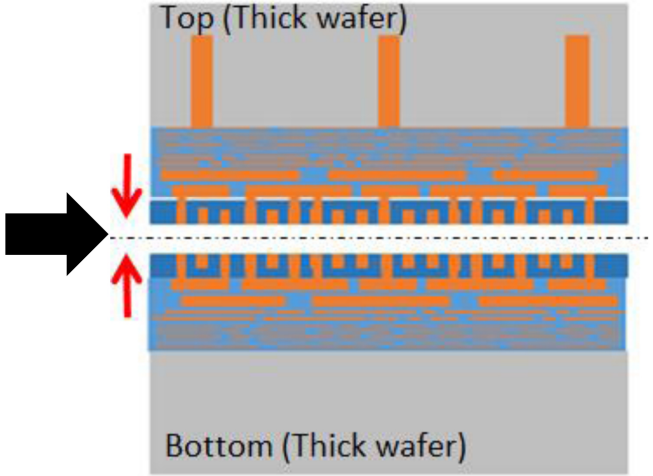
GLOBALFOUNDRIES F2F Process Flow

Face-to-Face Hybrid Bond (F2F) Process Flow

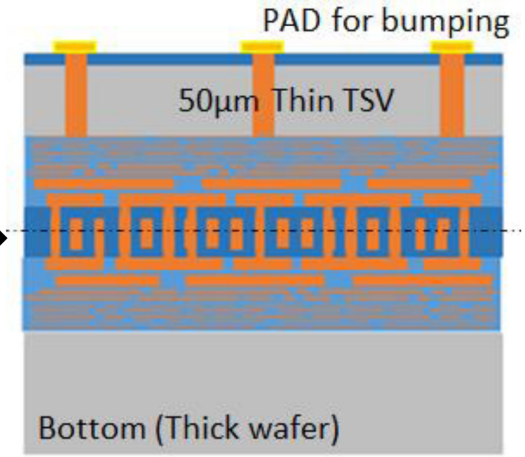


- Build top die with TSV

- Build bottom die w/out TSV



- HWB attach top & bottom wafers together



- Thin, Reveal TSV, form bump pads
- Send to bump/dicing

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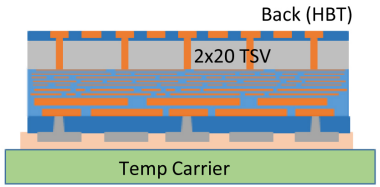
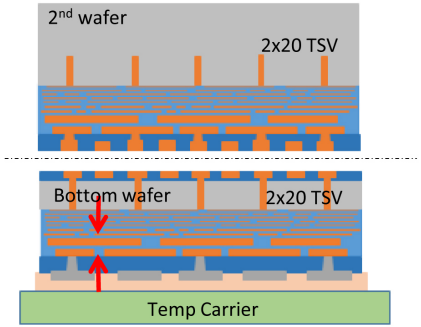
GLOBALFOUNDRIES F2B Process Flow

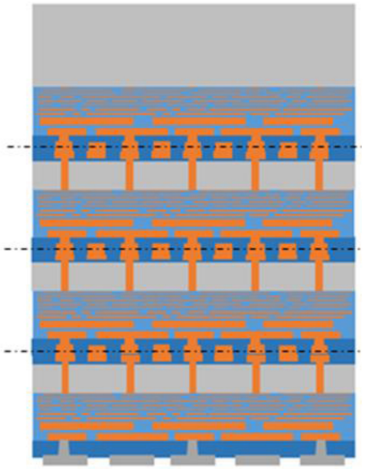
Face-to-Back Hybrid Bond (F2B) Process Flow



- Mount bottom wafer on temp carrier
- Thin, TSV reveal, form HBT back-side



- HWB attach next wafer face-down
- Thin, TSV reveal, form HBT back-side



- Repeat steps until 4th wafer (can be w/out TSV)
- Detach temp carrier, send to bump/dicing

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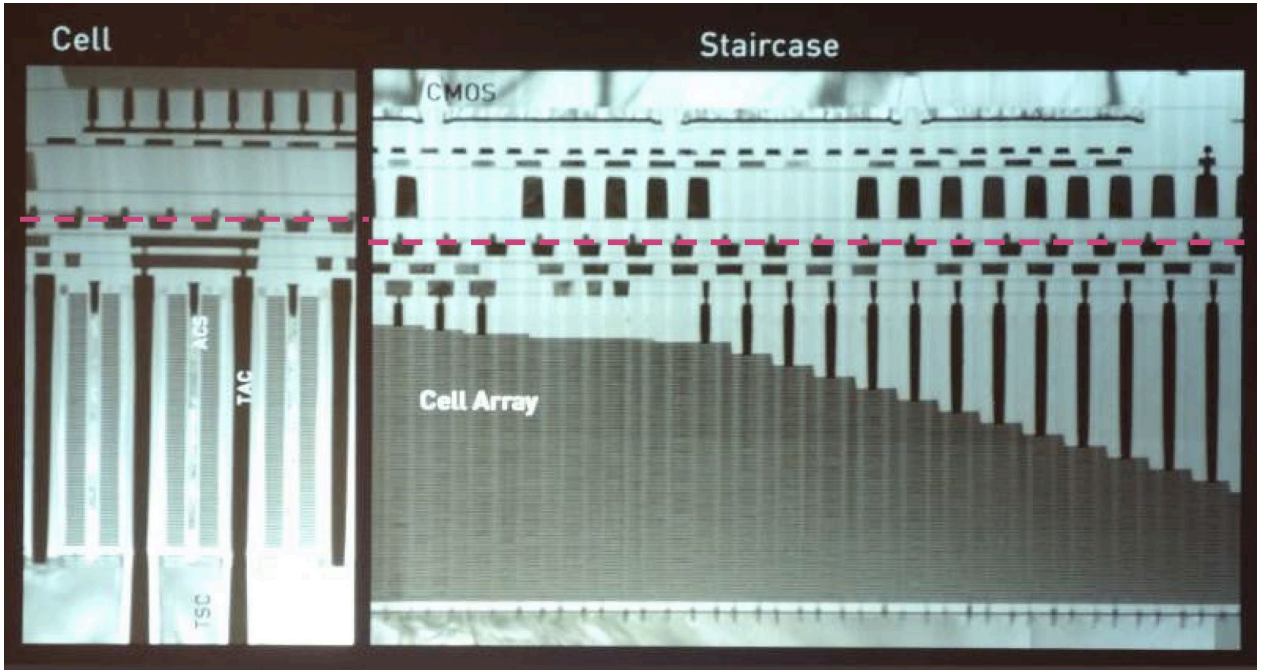
YMTC Flash Memory



- **W2W hybrid bonding to bond logic wafer to stacked cell NAND**

Intel Foveros 3D Face-to-Face Stacking

Source: Intel.

- **Intel's Foveros die are stacked on an active interposer (future hybrid bonding)**
- **Gives designers greater flexibility to mix and match IP blocks with various memory and I/O elements into new form factors**
- **Technology uses 3D face-to-face stacking process**
- **Large die are bumped and mounted on an active interposer next to memory or other die**
  - Active interposer can contact platform controller hub (PCH) that manages I/O for the system
  - Active interposer is attached to the package substrate with solder bumps

What is Required for Hybrid Bonding's Growth?

- **Process requirements**
  - Needs clean room environment
  - Good process control is critical (especially CMP)
  - Dicing method that generates few particles and process to remove particles (die cleaning)
  - Good pick and place and handling of thin die (D2W) or wafer handing (W2W)
  - Alignment accuracy is critical, (high accuracy, high yielding)
    - Die-to-wafer ≤ 1 µm
    - Wafer-to-wafer ≤ 200 nm
  - Low temperature process (plasma surface activation to remove copper oxide) and annealing temperature ≤350° C
  - High throughput method to inspect or test to guarantee good joints
- **Infrastructure**
  - Equipment and material suppliers
  - Investment in capacity for hybrid bonding (will this be only at the foundry or the IDM?)

Thank you!

TechSearch International, Inc.
4801 Spicewood Springs Road, Suite 150
Austin, Texas 78759 USA
+1.512.372.8887
tsi@techsearchinc.com

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