ASE GROUP

Integration Technologies Transforming the World

Yin Chang (Rich Rice presenting)
March 4th, 2020

16th International Conference
and Exhibition on Device Packaging
GBC Session

Top 10 Global Companies by Market Capitalization

These technology companies are leading the digital transformation of the global economy and fueling the AI revolution – Data is the new oil

2006 Dec 31

- Exxon Mobil
- General Electric
- Gazprom
- Microsoft
- Citicorp
- Bank of America
- Royal Dutch Shell
- BP
- Petro China
- HSBC

2019 Sep 30

- Microsoft
- Apple
- Amazon
- Alphabet
- Berkshire Hathaway
- Facebook
- Alibaba
- Tencent
- Visa
- JPMorgan Chase

Size of Global Datasphere

Source 2006 & 2019: Statista & FXSSI

Source: Data Age 2025, sponsored by Seagate with data from IDC Global Datasphere, Nov 2018

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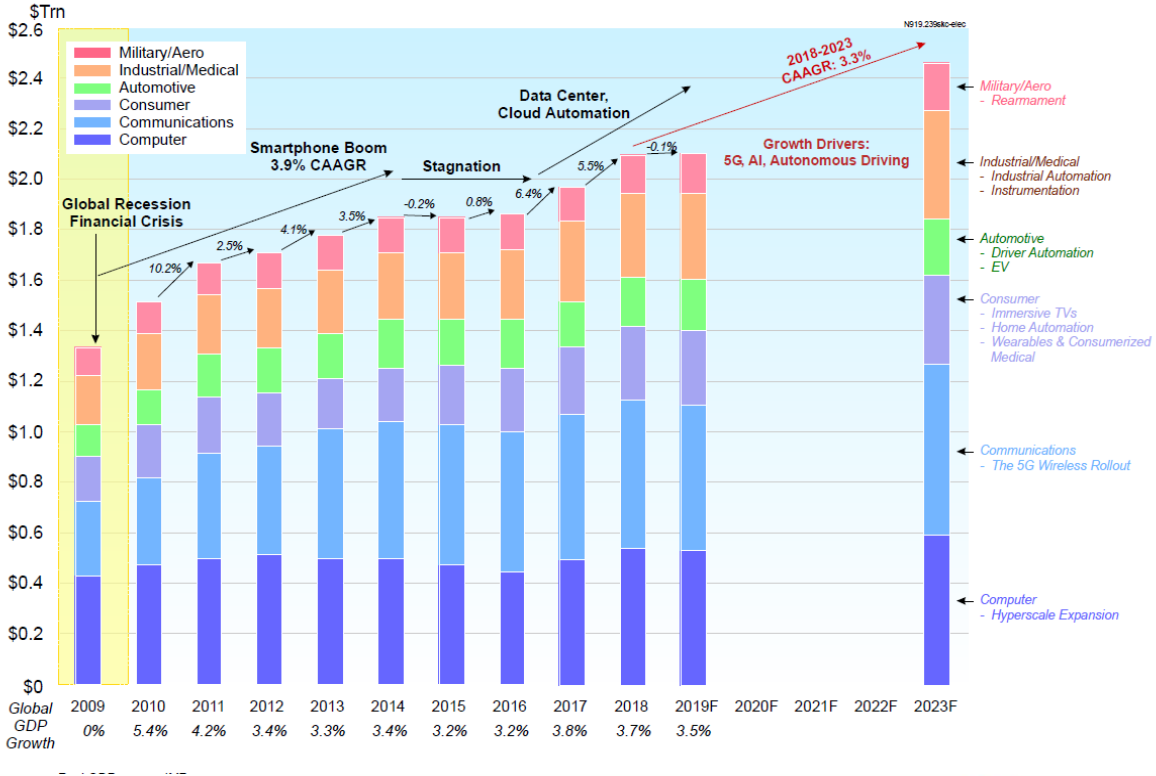
Electronics Industry Forecast



Prismark's View

- **2014-2017: Smartphone boom stagnation ($1.85T)**
- **2017: Industry growth cycle resumes ($1.95T)**
  - **Key drivers: data center & cloud automation**
- **2018-2023: Continued growth ($2.1T to $2.5T)**
  - **3.3% CAGR**
  - **Key drivers: 5G, AI and autonomous driving**

Source: Prismark, Oct 2019

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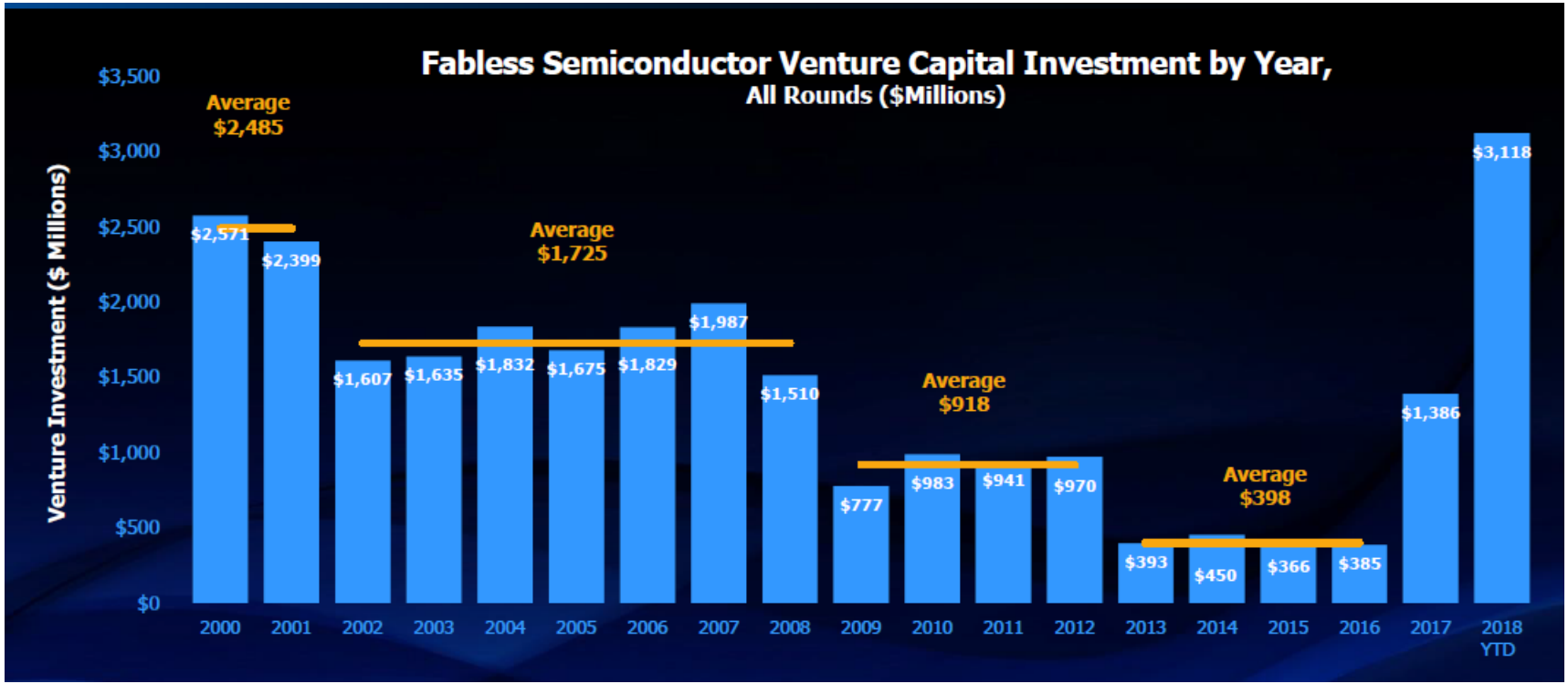
VC Funding for Semiconductor Start-Ups



Source: Wally Rhines, Mentor

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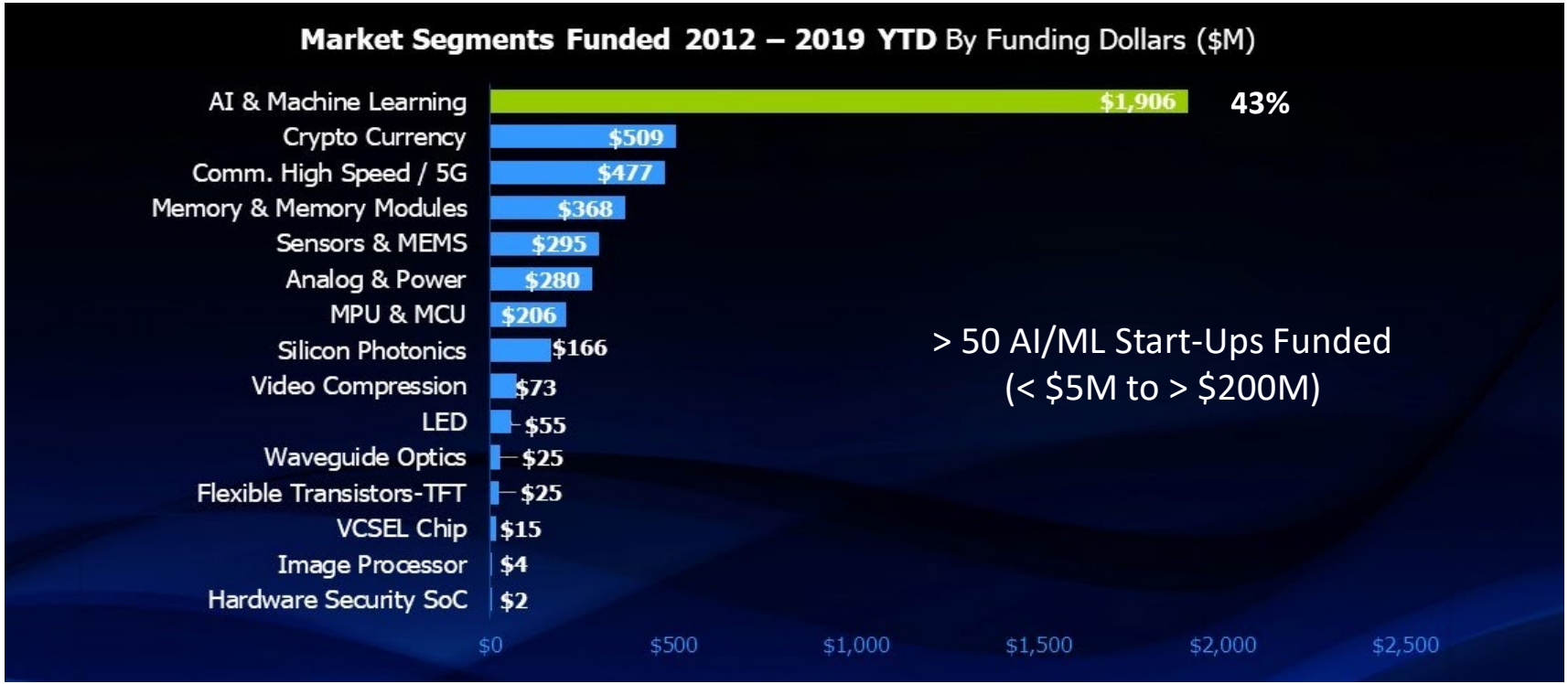
Start-Up Funding Dominated by AI / Machine Learning



Source: Wally Rhines, Mentor

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AI Deep Learning - Training and Inference Hardware

Market Forecast

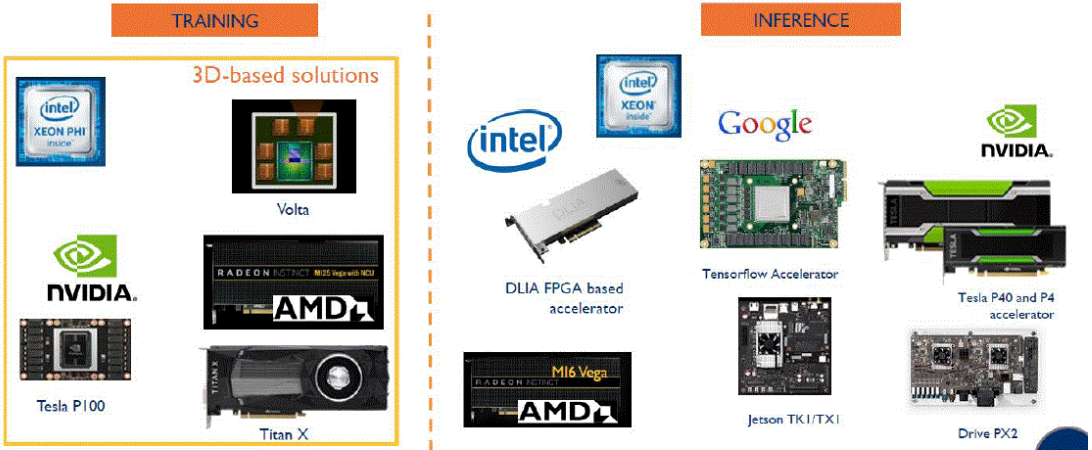
DEEP LEARNING HARDWARE

Hardware for TRAINING require large bandwidth, 3D-based products offer solutions.

INFERENCE require less bandwidth but low latency. Interposer could come as a solution because of its modularity and its capacity to integrate more than 4 chips.

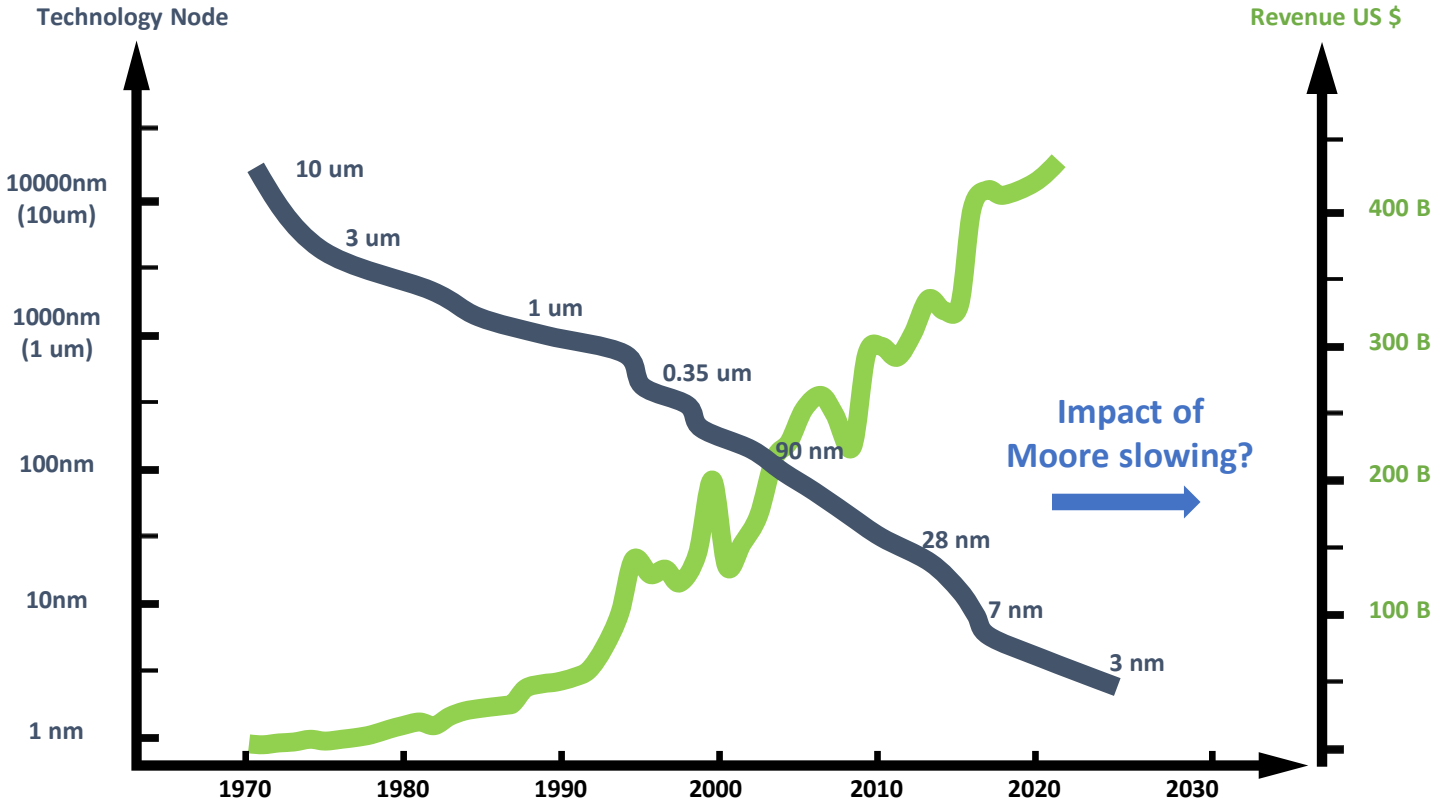
Main players offer clear different product lines as solutions for both steps.

3D and 2.5D packages have enabled performance hardware for deep learning applications



source: Yole 3D TSV and 2.5D Business Update - Market and Technology Trends 2017

Semiconductor Revenue vs. Process Generation



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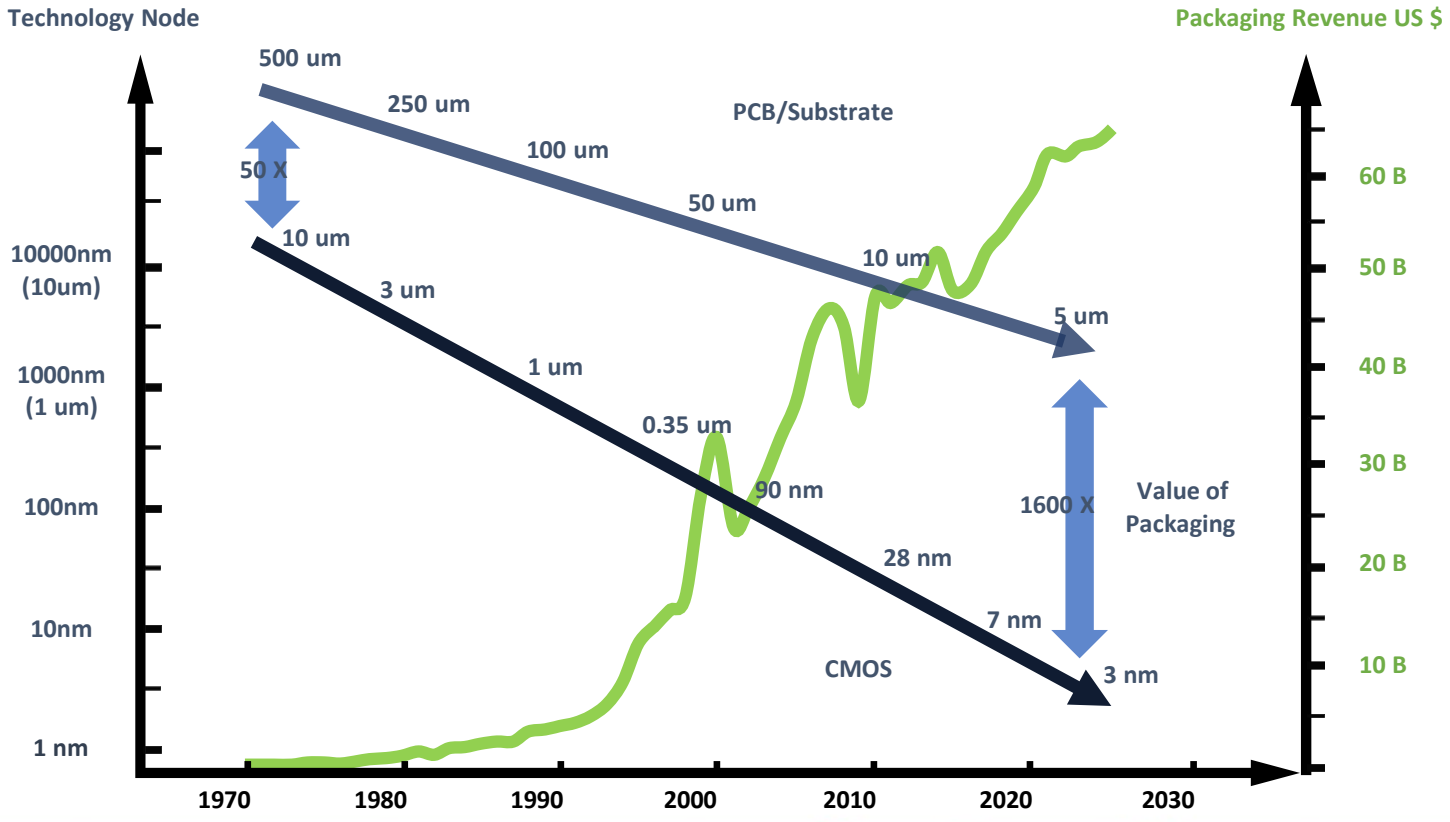
Value of Semiconductor Packaging is Increasing



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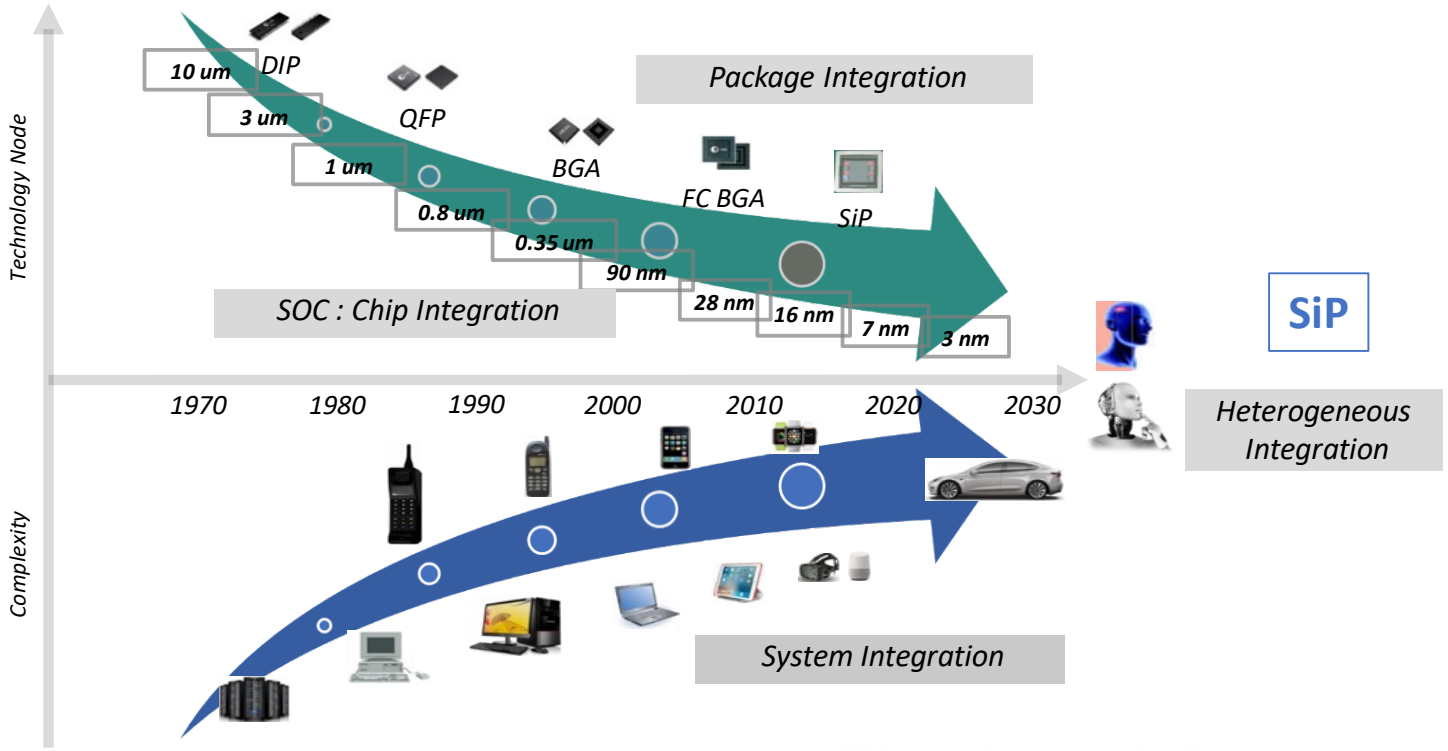
Chip & System Integration Convergence



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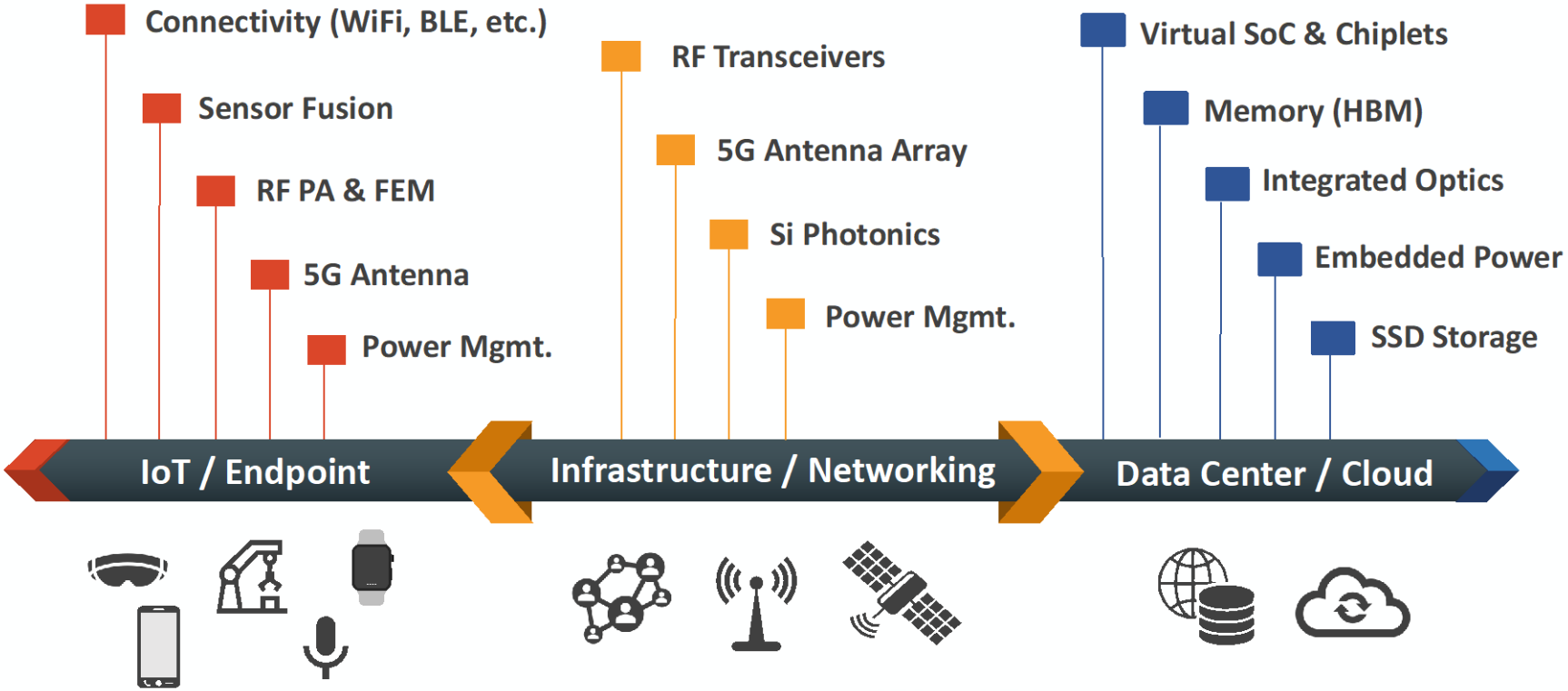
Integration Opportunities – From Edge to Cloud



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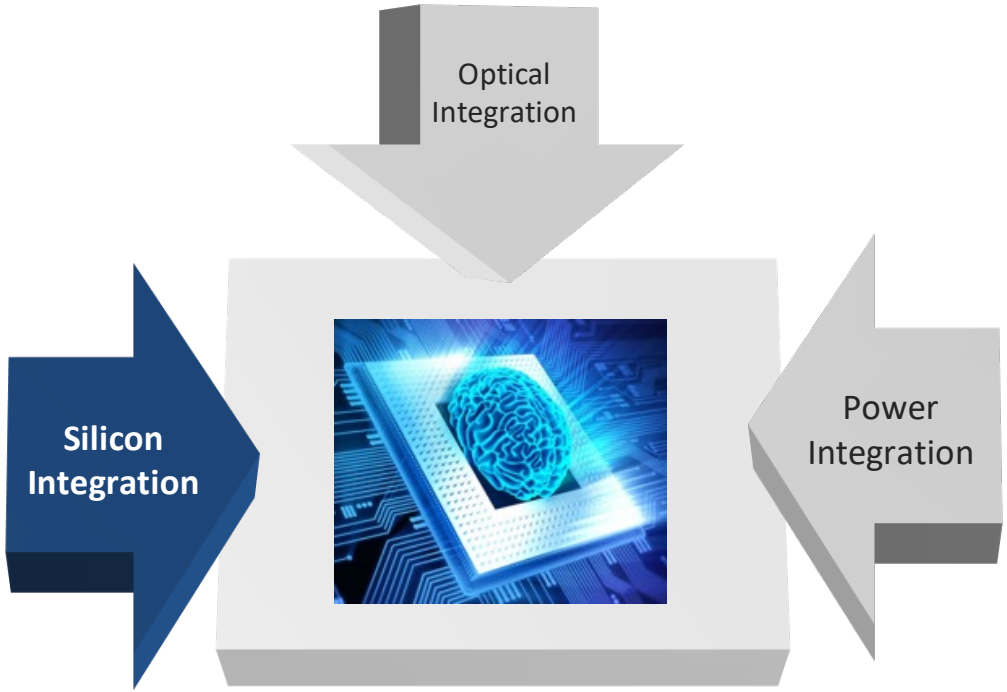
HPC / AI Packaging Technology Drivers



Silicon Integration

- SoC alternative
- Die partitioning (yield & cost)
- Memory integration (HBM)
- Separation of digital and analog
- IP re-use (Chiplets - SerDes)
- Power reduction
- Improved bandwidth and latency
- System integration

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Emergence of Die Partitioning and Chiplets

- Drivers and benefits:
  - Moore's law benefits are slowing at SOC level
  - Traditional SOC cost barriers- NPI costs inflating
  - SOC scaling limitations for integration of analog, logic and memory circuits
  - Economic leverage of trailing nodes for analog and mature devices
  - Mix & match systems – time to market, system flexibility
  - Performance and cost optimization for individual chips
  - Near Monolithic & More Than Monolithic Integration better performance than SoC

- Key Integration Technologies
  - MCM, 2.5D, 3D, Fan-out, Bridge

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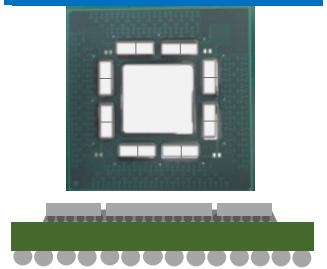
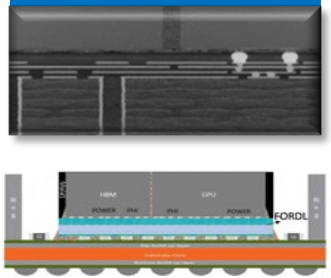
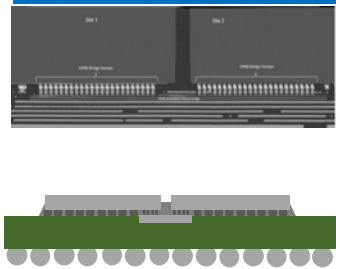
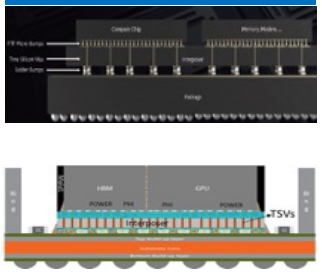
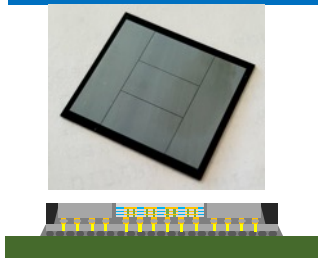
Heterogeneous Silicon Integration Platforms

FC MCM	FanOut RDL	BRIDGE	2.5D TSV	3D IC
				
• Organic substrate ($) • Low/med density D2D • > 10um line/space • > 100um bump pitch • > 50um D2D spacing • Chip last process • Cost effective	• Post fab RDL ($$) • FC to organic subs. • Med/high density D2D • > 1um line/space • > 40um bump pitch • 100um D2D spacing • Chip first / last • No TSV – lower loss	• Embed Si die ($$$) • Med/high density D2D interconnect • < 0.5um line/space • > 40um bump pitch • High bandwidth • 100um D2D spacing • Chip last process • No TSV – lower loss	• Si Interposer ($$$$) • High density D2D • < 0.5um line/space • > 40um bump pitch • High bandwidth • > 50um D2D spacing • Chip first/last • Power limitation	• Direct D2D ($$$$) • High density D2D • Foundry line/space • > 40um bump pitch • High bandwidth • Shortest interconnect • FC or hybrid bond • Custom die designs

Increasing Bandwidth & Cost

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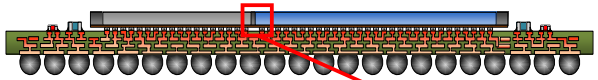
FanOut / FOCoS

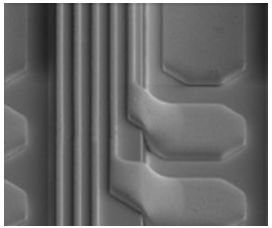
- RDL based interconnect, 2/2um line/space
- Multi-layer routing (3-4 lyrs.)
- Medium to high interconnect density (1000's to 10,000)
- Large FO area (1200-1600mm2)
- Stacked vias (10um hole/15um land)
- Chip first or chip last process
- Benefits
  - Die size, yield and cost optimization
  - Process node / functionality optimization
  - Integration of digital/analog SoCs
  - Short, high density interconnect
  - No TSV - Lower cost alternative to 2.5D
  - Increased reliability vs. MCM

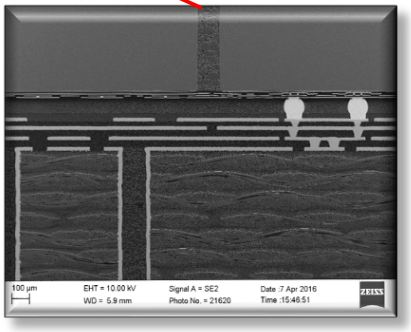
Fan Out Compound Die

Fan Out Hybrid BGA Package




Stacked Via


2/2 µm
Lines/Spaces



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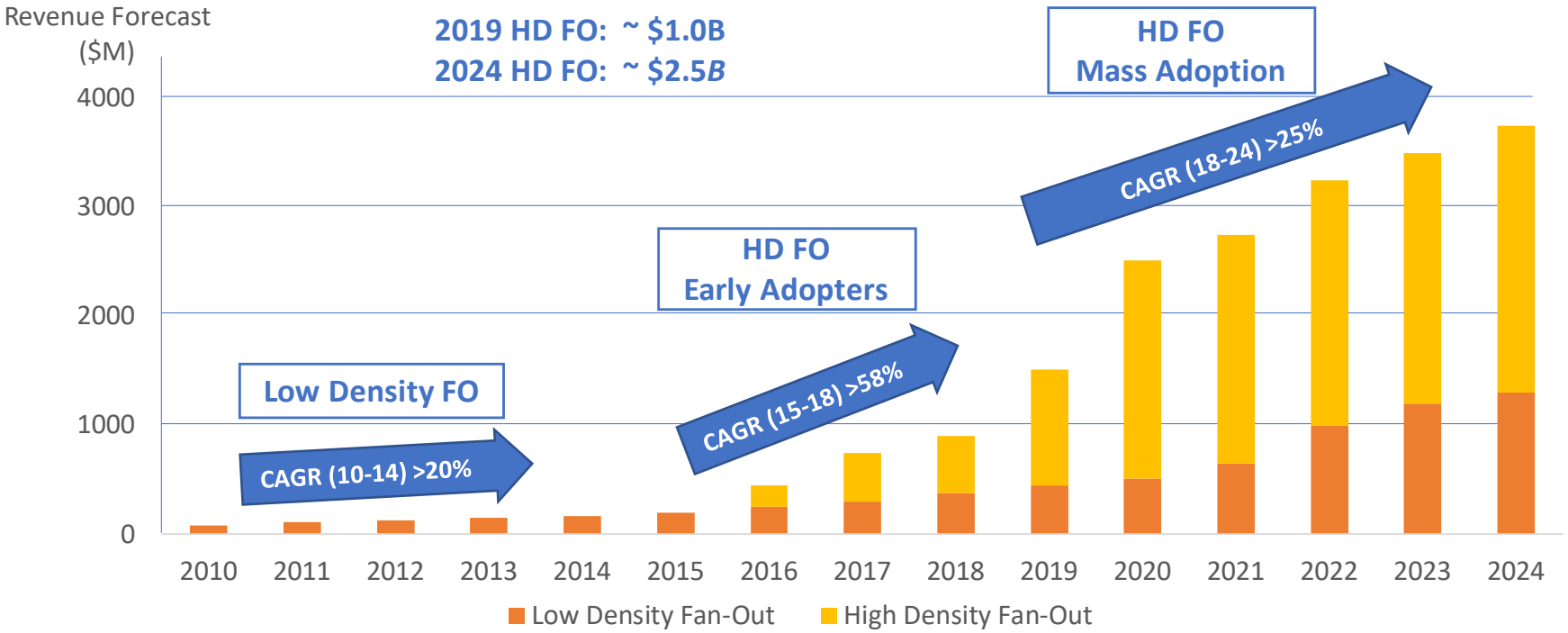
Fan-Out Market Forecast



Source: Yole Development, Jan 2019

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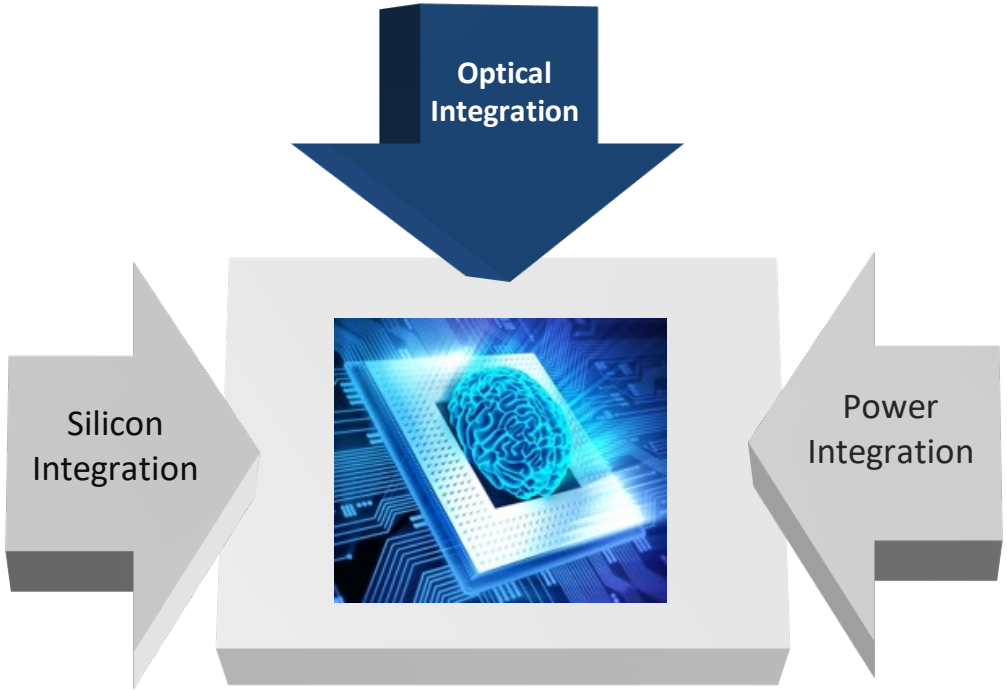
HPC / AI Packaging Technology Drivers



Optical Integration

- Increased data rate & bandwidth
- Reduced power consumption
- Decreased thermal load & management
- Increased data center east/west traffic
- Longer interconnect distances
- Higher reliability

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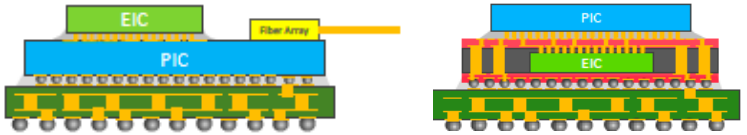
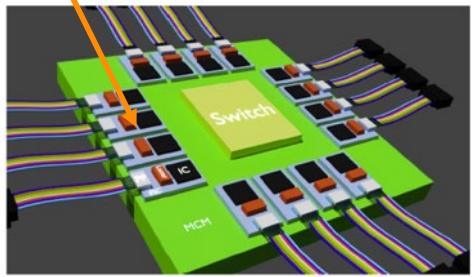
Connectivity Roadmap

- **Transition:**
  - **Telco/longhaul -> DCI/intra-data center**
  - **Pluggable -> On-Board (OBO)**
  - **OBO -> Co-Packaged (CPO)**
- **Optical interconnect drivers:**
  - **> 100-400GHz performance**
  - **Long data center interconnect (< 2km)**
  - **Wired solution power consumption**
- **Replace discrete optics with Si Photonics for cost and scale**
- **Eliminate faceplate connector density constraint**
- **Enable 50Tb and above switching**

Si Photonics Engine



Pluggable transceiver connectivity



Co-packaged optics for direct switch connectivity

2015 data center power consumption (45.9GW) represented 1.62% of worldwide production - will rise to 1.9% (58GW) by 2020

Source: Yole

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Benefits of Using Optical

- **Higher bandwidth -> Higher data rate**
- **Low attenuation -> reduced power and less repeaters/amplifiers**
- **Reduce power -> less heat generated and less facility cooling required**
- **No electromagnetic interference -> improved signal quality and integrity**
- **High reliability -> moving fiber inside data center**

	Optical Communication	Electrical Communication
Transmission	Optical fiber	Copper wire
Maximum Bandwidth	~75000 GHz	~1GHz
Data Rate	100Tbps - 1000 Tbps	10 Gbps - 100 Gbps
Attenuation	0.3dB/km Signal strength loss 7% per Km	20dB/100m Signal strength loss 99% per 100m
Electromagnetic interference	None	Yes

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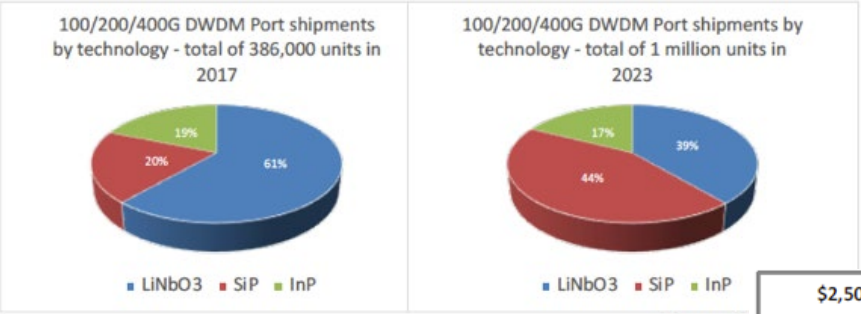
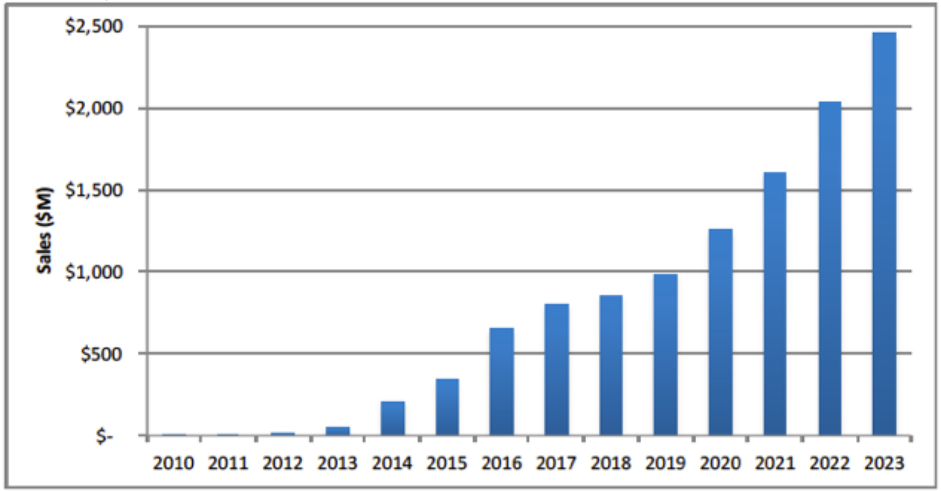
Si Photonics Outlook



- SiPh transceiver market reached ~ $800m in 2017 (22% YoY growth)
- SiPh transceiver market to grow at 20% CAGR to $2.4B in 2023

- SiPh driven by 100G, 200G and 400G DWDM applications
- SiPh share to accelerate for > 400G devices due to need for more integration
- SiPh based 100-400G port shipment share to reach 44% in 2023



Source: LightCounting

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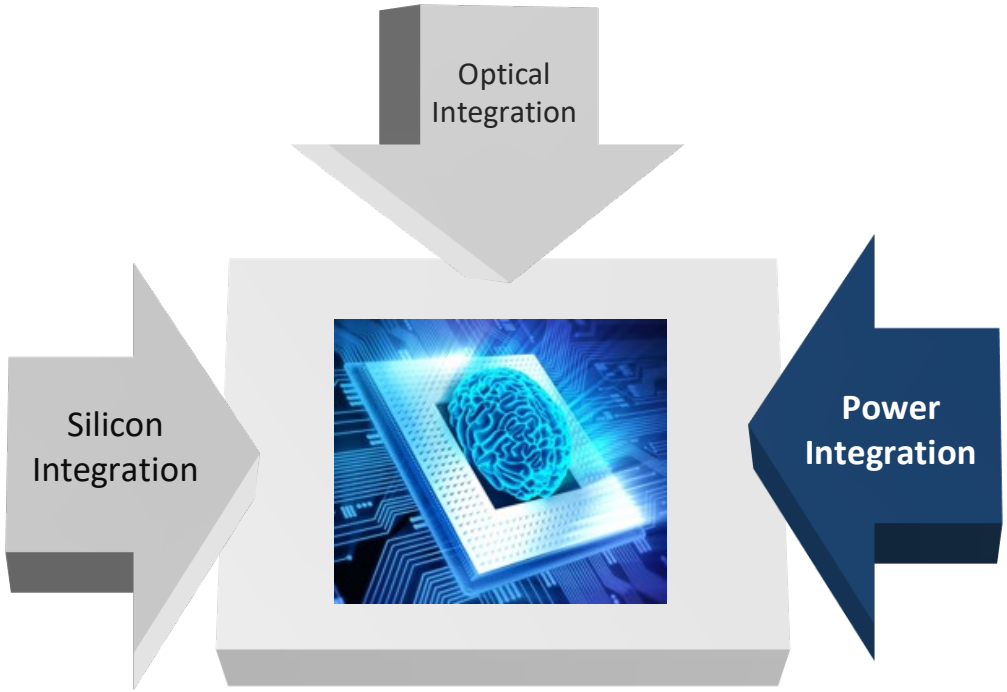
HPC / AI Packaging Technology Drivers



Power Integration

- Increasing power consumption
- Decreasing operating voltages
- System efficiency limitations with lower V_{out}
- Impact of droop
- Higher switching speeds
- System board size reduction
- Power rail limitations

Efficiency is inversely proportional to the physical distance power delivery is from the die

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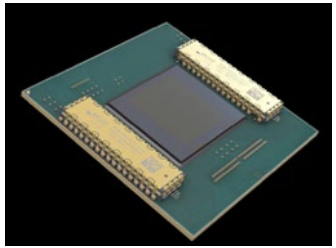
Power Integration Approaches

- **Silicon solution**
  - **Passive component integration in die or interposer**
  - **Wafer based processing**
  - **Advantages: Small size, well controlled values, scalable with die area**
  - **Challenges: Cost, low input voltage, new chip design**
- **Package/substrate solution**
  - **Passive components embedded in substrate**
  - **Advantages: No direct chip design impact, reduces board size, high efficiency, scalable with die area**
  - **Challenges: Passive availability, embedding limitations**
- **Platform solution**
  - **Discrete power modules mounted on package substrate**
  - **Advantages: No chip design impact, smaller system board, 'off the shelf' solution**
  - **Challenges: Size, scalability, Z height, power rail limitations**



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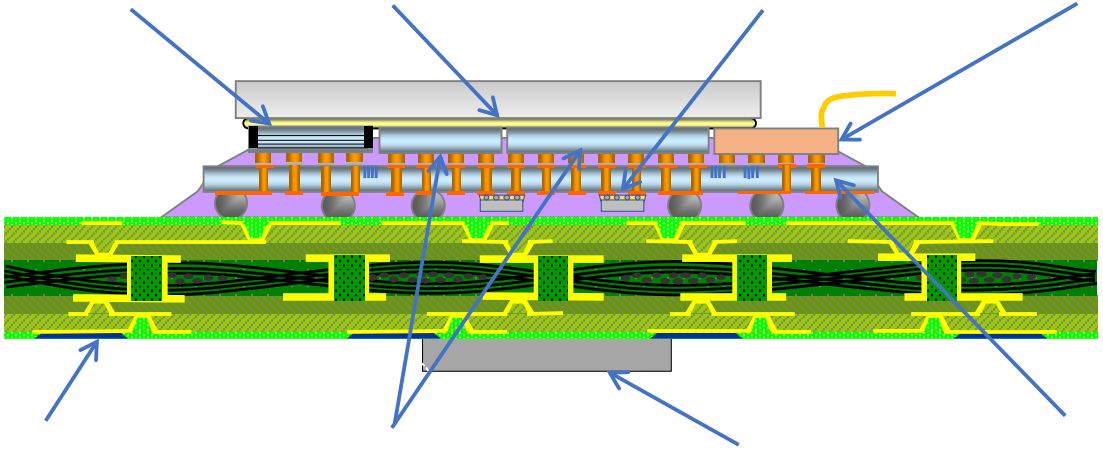
HPC / AI Integrated Compute Platform?

High Bandwidth Memory
- 4-High / 8-High

High Power Dissipation
- 500W @ 800mm^2

Power Integration
- DT Caps, Inductors

Optical Chiplets
- Active Interposer



Large Package
- > 90x90 mm

Heterogeneous Die Integration
- Chip first/chip last

Power Mgmt Module
- Surface mount

Large Interposer (or FanOut
- > 1.5x reticle size

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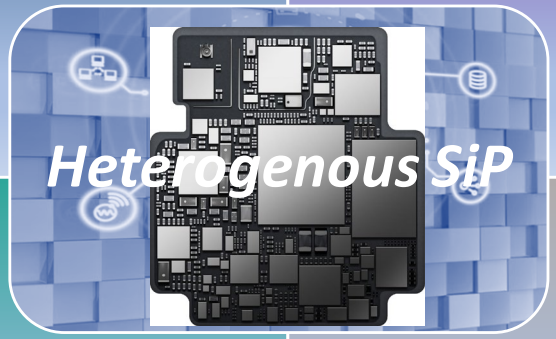
At the Edge: rising demand for integrated products

IoT and Cloud create the need for edge computing where data processing occurs in part at the network edge, rather than completely in the cloud.

Edge devices must manage complex operations, including sensing, compute, power management, and increasingly Artificial Intelligence.



Ensuring the right processing takes place at right time and place, edge compute devices can address latency, battery life, bandwidth costs, security, privacy, and more.

Heterogeneous integration through SiP provides a platform for multiple die from multiple sources to be packaged together, offering huge performance, power and footprint advantages.

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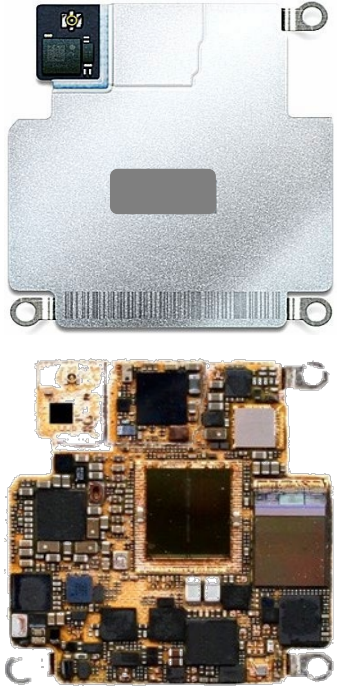
SiP – System in Package

- Multi-device & passive component integration
- System / sub-system functionality
- Bare and packaged die
- Leverage IC packaging technology & HD SMT
- Enables local compute and AI processing – small data
- Benefits
  - MicroPCBA system solution
  - Supports sensor integration
  - Module level certification (FCC, etc.)
  - Improved reliability
  - Reduced power and size



~ 26x28mm

Source: TechSearch, TPSS Level 2.5E July 2015

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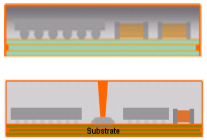
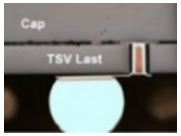
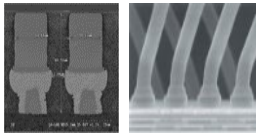
SiP Module Enabling Technologies



Shielding

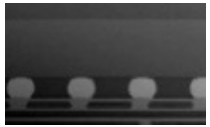


TSV



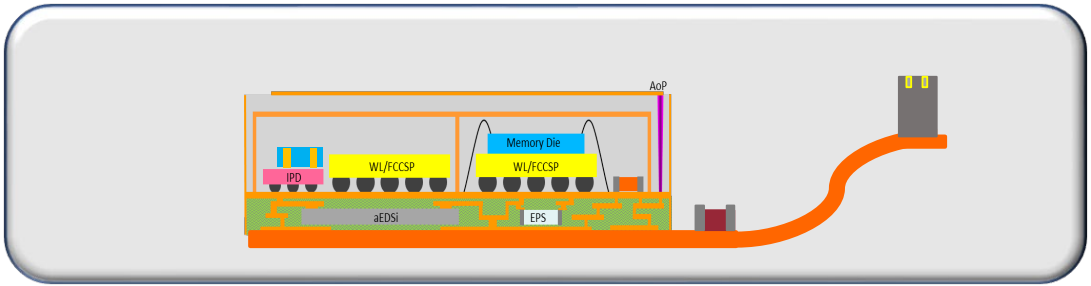
Interconnection

Antenna

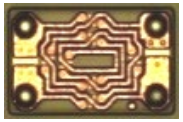


Molding

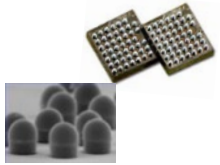
HD SMT



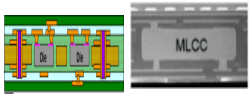
DK SiP Enablement-
Proto/Test



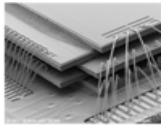
Passives / IPD



Wafer Bumping
/ WLP/FOWLP



Substrate/Carrier
Technology



Die / Pkg
Stacking

Mechanical
Assy

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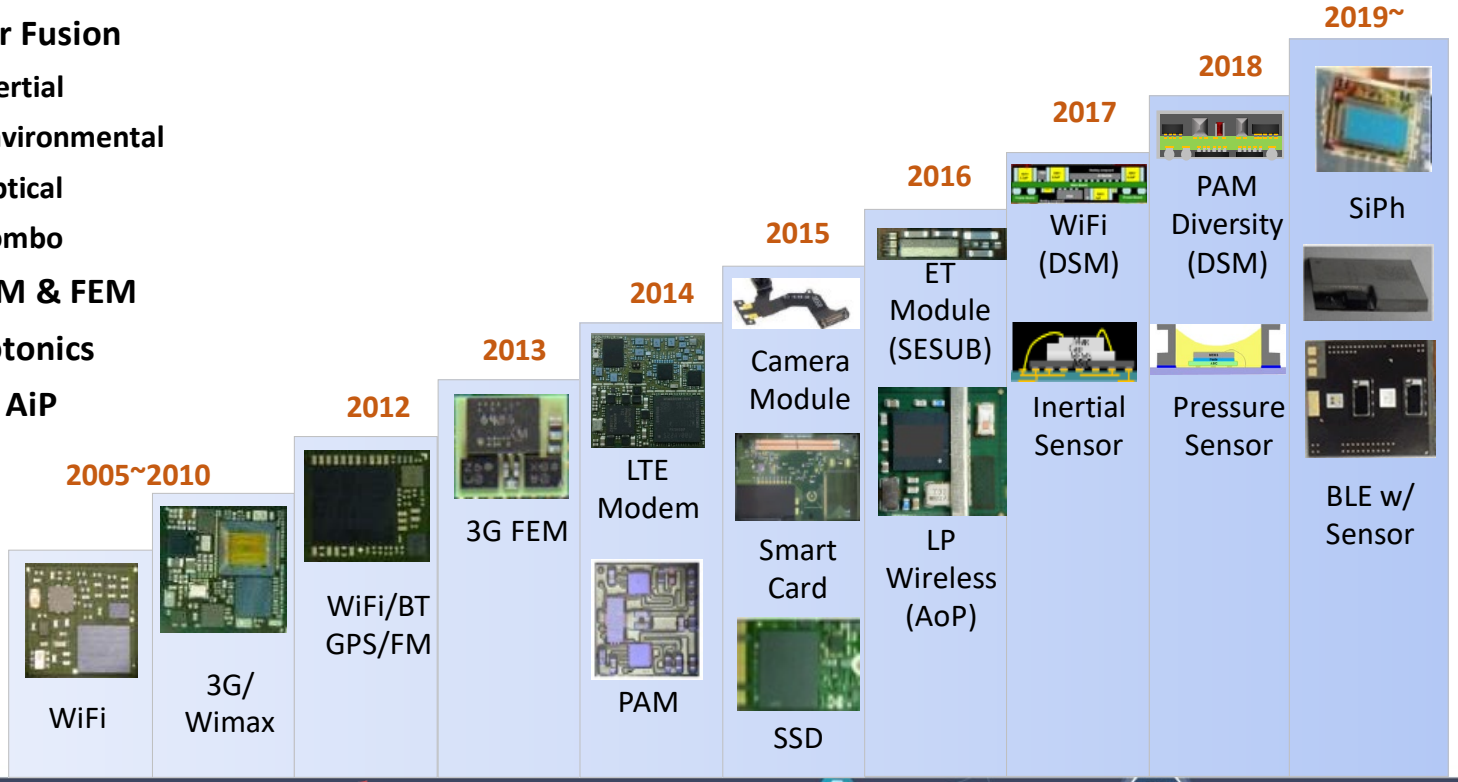
SiP Module Evolution

- Connectivity Modules (LTE, WiFi, BLE, etc)
- Sensor Fusion
  - Inertial
  - Environmental
  - Optical
  - Combo
- RF PAM & FEM
- Si Photonics
- 5G RF AiP



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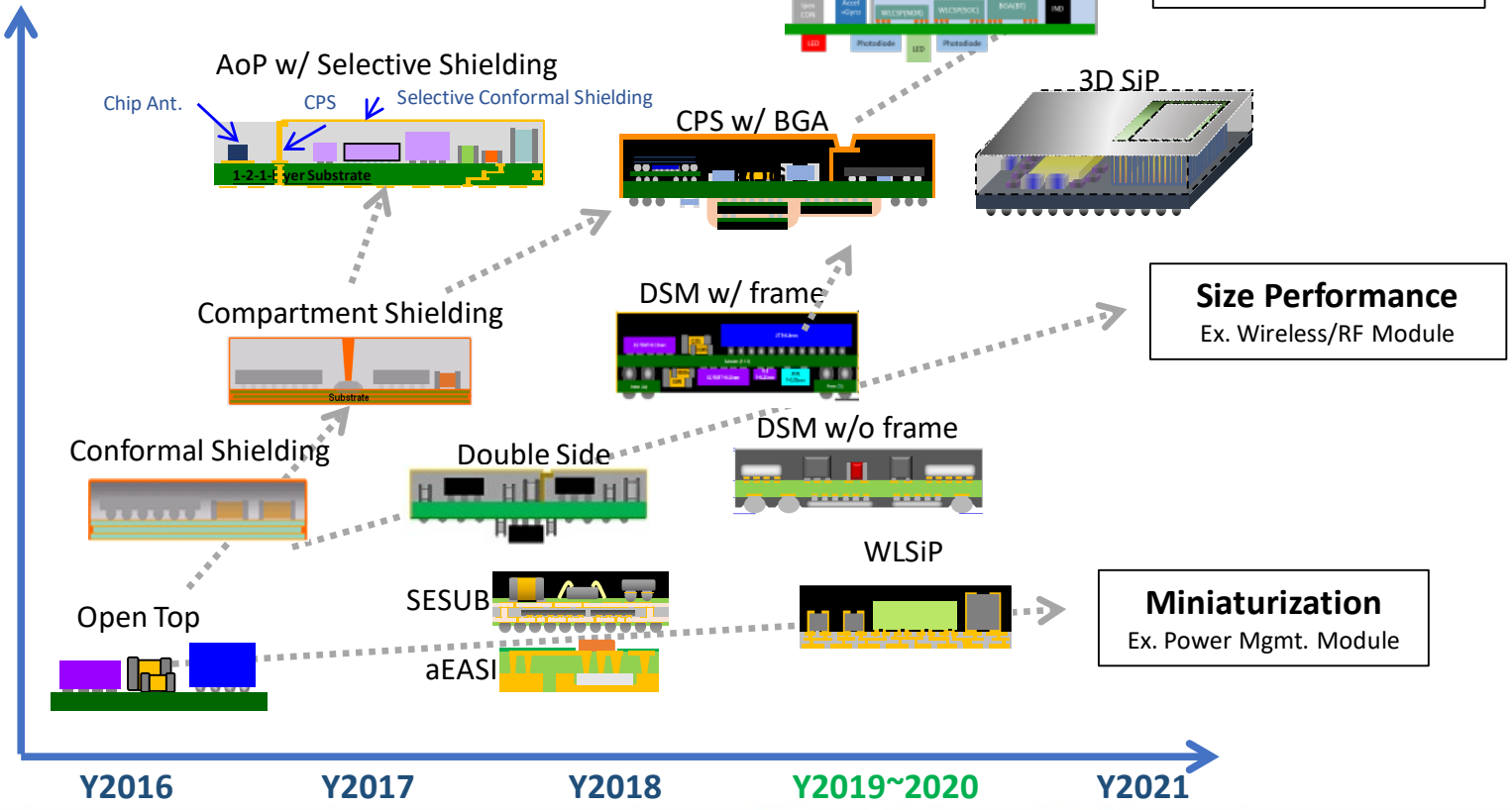
SiP Technology Direction



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Ecosystem Support Required

- **EDA & simulation**
  - 2/2.5/3D device/package co-design & tools
  - Mixed organic and silicon based material sets
  - Multi-process and functionality devices
- **Assembly:**
  - High accuracy / UPH bonders (FC and hybrid)
  - High volume / UPH optical alignment & assembly tools
- **Metrology:**
  - Process monitoring and inspection of 3D die/package structures
  - Underfill / mold voids, RDL /vias, solder joints
- **Test**
  - SiP test systems and methodology - ATE vs. SLT
  - DFT – Bring-up and debug
  - Yield monitoring & optimization tools
- **Materials**
  - Low profile & embedded passives for power integration
  - Low Dk/Df substrates
  - Thermal management

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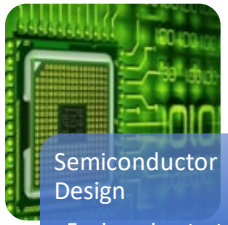
Providing Complete Value Chain Solution

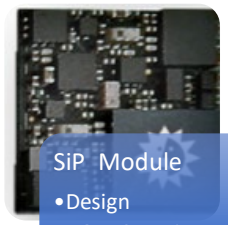
Integrating OSAT and EMS



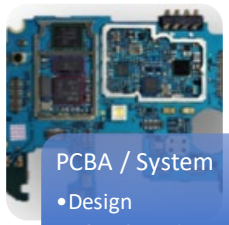
Semiconductor Design
- Engineering test services

Wafer Fabrication
- IDM
- Wafer Foundry

Packaging & Test
- Wafer Sort
- Bump / FanOut
- Assembly
- Final Test



SiP Module
- Design
- BOM Sourcing
- Assembly
- Module Test
- FAE support



PCBA / System
- Design
- BOM Sourcing
- Assembly
- System Test
- Logistics

ASE Group Services

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Thank You

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