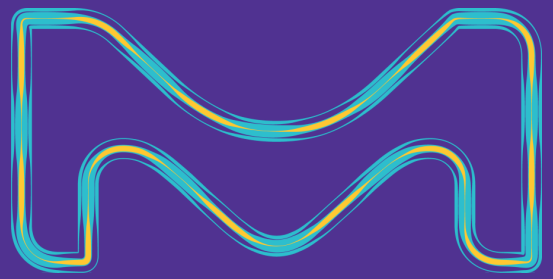
TLPS pastes for Anywhere Embedded Passive Components in substrates and PCBs

Catherine Shearer and Gary Legerton

Ormet Circuits, Inc

IMAPS Device Packaging Conference 2021



EMD Electronics

TLPS Z-Axis Interconnect with Embedded Passives
Agenda

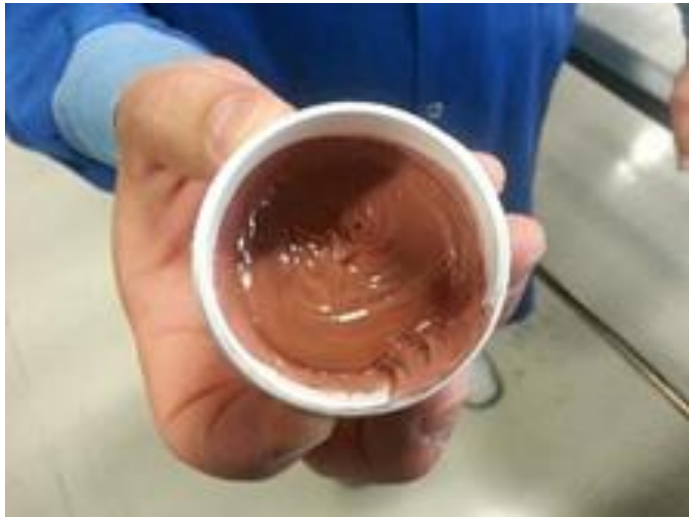
Introduction to TLPS pastes for Z-axis interconnect

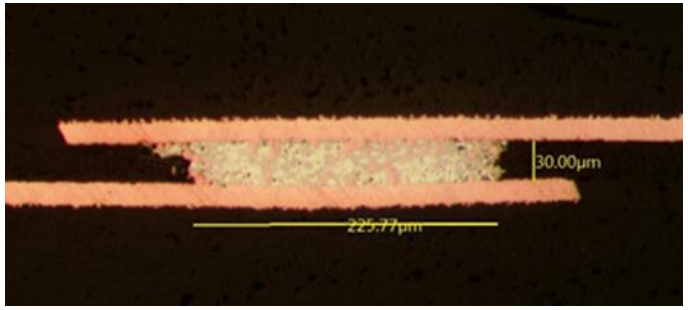
Strategies in implementation process

- Any-layer
- Core-to-core
- Mixed mode

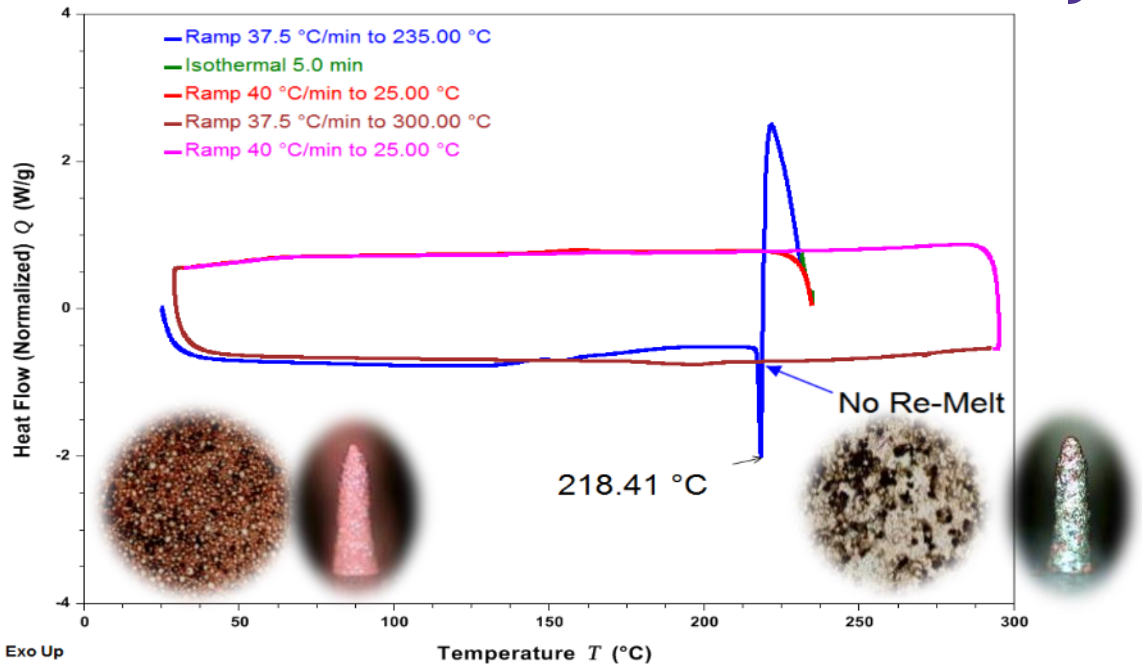
Embedded passives

- Reflow vs. via attachment
- Prototype builds using a daisy chain test vehicle
- Comparison of results

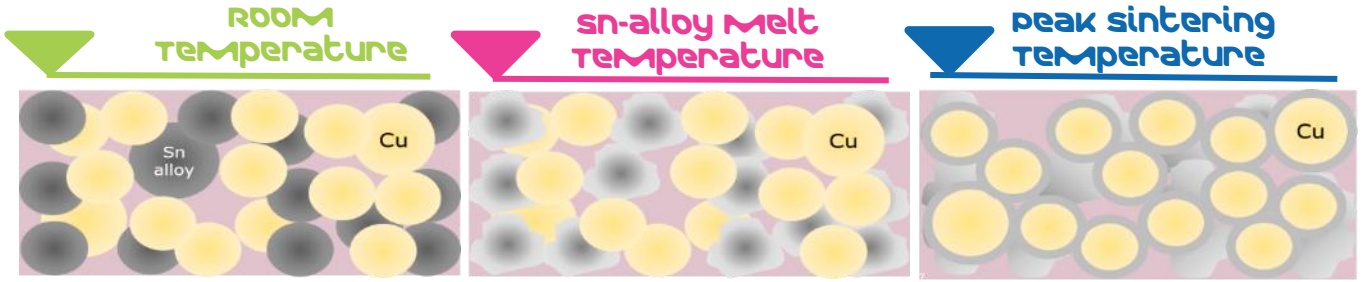




What we make:
Transient Liquid Phase Sintering: Ormet® TLPS



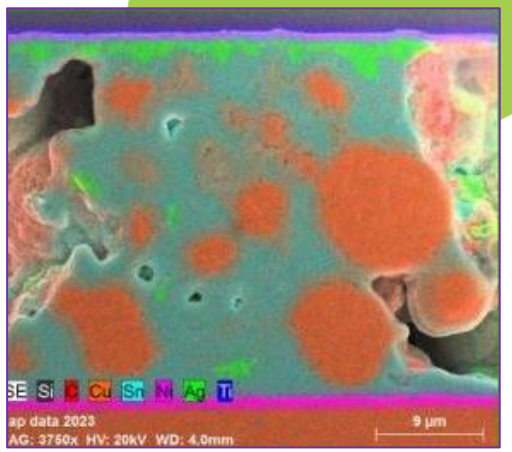
- **Processes like solder**
- **Electrical, thermal and mechanical characteristics like solder**
- **Does *not* remelt like solder – multiple assembly steps can be accomplished with the same paste formulation**



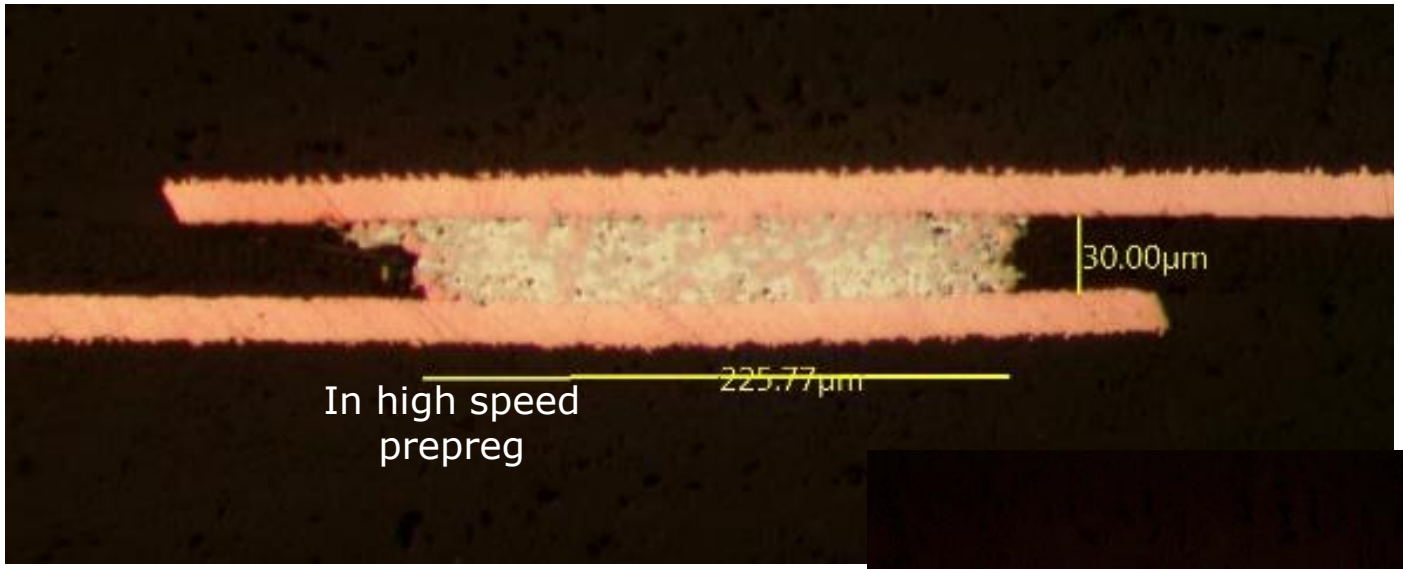
Cu and Sn-alloy particles are suspended in a flux vehicle

Alloy particles melt and wet the copper particles and metallized surfaces

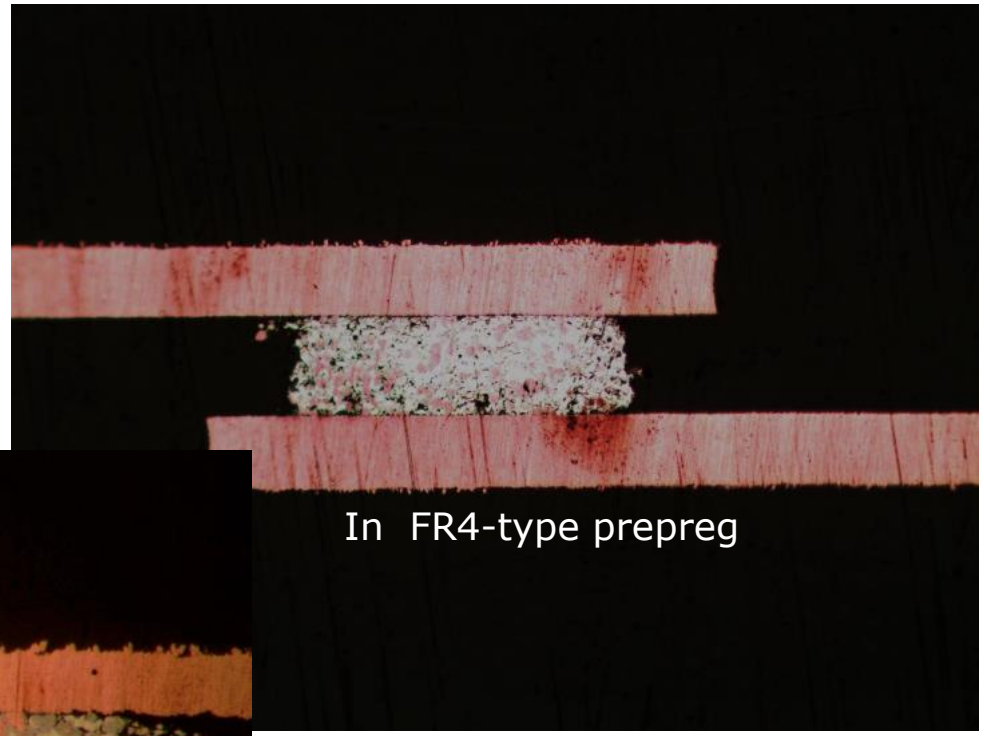
Sn and Cu interdiffusion to form new alloys with melting temperatures **>400°C**



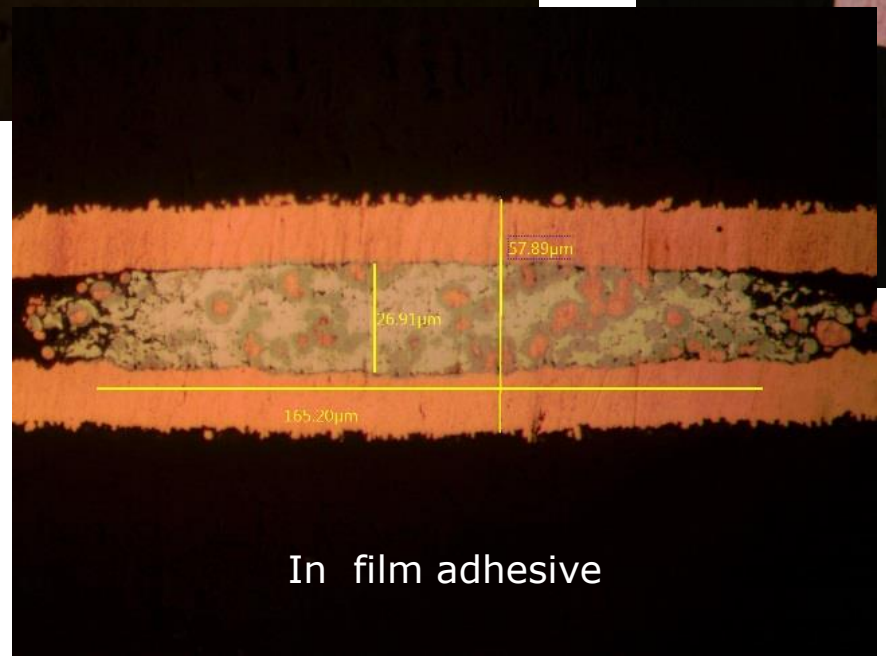
A versatile platform
Microstructure and Compatibility with Lamination Adhesives



In high speed prepreg



In FR4-type prepreg



In film adhesive

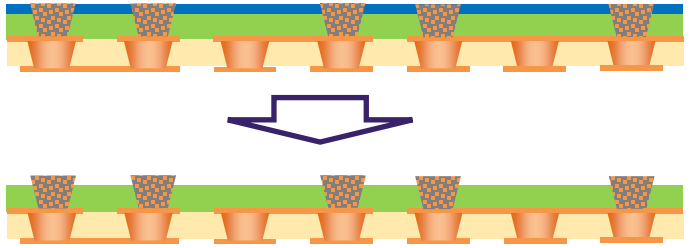
Basic implementation of TLPS paste vias
Fabricate cores in parallel and join with via layers

STEP-1: Adhesive material selection

STEP-2 Tacking to circuit core

STEP-3 Laser ablation of blind vias

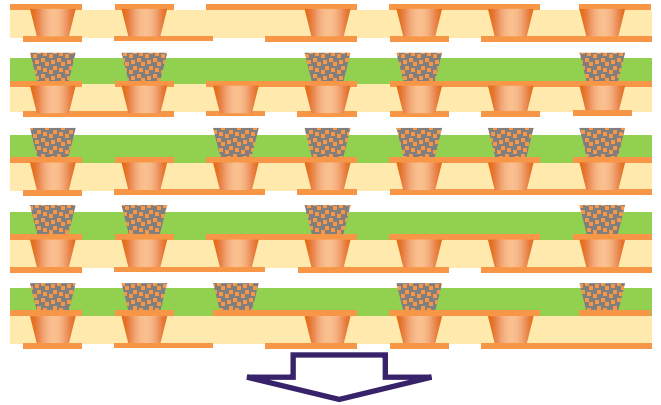
STEP-4: Via filling



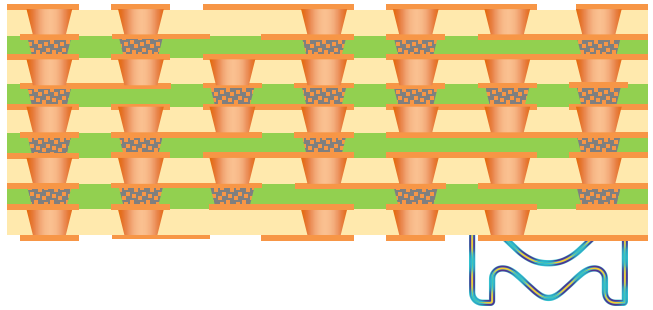
After Cover layer "PET" removal

STEP-5 : Laminate

Before lamination



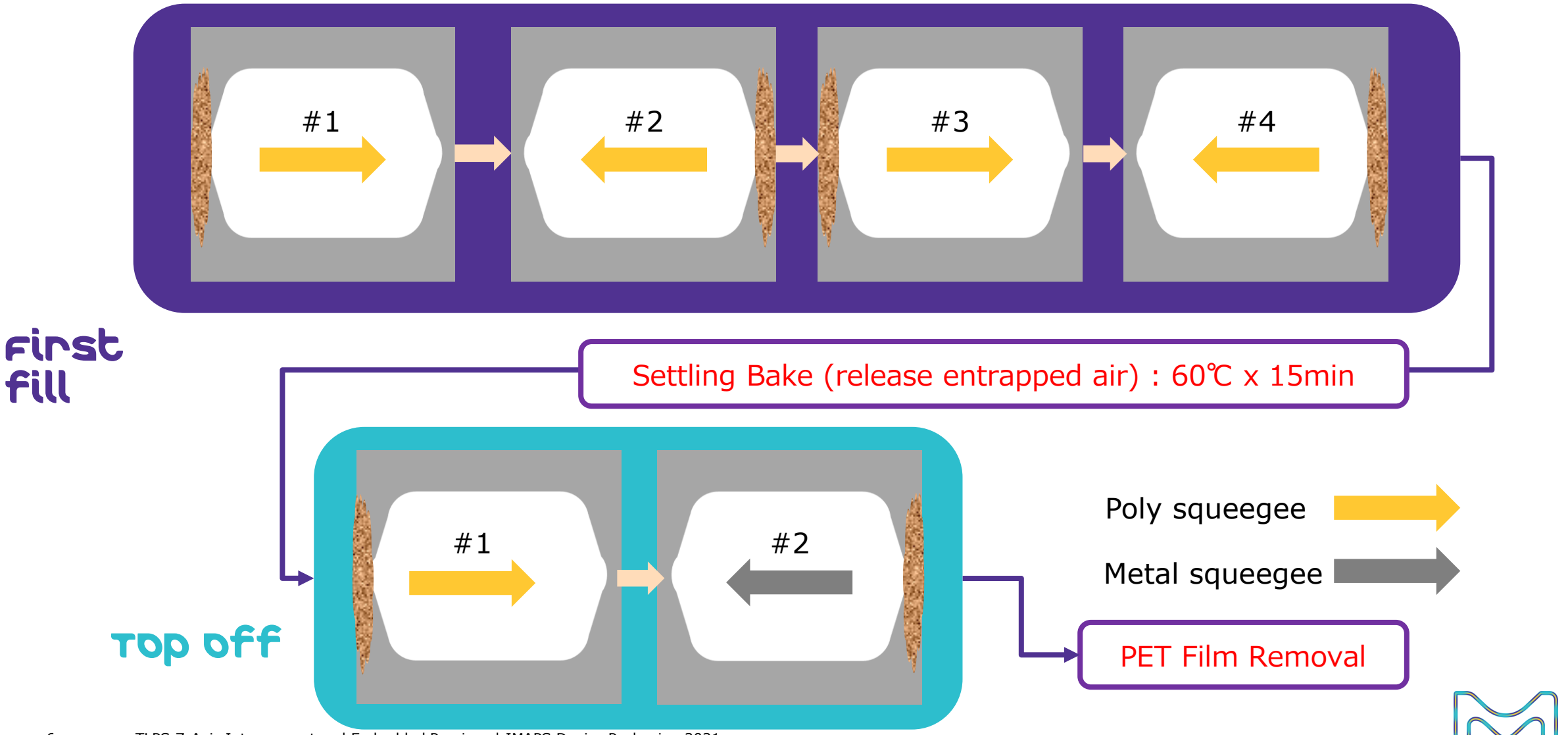
After lamination



Via filling detail

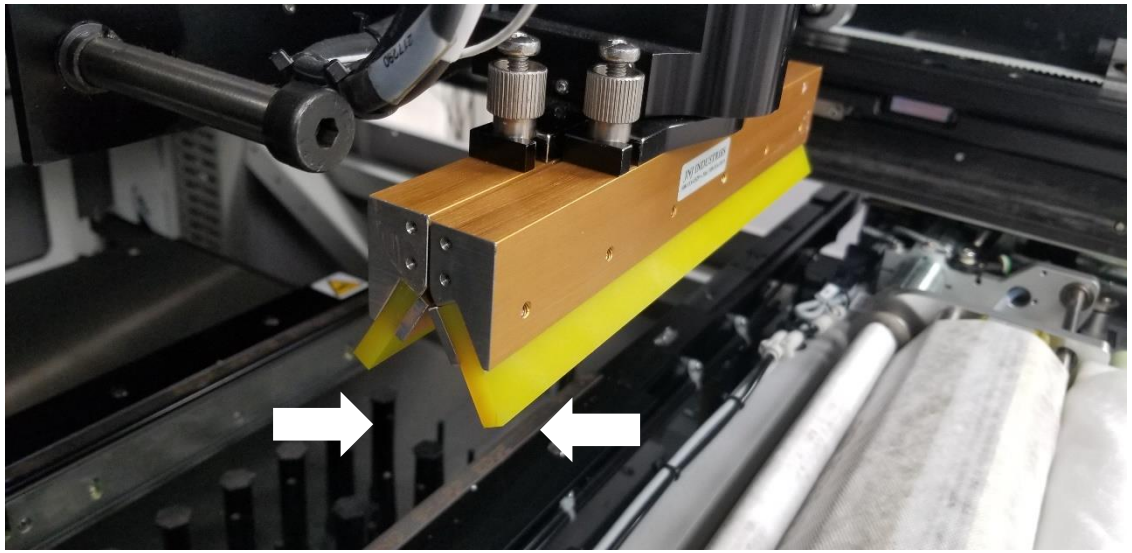
A typical fill process

Number of passes depends on aspect ratio and complexity of the structure



The tools
Example of the set-up for filling on a stencil printer

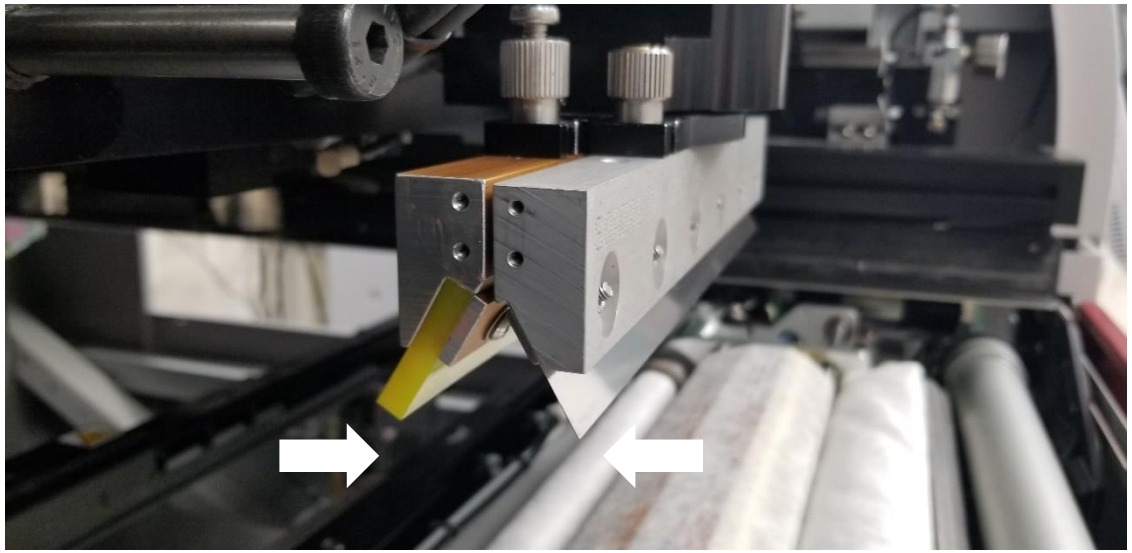
first fill



Forward
Pull ->
(#1, 3 stroke)

Return
<- **Pull**
(#2, 4 stroke)

top off

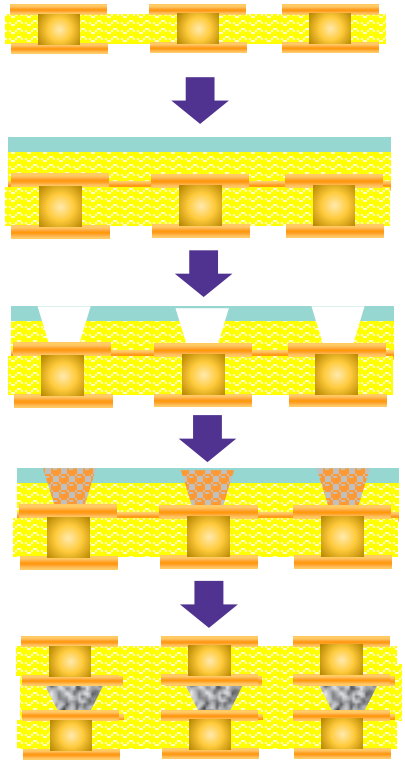


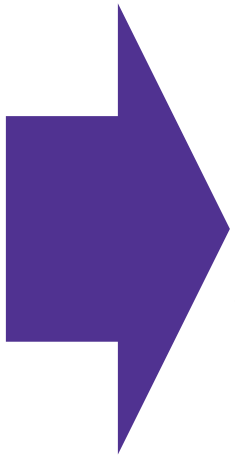
Forward
Pull ->
(#1 polymer)

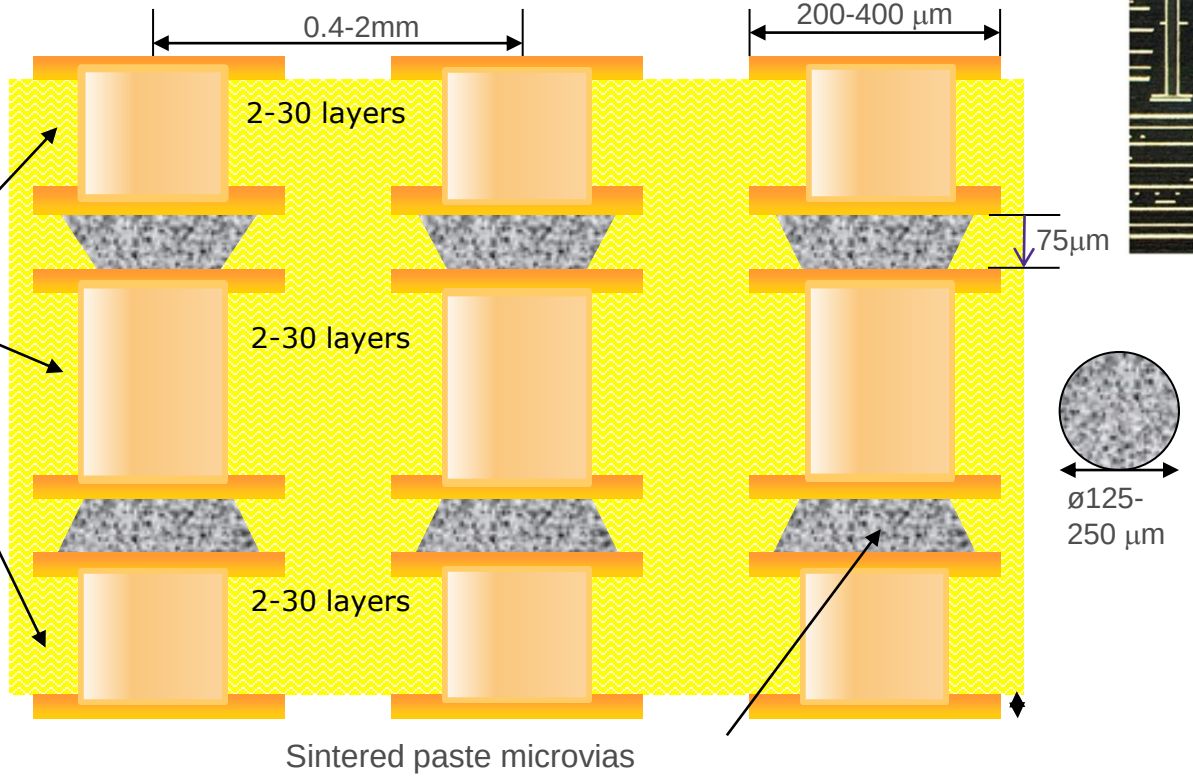
Return
<- Pull
(#2 metal)

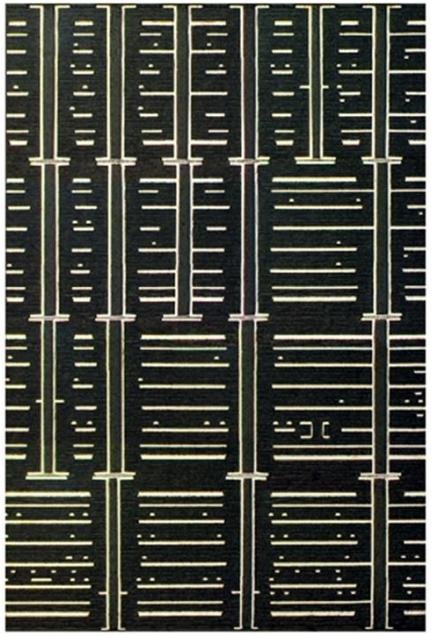
Improving yield in very high-layer-count PCB

Build sub-PCB's in high yield and connect with paste vias







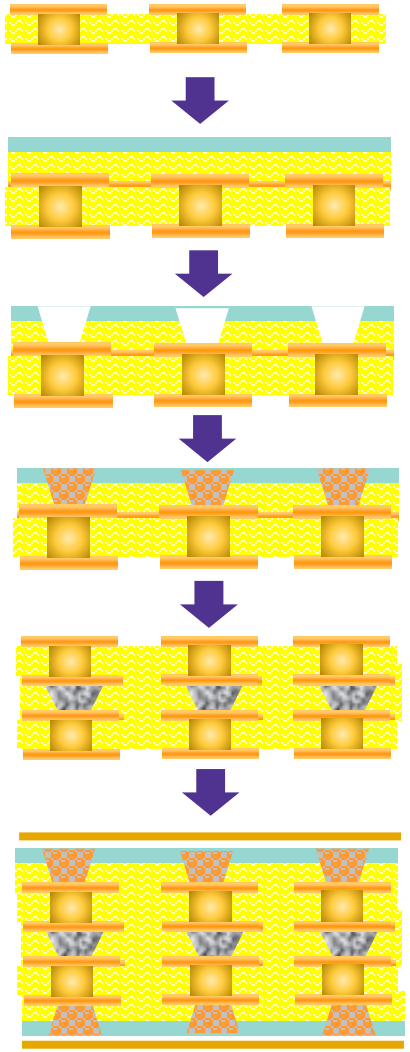


Number of layers in each 'sub-core' is variable by application

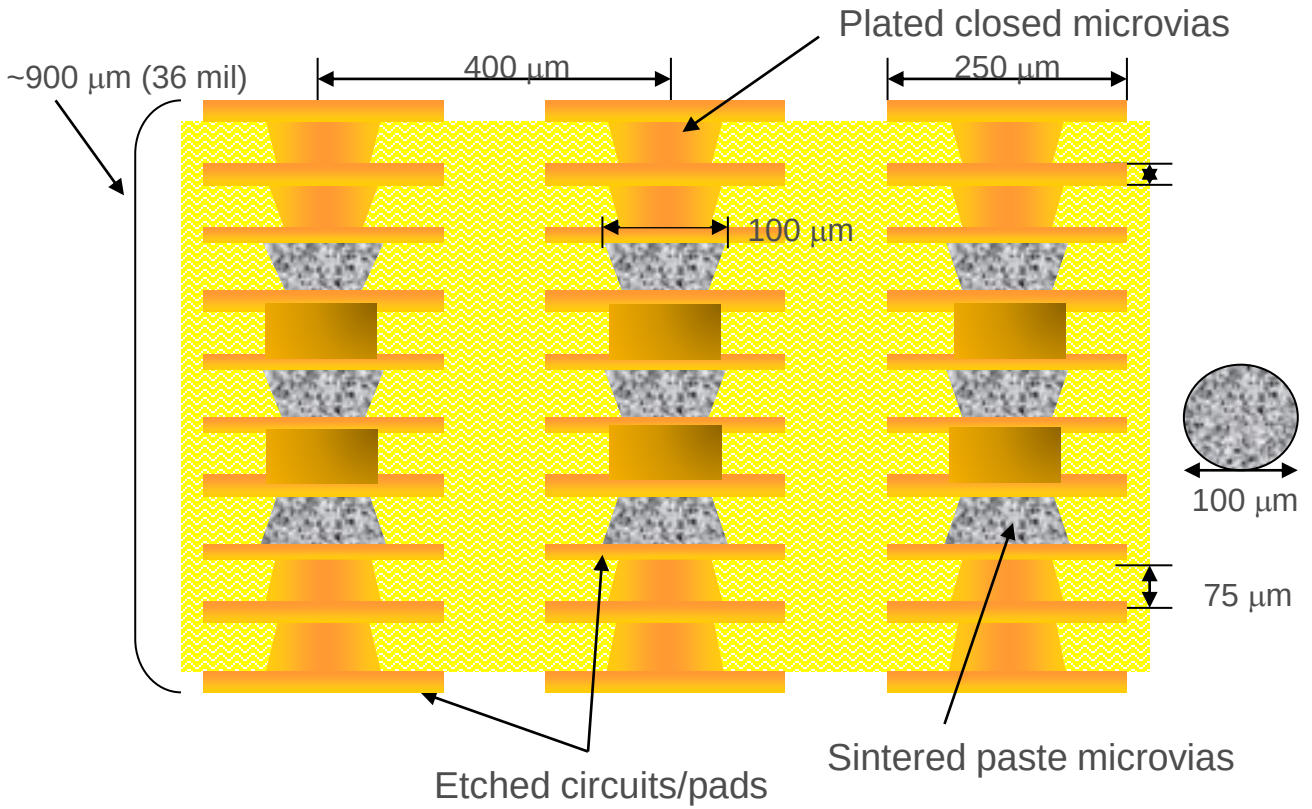
All sub-cores and via layers joined in a single lamination cycle

Can eliminate stubs

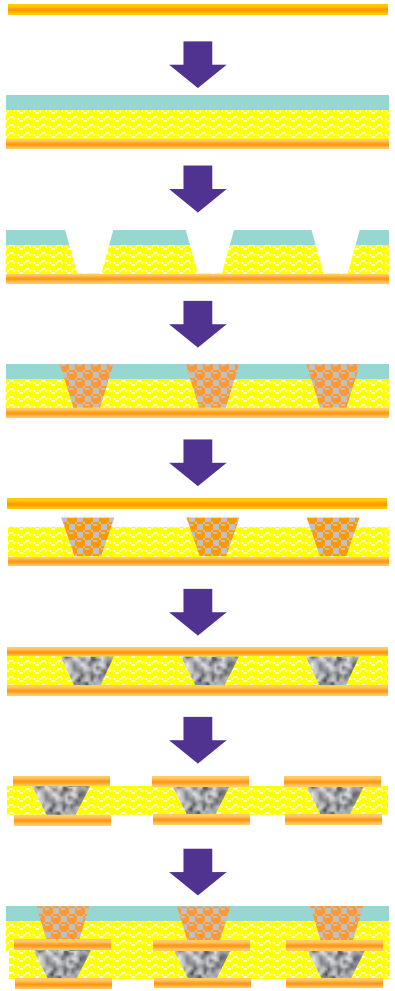
Conventional subs mixed with TLPS vias and conventional HDI outerlayer
Mix and match for reduced lamination cycles and optimum density

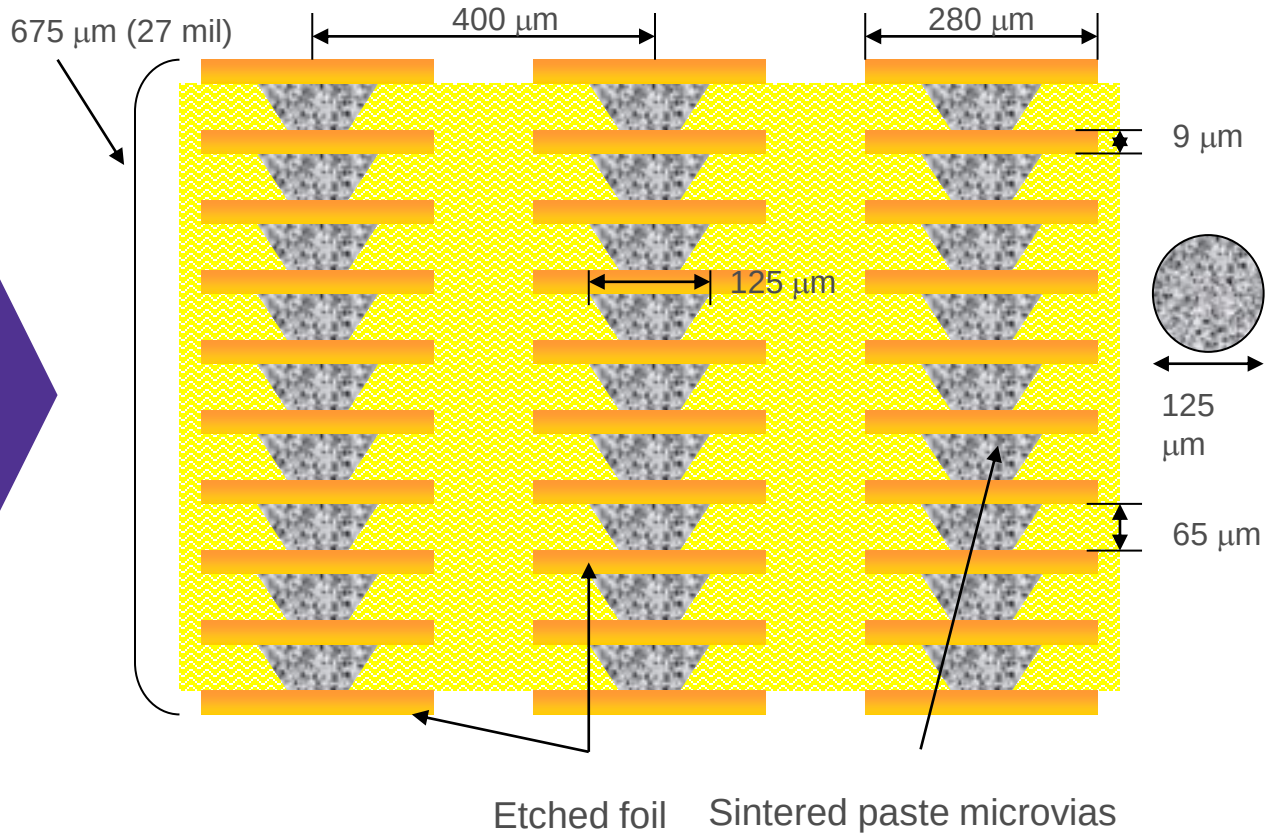


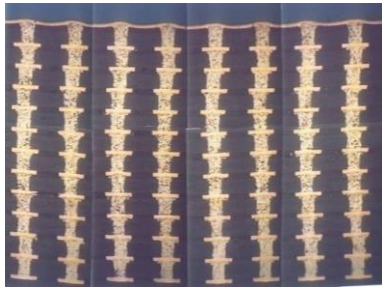
+SBU



"Any layer" interconnect for HDI applications
TLPS paste interconnects in a stacked microvia configuration





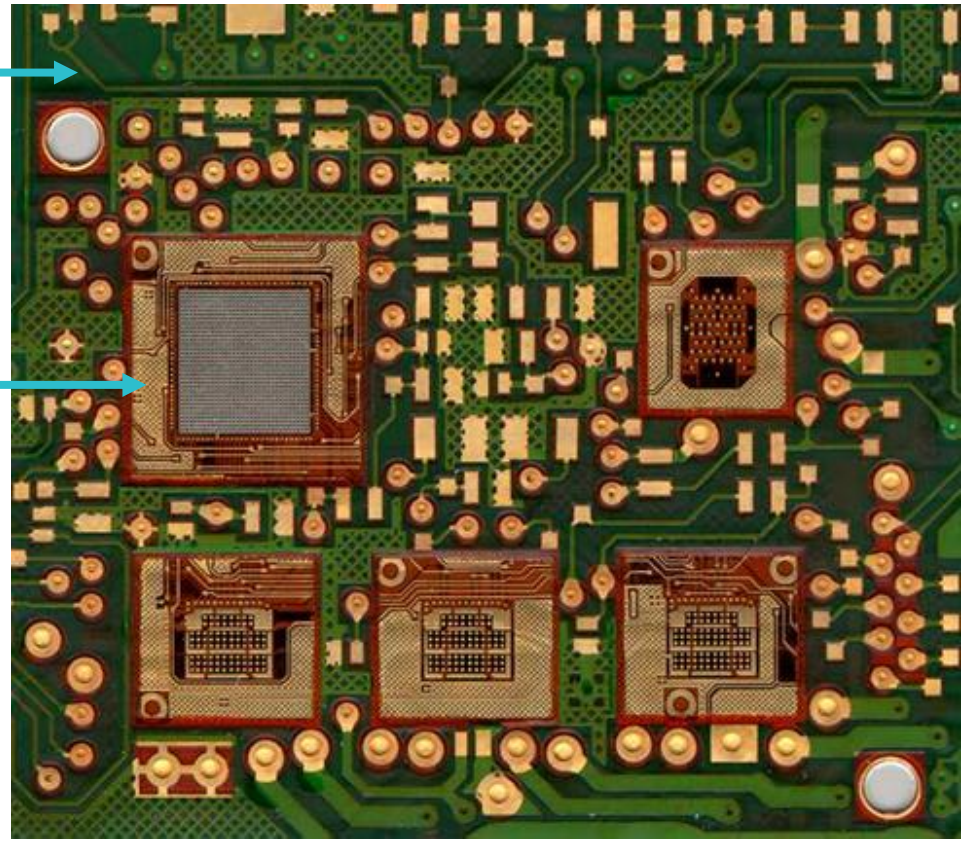


Heterogeneous integration in the PCB
“Sub-cores” joined do not need to be of the same type

- Low density to high density
- Rigid to flex
- High speed outer layers
- High frequency outer layers
- Area array to aggregator
- POP
- **Embedded components**

Low density standardized PCB

High density customized test socket

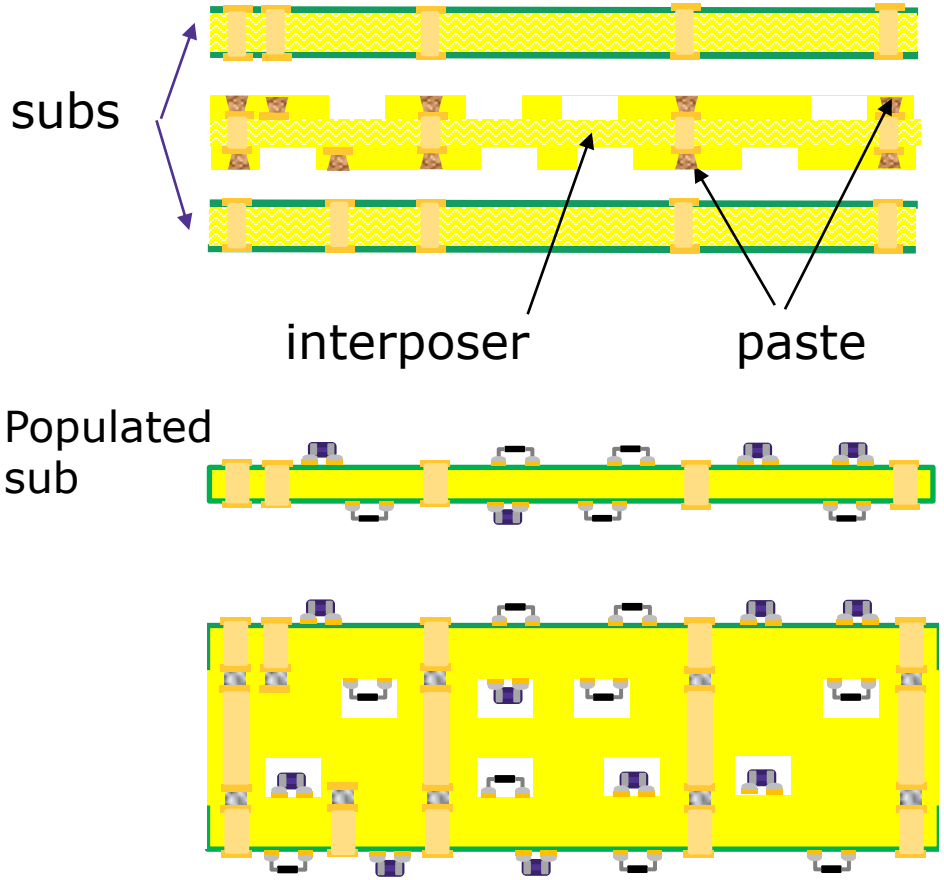


Embedded components using SMT & TLPS core-to-core

Definition:
- Components are assembled using solder or conductive adhesive
- Subs are joined using TLPS microvias

Pros:
- Sub-PCB's are fabricated in the regular fashion
- Assembly can be contracted to CEM
- TLPS replaces some PTH

Cons:
- Soldermask required if solder is used
- Reliability of prepreg to soldermask bond
- Density loss due to PTH in subs
- Remelt of solder in outer layer assembly
- Performance/reliability of conductive adhesives



Embedding components using TLPS SMT and core-to-core

Definition:

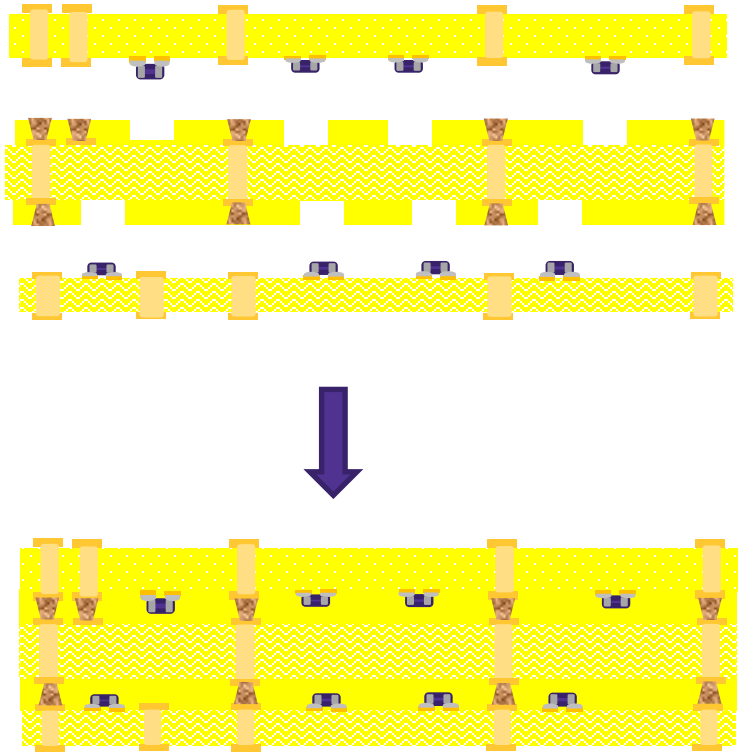
- Use TLPS solder substitutes to attach components to interior surfaces
- Join subs with TLPS microvias

Pros:

- Fully compatible with standard lamination materials
- Adhesion promotion treatments can be used on innerlayers
- No soldermasking required
- No remelt – so outerlayer surfaces can be assembled as normal

Cons:

- "Relief" routing in the prepreg must be carefully designed for the attached passives
- TLPS reflow of components may introduced shrinkage/dimensional scaling issues for subsequent lamination



Embedded components using just TLPS microvias

Definition:

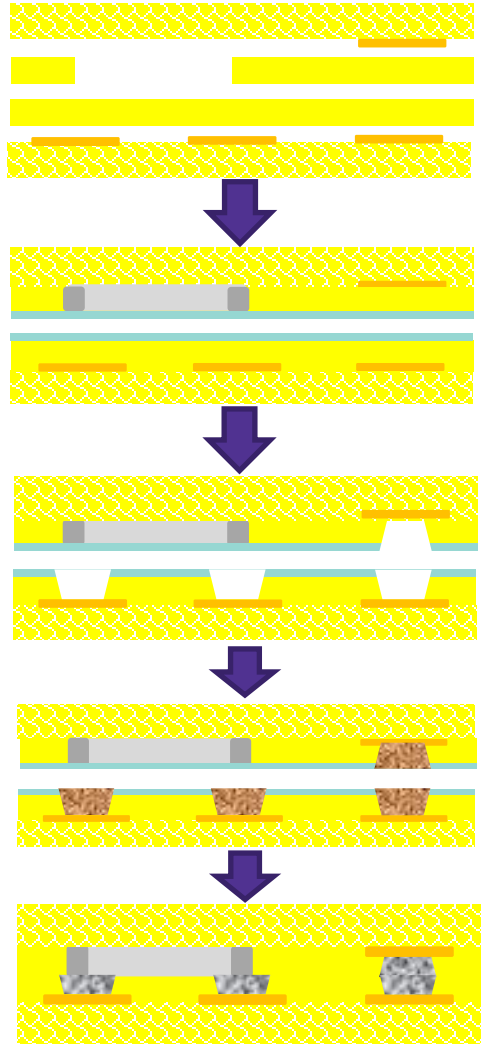
- TLPS via layers assemble components and create z-axis interconnects in a single step

Pros:

- No soldermask
- No remelt in outer layer assembly
- No PTH
- No reflow capability need by PCB fabricator

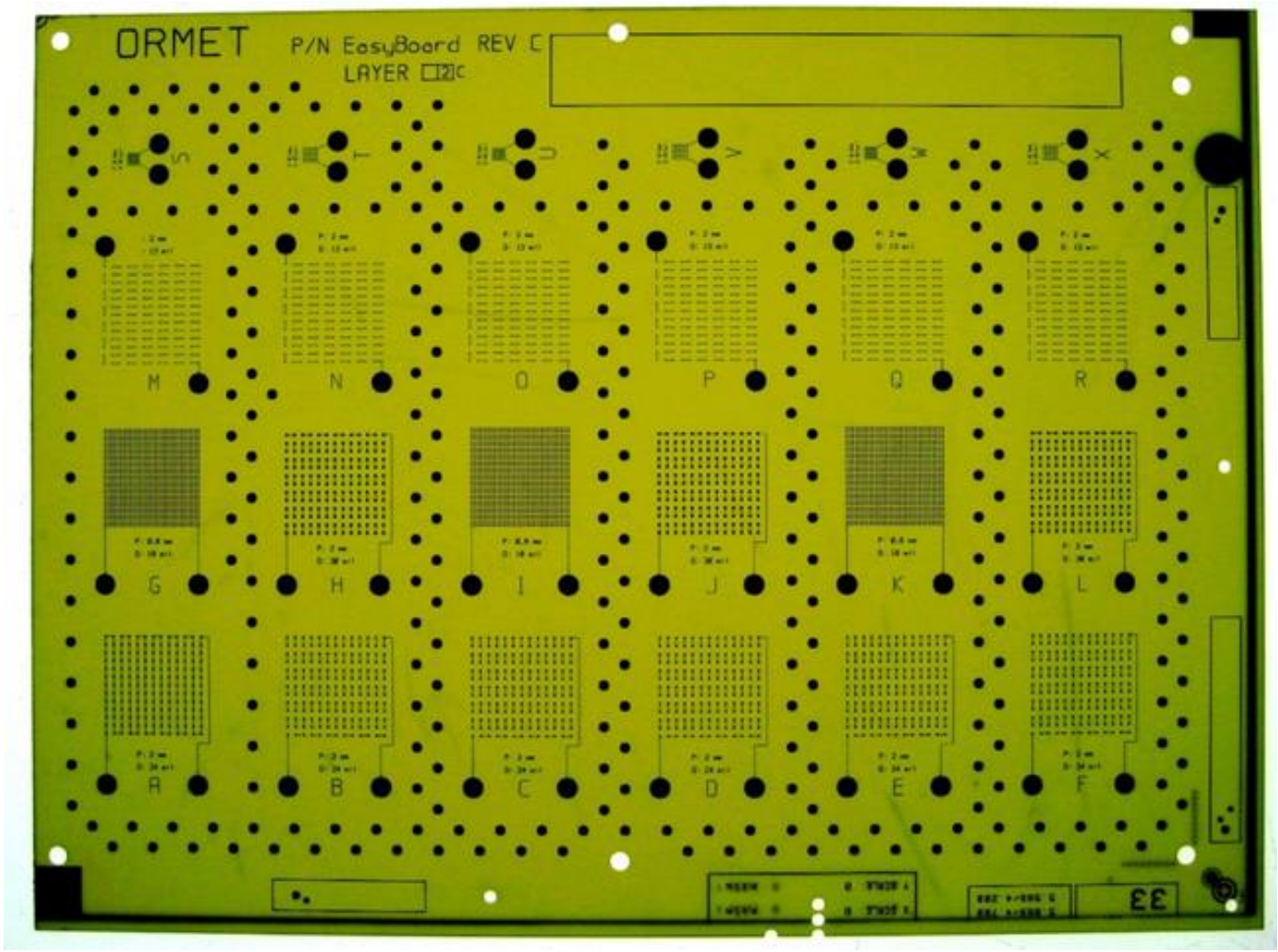
Cons:

- Prepreg needs to be similar in thickness to the passives
- Tight via pitch for small passives

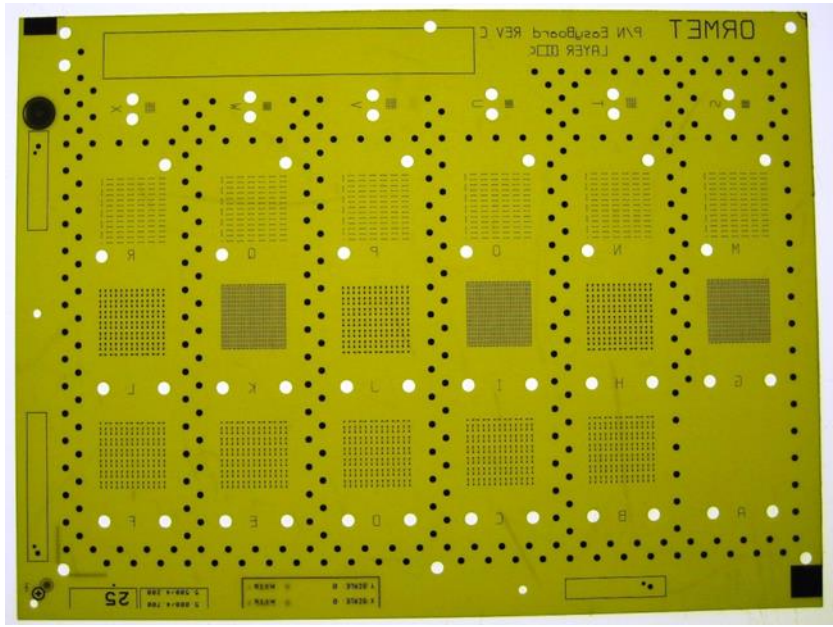


Test vehicle for embedding
Array of daisy chain connections

side 1



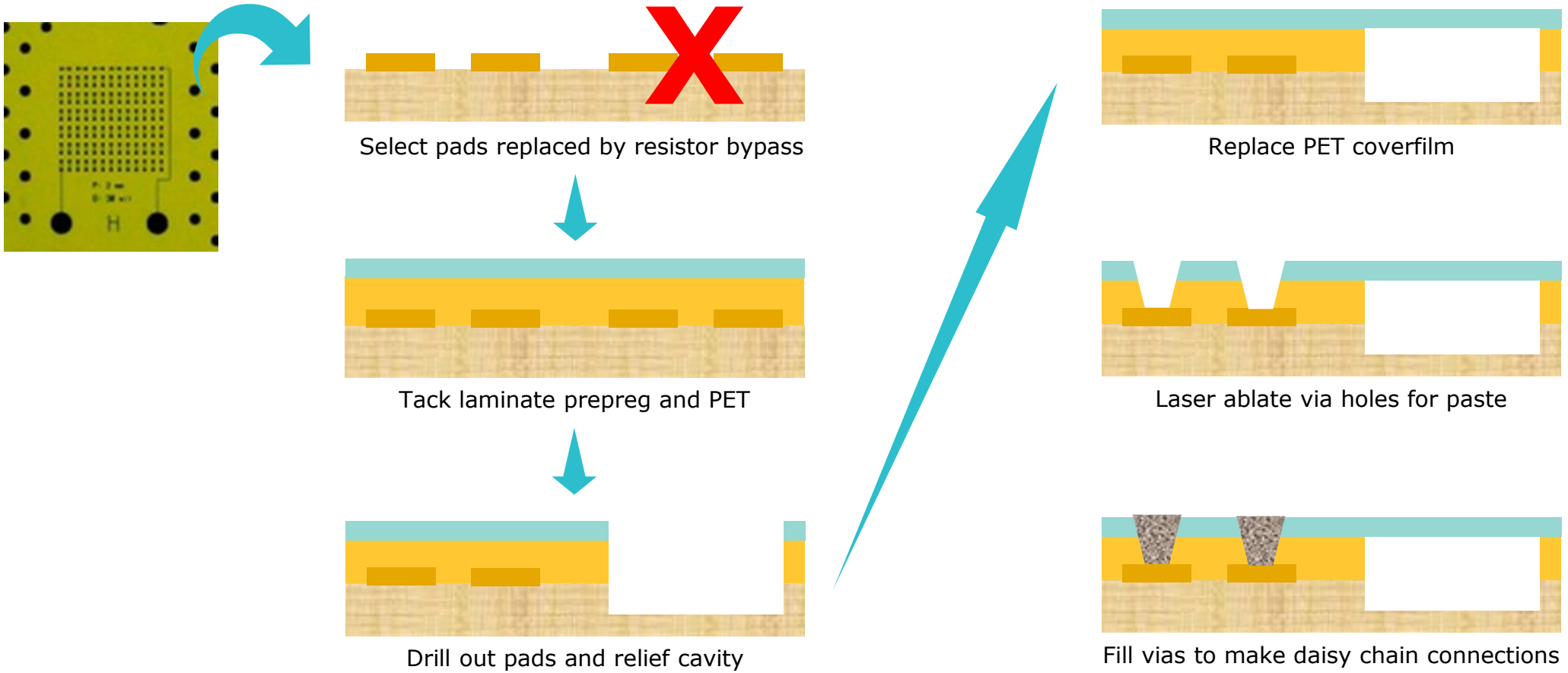
side 2



- 2mm pitch arrays are perfect size for accepting 0805 SMD resistors
- Removing the opposing pads in the resistor locations will allow electrical test

Reflow embedding vs. via embedding test vehicle

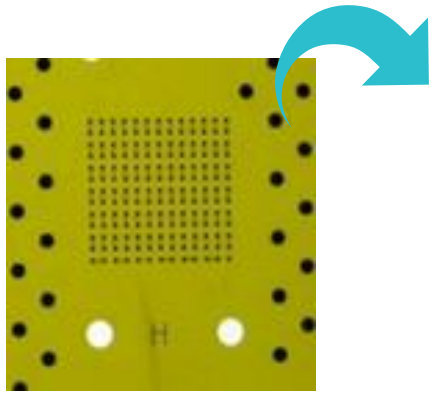
Process flow for side 1 is the same



Relief cavity preparation and installation of TLPS vias for z-axis interconnect

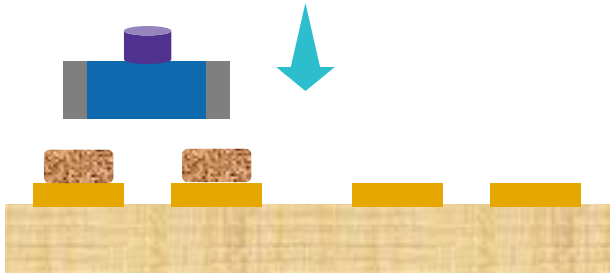
Reflow embedding vs. via embedding test vehicle

Process flows for side 2 diverge

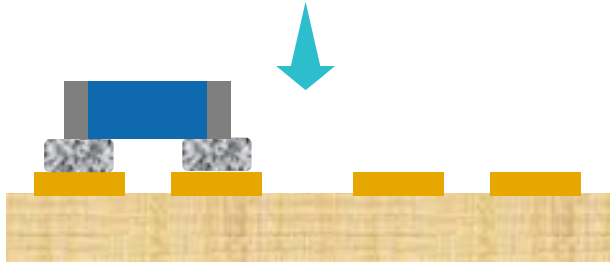


Reflow process

Stencil print TLPS reflow paste



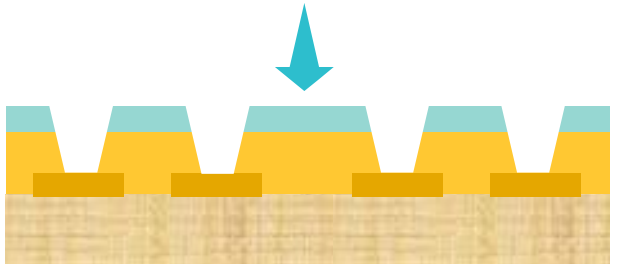
Pick and place components



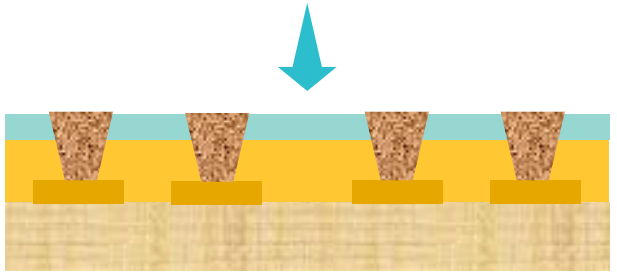
Reflow (255°C peak)

via process

Tack laminate prepreg and PET

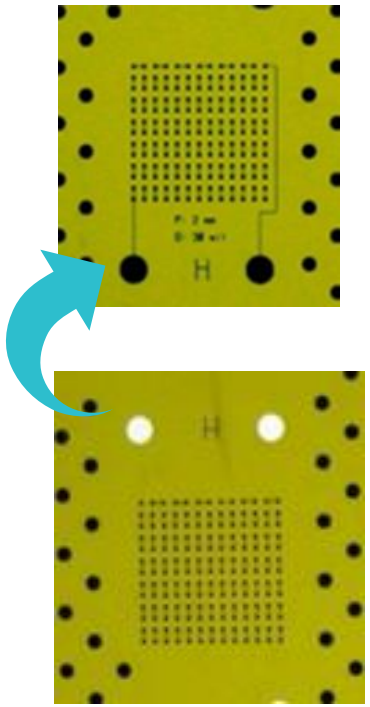


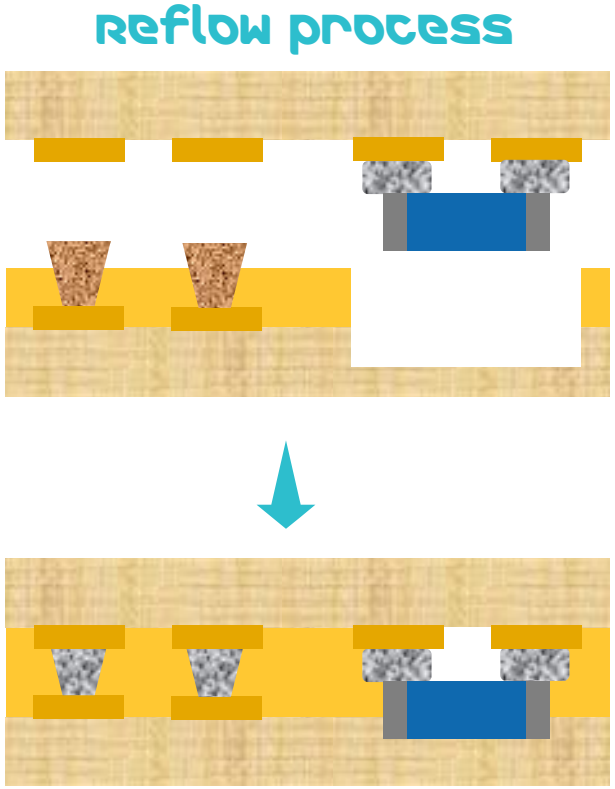
Laser ablate via holes for all connections

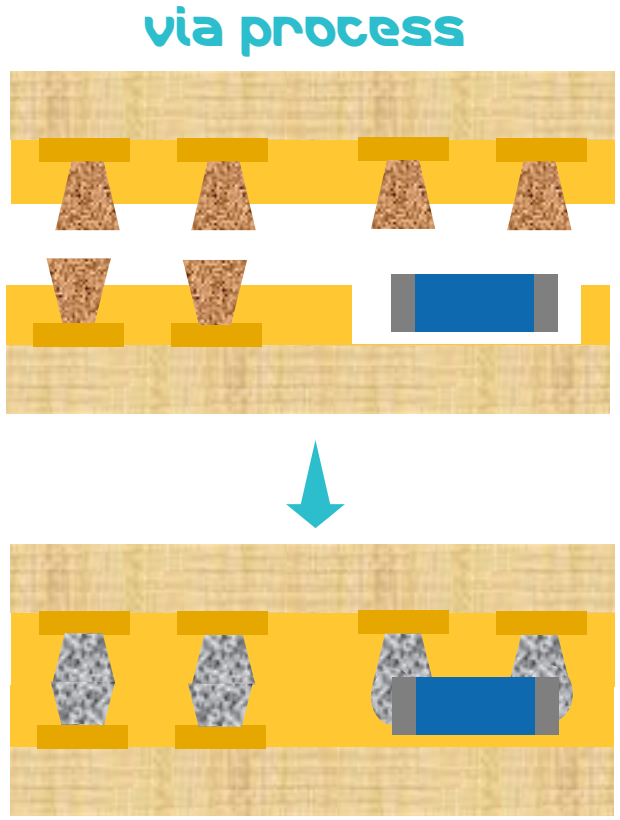


Laser ablate via holes for all connections

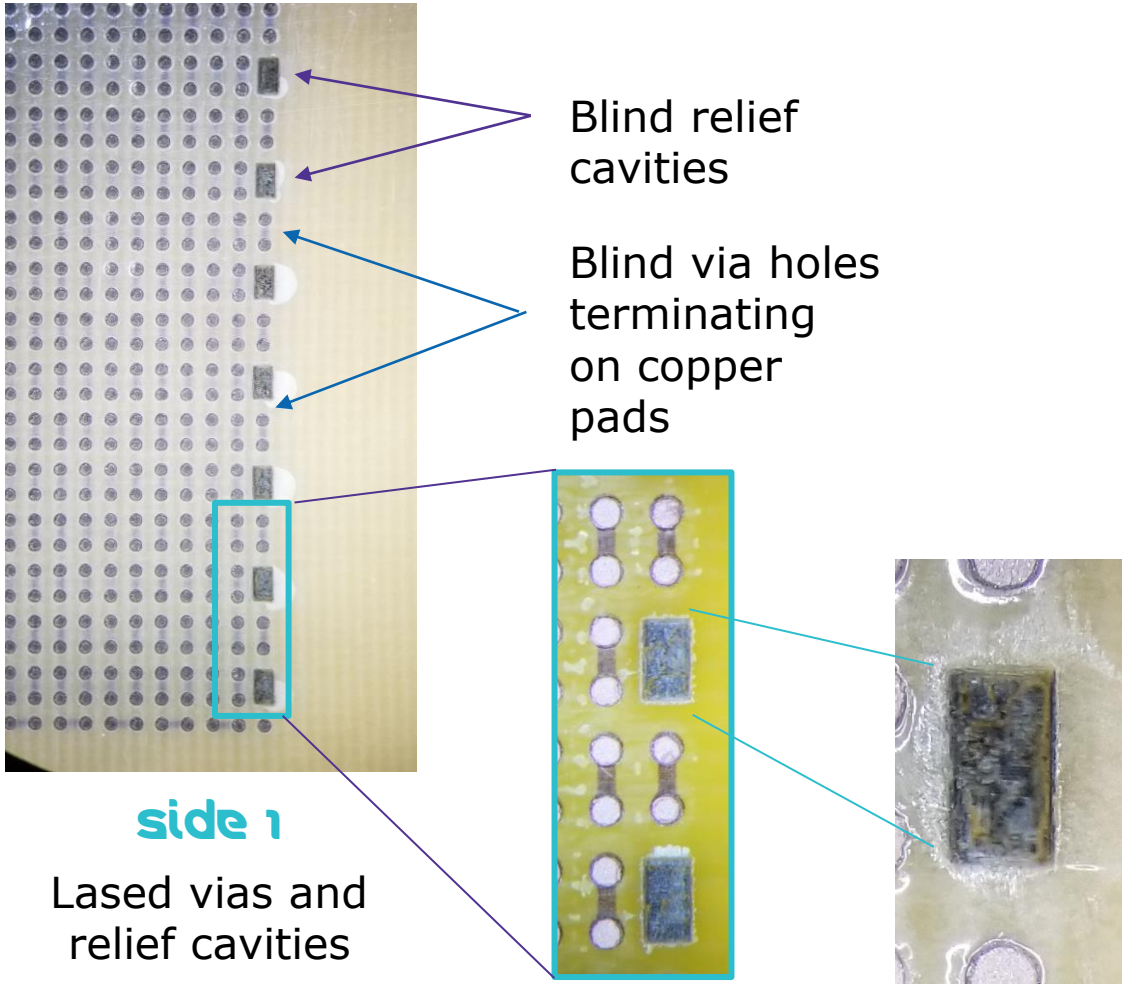
Reflow embedding vs. via embedding test vehicle
Bringing the pieces together







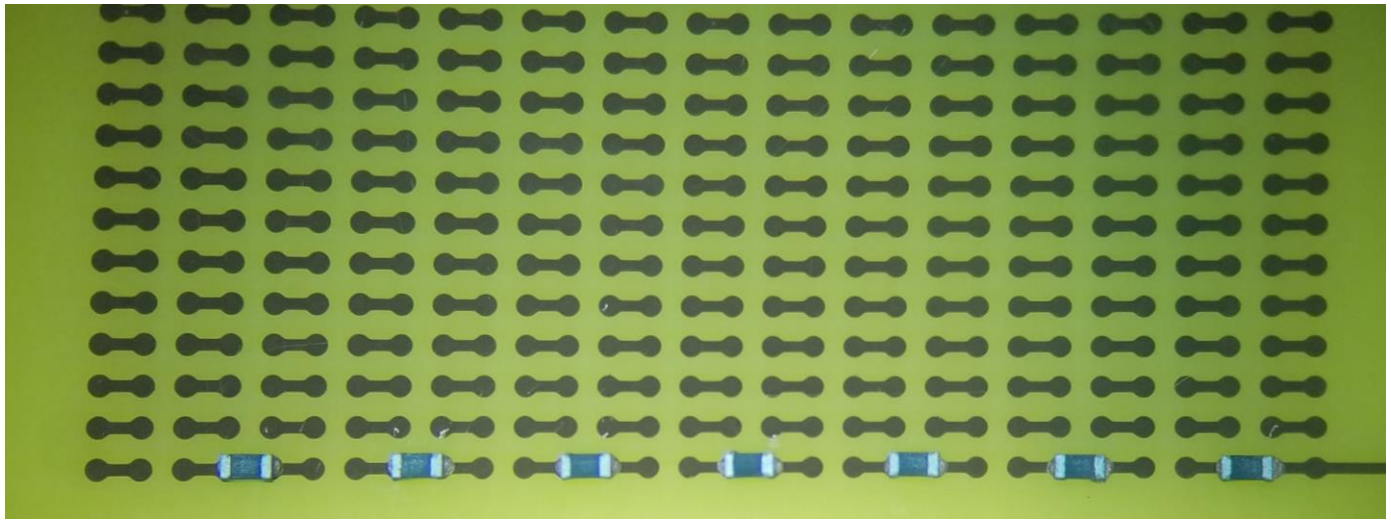
Process photos
Side 1 preparation



Lessons learned

- Mechanical machining better than laser machining for cavity formation
  - Laser locally cures prepreg
  - With pads removed there is no natural ablation stop
- C-stage could be machined and B-stage mechanically drilled prior to tacking cycle – no need to double tack the PET

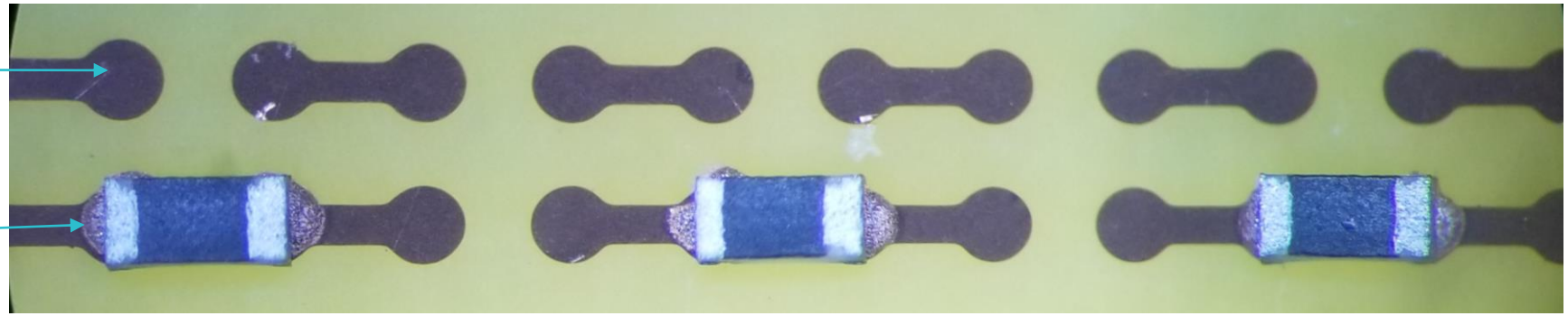
Process photos
Side 2 preparation: Reflow method



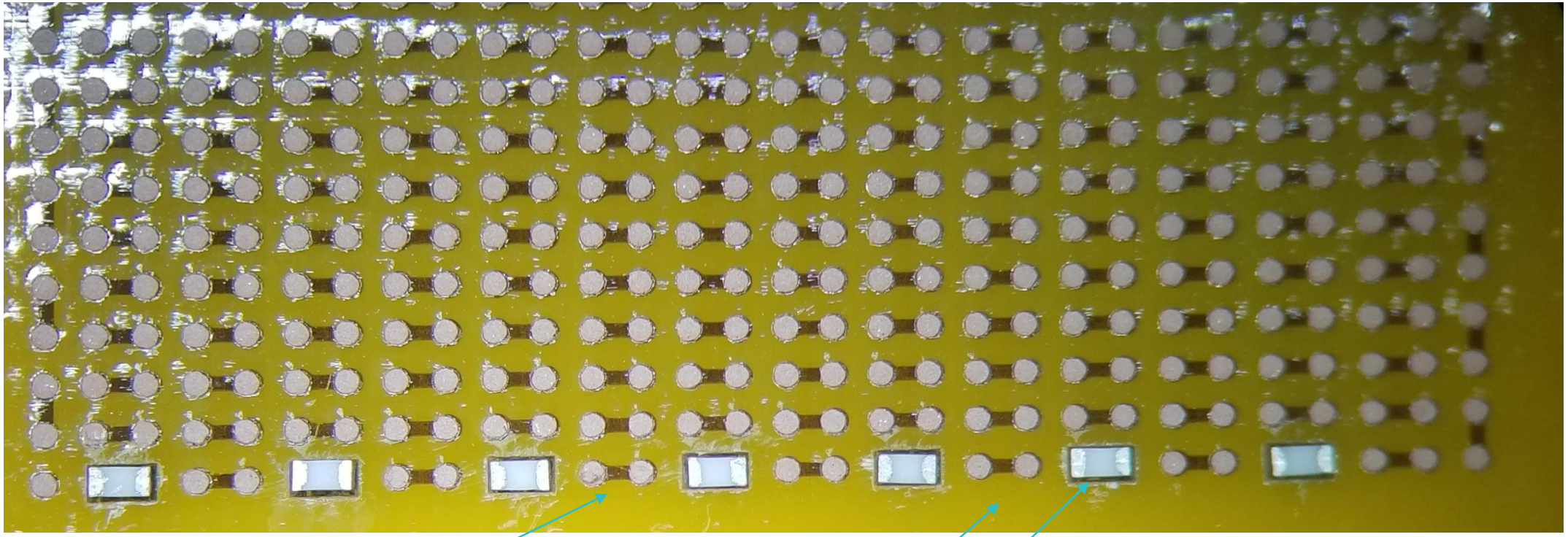
- PET film laser ablated for side 1 preparation was reused as a stencil for reflow side 2
- 25µm PET was thinner than min stencil thickness recommended for TLPS solder replacement
- 0402 chip resistors were hand-placed and reflowed using a modified SAC profile

Pad with oxide replacement coating

TLPS solder substitute

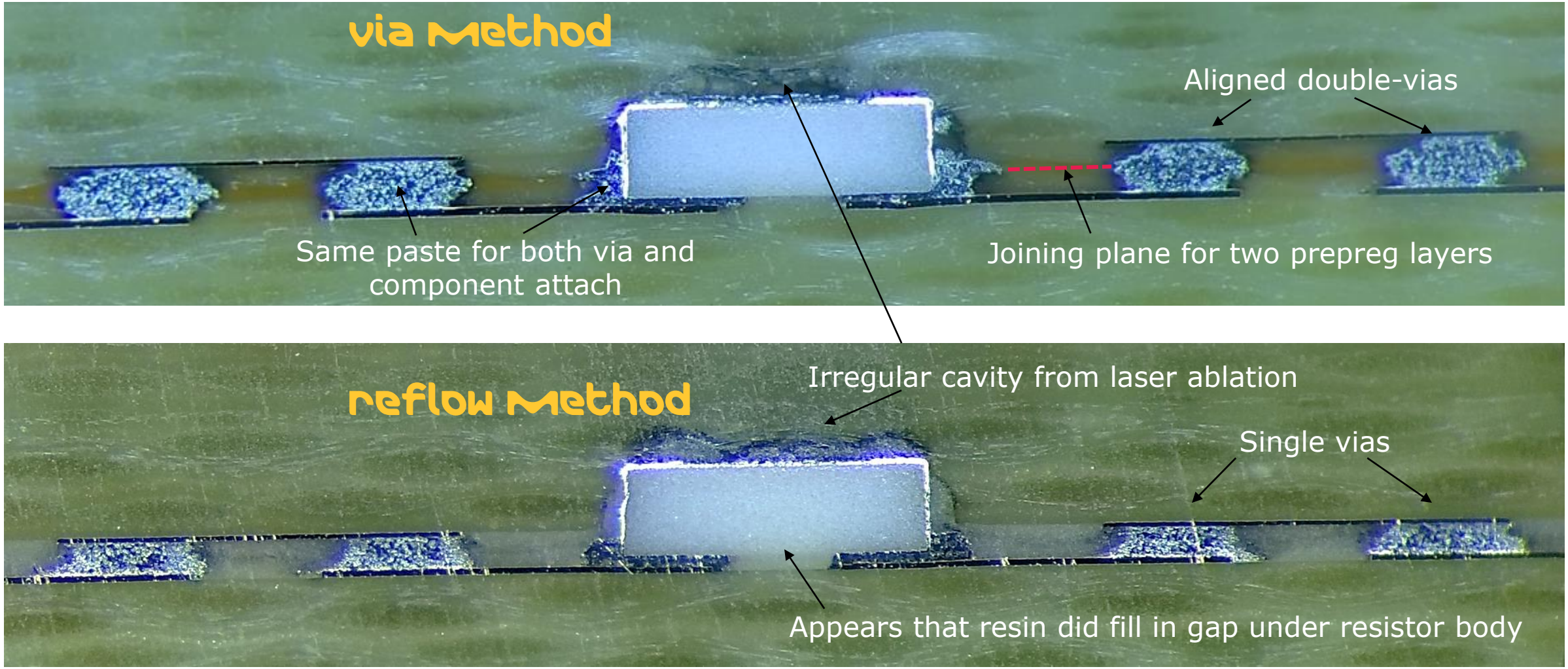


Process photos
Via method



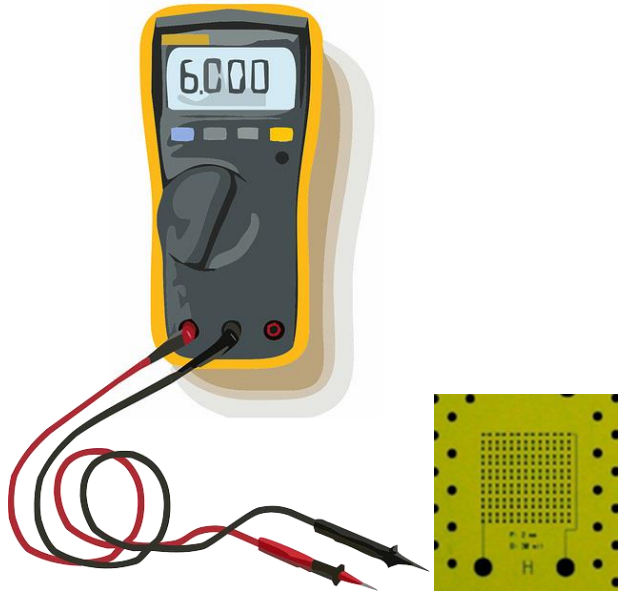
- Filled side 1 vias
- PET removed (note clean prepreg surface)
- 0402 resistors inserted into ablated cavities
  - Note: small, lightweight resistors were not inclined to stay in the cavities – some fixative scheme is needed

Cross sections
As laminated



Electrical results
As laminated and after multiple reflows

Cycle #	Via Method	Reflow Method
After 1hr. 150c Bake	2.99 Ohms	5.60 Ohms
Cycle #1	2.99 Ohms	6.17 Ohms
Cycle #2	2.98 Ohms	6.70 Ohms
Cycle#3	2.98 Ohms	6.70 Ohms
Cycle # 4	2.97 Ohms	6.66 Ohms
Cycle # 5	2.96 Ohms	6.50 Ohms
Cycle #6	2.96 Ohms	6.39 Ohms



Daisy chain

- 900 vias on 0.8mm pitch
- Pad/via diameter 450/200µm
- Zero Ω resistors replace 14 vias
- Typical resistance without the resistors: ~3Ω

Solder reflow cycle

- Forced air convection tunnel
- Typical SAC reflow profile (255°C peak)

Both types of connections survive multiple reflow cycles

Lower resistance from via method may be due to:

- Pressure assist in the sintered connection to the resistor causing low bulk resistance in the via TLPS paste
- Pressure assist in penetrating oxide replacement treatment on the copper pad – lower interfacial resistance
- More contact area between paste and resistor termination

Summary

TLPS paste provides design flexibility in advanced PCB

- Anywhere z-axis connections
- Mixed core implementations
- Embedded components at any layer

Reflow and via connection to the embedded passives

- Both appear to be viable strategies
- Mechanical formation of relief cavities would be preferable to laser
- Both yielded electrically and were stable in solder reflow cycling
- Likely due to the applied pressure during interconnect formation, the via method yielded lower and more stable resistance
  - Alignment of the double vias was excellent

thank you!