



Device Packaging 2021

Innovative PVD Technology Solutions

Advanced Substrate, EMI Shielding, & Backside Metal

Jeff Turner – Applied Materials®

March 2021



Jeff Turner

KPU Head Tango Products – Packaging Business Unit, Applied Materials

With over 25 years of experience in Semiconductor Packaging, Jeff is leading the Tango product group after acquisition by Applied Materials. He got his start in packaging as a process engineer for Semitool, specializing in electroplating and wet cleans. Post acquisition of Semitool by Applied Materials, his career transitioned into product management and then business management supporting electroplating and PVD systems in Applied's Packaging Division.



Applied Materials Acquired Tango Systems



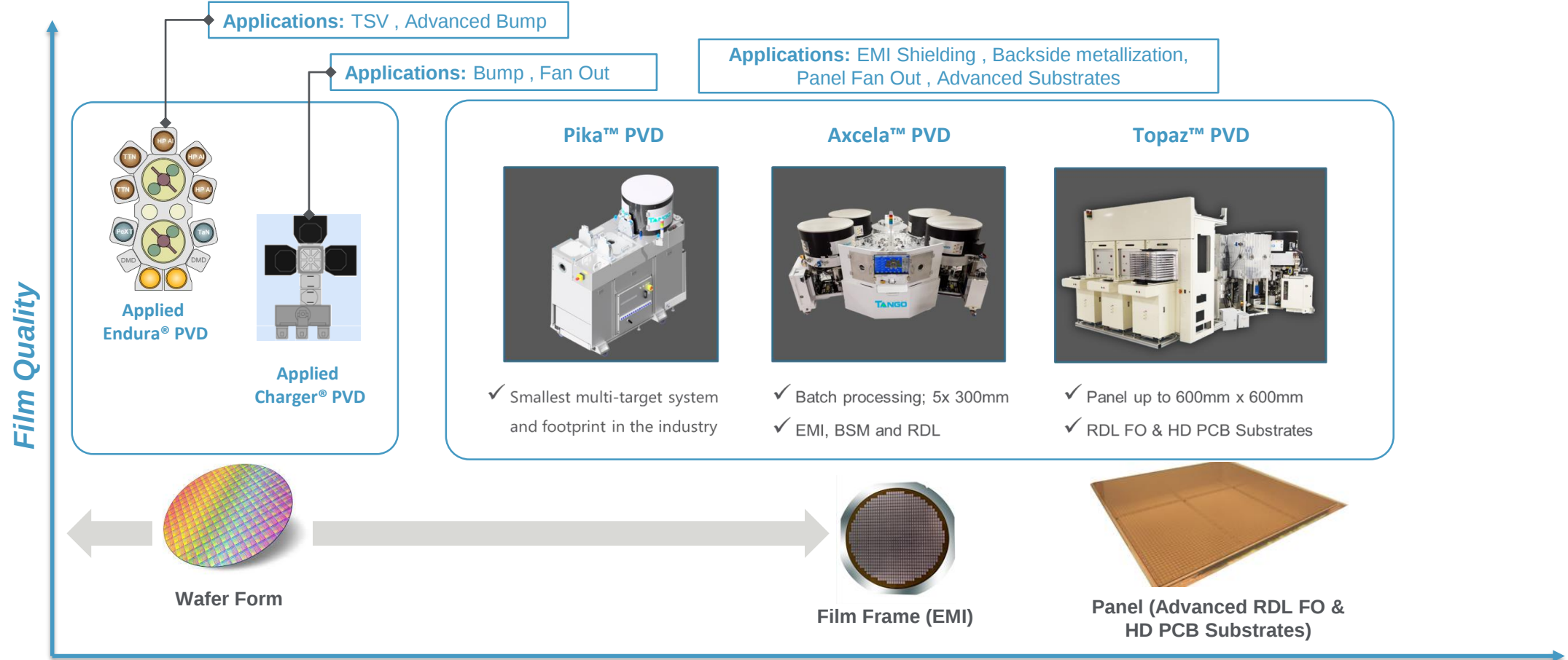
- ✓ Broad customer & supplier network
- ✓ Extensive product support infrastructure
- ✓ Broadest portfolio for Packaging products
- ✓ Largest investment in Packaging roadmap

- ✓ Flexible, high performance, & cost competitive PVD platform
- ✓ Wafer, Film Frame (EMI) and Panel
- ✓ Leading positions in EMI and Panel PVD

Leverage Applied's global footprint to better support Tango's customers
Accelerate development of technology and productivity solutions for Advanced Packaging



Tango Products Integration to Applied Materials

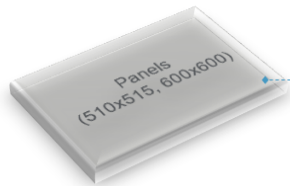


Large Area Panel Processing



Strategic Initiatives: Large Area Processing

Large Area Processing | Where we have traction



PVD : Deposition , Pre-clean
Plating : Uniformity, Coplanarity, Modeling
Wet processes : UBM Etch, PR strip, Consumable Development
Patterning : Digital Litho, Fine Line RDL , Large Dies
Disruptive Technologies : Fine Via, Laser processes, Materials
AMAT Ventures : Investments, Co-Development

TRACTION

AMAT has industry leading equipment expertise on wafer level

Areas of Strategic engagement / partnership

4 | Applied Materials Confidential



MARKETS



EMI

Fast and continuously growing application in the global marketplace for 5G: Mobile, Auto and IoT



5G DEVICES

For increased bands, antennas and filters, and higher package densities

PANEL LEVEL PACKAGING

Tango leading the way
Best in class performance

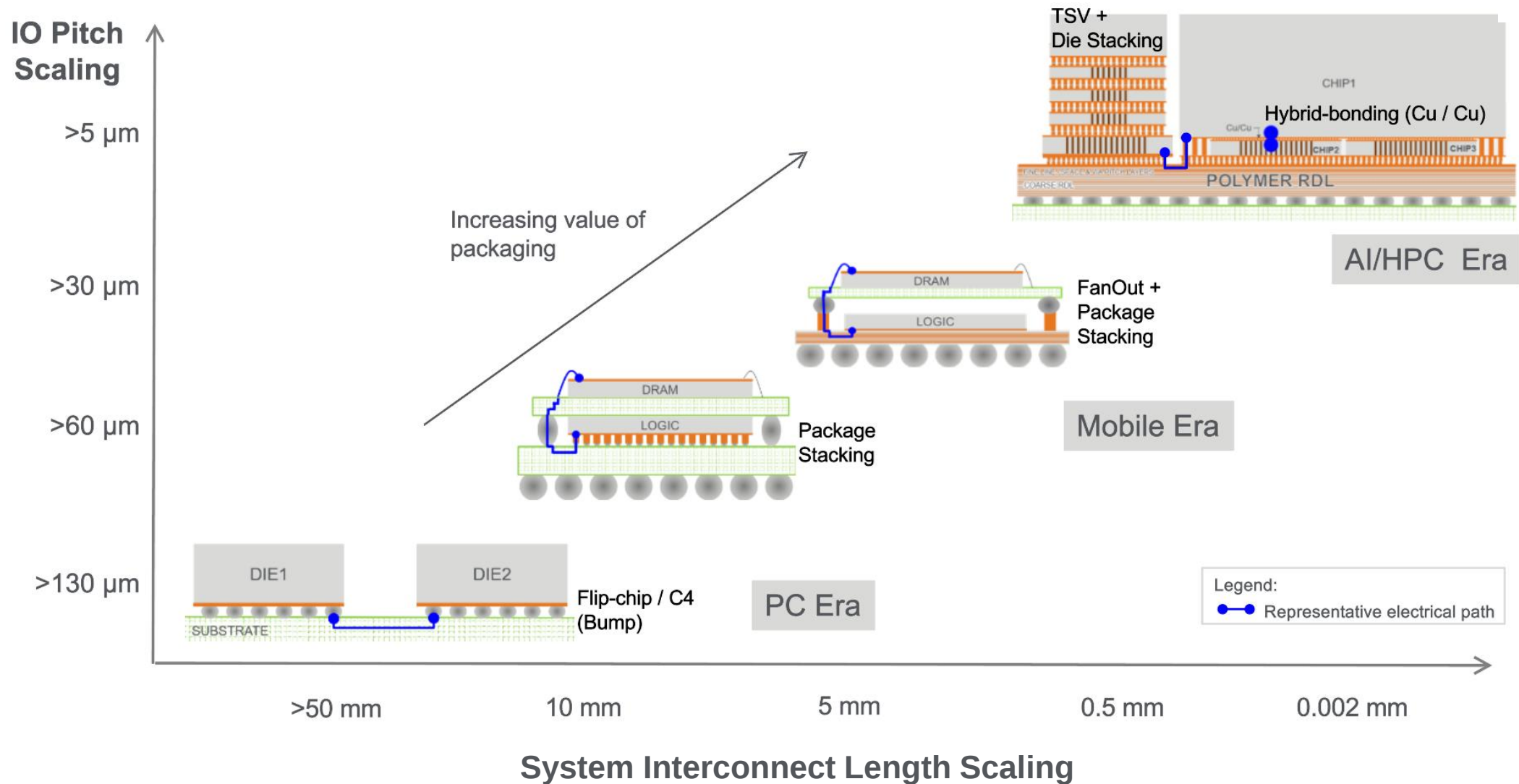


Source: Applied Materials Internal





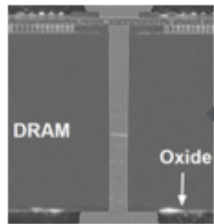
System Interconnect Scaling Roadmap



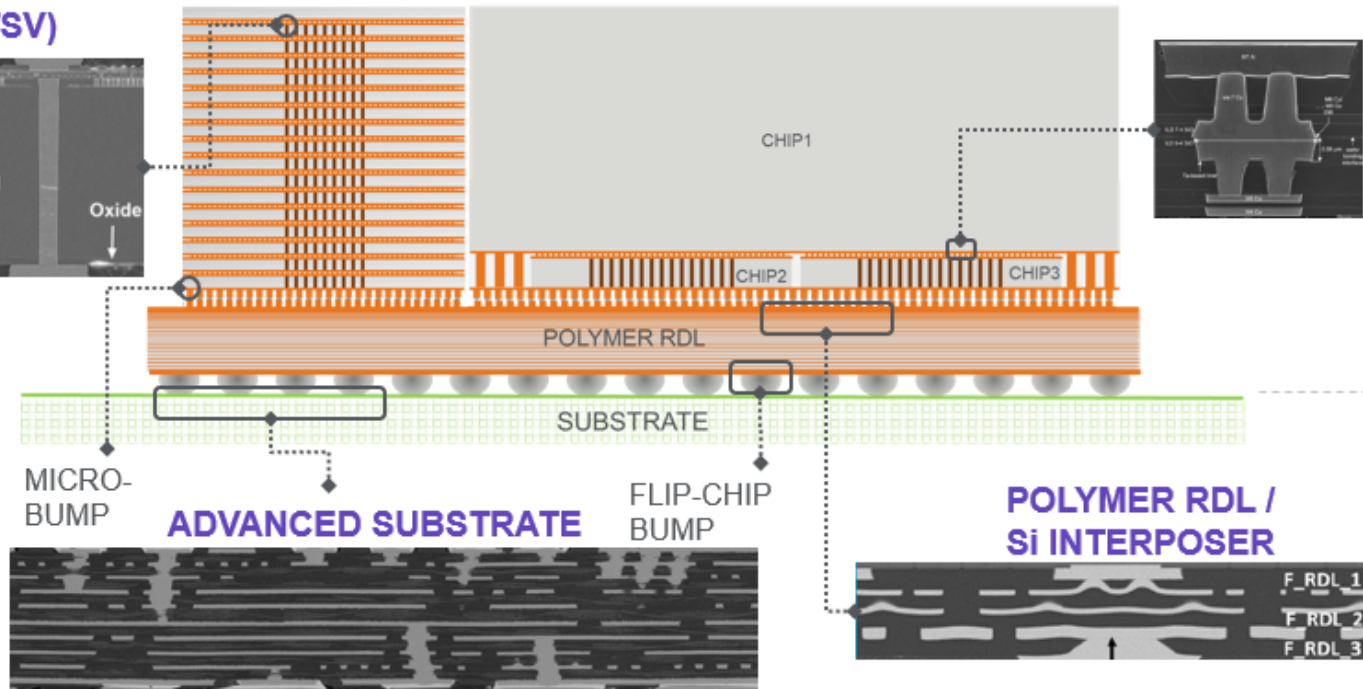
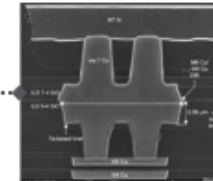


System Integration with 2D & 3D Interconnects

THRU SILICON VIA (TSV)



HYBRID BONDING



3D Interconnects

- Thru Silicon Via (TSV)
- Hybrid bonding [\[Emerging\]](#)

2D Interconnects

- Redistribution layer (RDL) (Bump, bond-pad)
- Advanced substrate [\[Multiple Platforms Emerging\]](#)

Broad technology portfolio and ability to deliver integrated solutions for both 2D & 3D





Panel PVD Applications, Materials, & Equipment

- Panel Applications
 - ▶ RDL
 - ▶ BSM
 - ▶ EMI Shielding
- Panel Materials
 - ▶ ABF (Ajinomoto Build-up films)
 - ▶ Glass
 - ▶ Molded Compound
- Equipment: Topaz™
 - ▶ Panels up to 600mm x 600mm
 - Frameless handling
 - Glass carrier handling for panels
 - ▶ Automation: Warped Panel Capability
 - ▶ Semiconductor grade capable processes
 - Degas, Preclean, Deposition



Applied Material Topaz™



Topaz™: Wafer Grade Capability in Panel Form



Load Lock Degas

- ▶ Multi panel load lock
- ▶ Increased degas capability in LL

Staged Degas

- ▶ Multi panel batch degas
- ▶ Heating capability
- ▶ Moisture monitoring for process control



Preclean Chamber

- ▶ ICP preclean technology
- ▶ Process temperature control <120C
- ▶ Contaminant control for superior Rc performance
- ▶ Enabling superior adhesion strength

PVD Chamber

- ▶ Ti or Cu deposition
- ▶ Process temperature control <120C
- ▶ Uniform film deposition
- ▶ Capability for high AR vias

Fully automated high throughput low cost of ownership operation



EMI Shielding

EMI: Advances in Shielding Technology

Dr. Harrison Chang, Vincent Chen, USI at SEMICON West 2013, Edited



- Bulky
- Not possible for high functional devices

Metal Cans

- Worked well
- Mech structure

1990s-2006

- Not effective shield
- High Overall cost
- Quality issues

Spray Shields

- Easy to implement
- Low capital costs
- Low temperature

2007-2013

- Large Footprint
- High Overall cost
- Contact Resistance
- Adhesions challenges
- Temperature

Inline Sputter

- Better shielding

2013-2015

- Higher Capital cost

Cluster Sputter

- Small Footprint
- Low cost of ownership
- Low Contact Resistance
- Best Adhesion
- Best in class for high and Low frequency shielding

From 2015

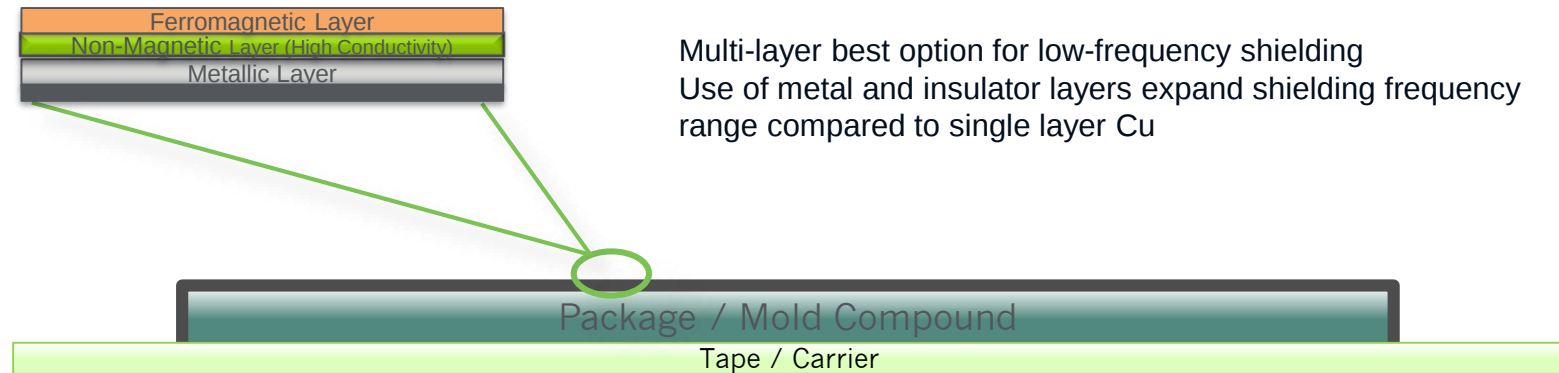


High & Low Frequency Shielding Scenarios

High Frequency



Low Frequency





5G Shielding Requirements

- Lower contact resistance
 - ▶ 100X improvement required
 - ▶ 1-2 ohm to 0.01-0.02 Ohm
 - ▶ Less Noise required for 5G

- Higher Step Coverage
 - ▶ Package thickness increase >0.8mm
 - ▶ Addition of Antenna on modules
 - ▶ Coverage > 40% for lower CoO

- Higher Conductivity
 - ▶ Higher conductivity to reduce shield thickness
 - **Tango™ <4um** Vs **competition >5um**

Rc Specification Trends

	5G	4G	3G
Rc Spec (Ohm)	0.02	0.20	2

Applied Rc Performance

Contact resistance
as low as
4.5 mOhm!!



Contact Resistance (mOhm)	
Measurement	Tango
Min	4.5
Max	4.6
Ave.	4.6
St. Dev.	0.01





EMI Platform Comparison

Attribute	Axcela™	Inline Tools	Axcela™ Key Differentiators
Contact resistance	1X	10X	10x Lower Rc performance
Adhesion	> 5B	≤ 4B	Best in Class (Mold/Si/Exposed Wires)
Required deposition thickness	1X	1.5X	Small dense grains; requires less deposition to achieve device performance
Process Temperature & Control	Low	High / Unstable	Eliminates thermal budget concerns
Sputter Materials	Ti/Cu/SUS/Ni/Nife/Co	Ti/Cu/SUS	Capability to do both High & Low Frequency Shielding
Package Type	BGA/LGA/STRIPS/DSBGA	LGA/BGA	Preferred vendor of choice for all 5G products
Footprint (m2)	1X	3X	3x Tools in same Clean room space
Uptime	Modular = > uptime	Full system down for PM	Modular cluster, one chamber is down for PM - others running production

15

Axcela™ – The best choice for today and extendibility for next generation requirements



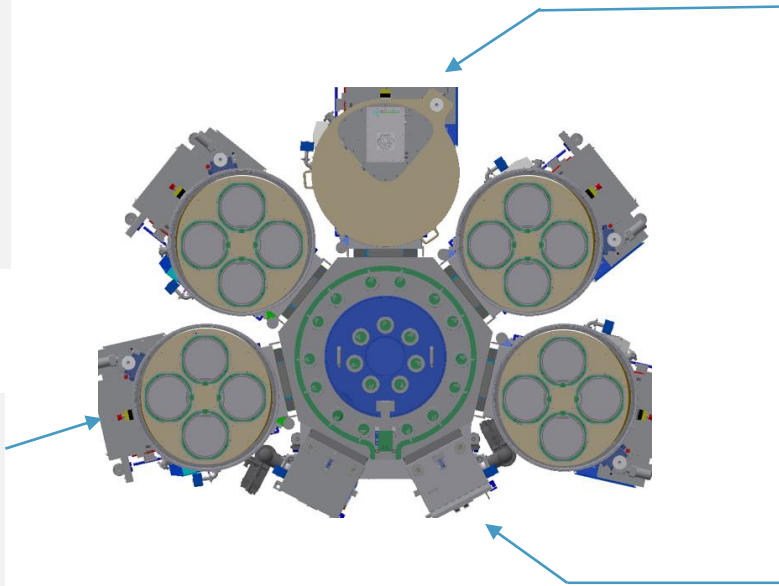


Axcela™: Industry Solution for EMI

Axcela - 7

- Batch processing system
- 4 – 5 carriers/chamber
- Up to 4 PVD chambers to enable highest throughput and lowest cost of ownership
- Semiconductor based architecture for exceptional process performance & control

Axcela 7



Multi-Target & Multi-Frame PVD

- ▶ Up to 3 targets per chamber
- ▶ Co-sputtering of multiple films in same chamber
- ▶ High throughput & low operation cost

Multi-Frame Preclean

- ▶ ICP preclean technology
- ▶ Process temperature control <120C for low temp etching
- ▶ Combination of Bias / Source for high etch rates & throughput
- ▶ Enables superior adhesion strength & Rc performance

Load Lock Degass

- Multi frame load lock
- 380mm/350mm/330mm Film Frames
- Batch degas process for moisture removal

Source: Applied Materials Internal

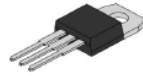


Backside Metal (BSM)

Power Devices

- Controls electrical energy from source to the load according to load demand at high efficiency and with outstanding reliability

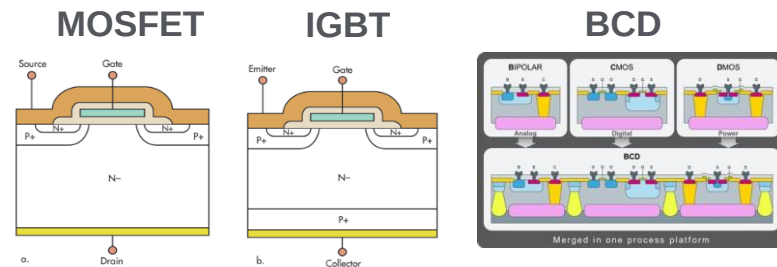
- Discrete Power Die (single die)



- ▶ IGBT: Med/High V → Automotive ; Energy ; Industry
- ▶ MOSFET: Low/Med V → Consumer-based ; Computing & storage

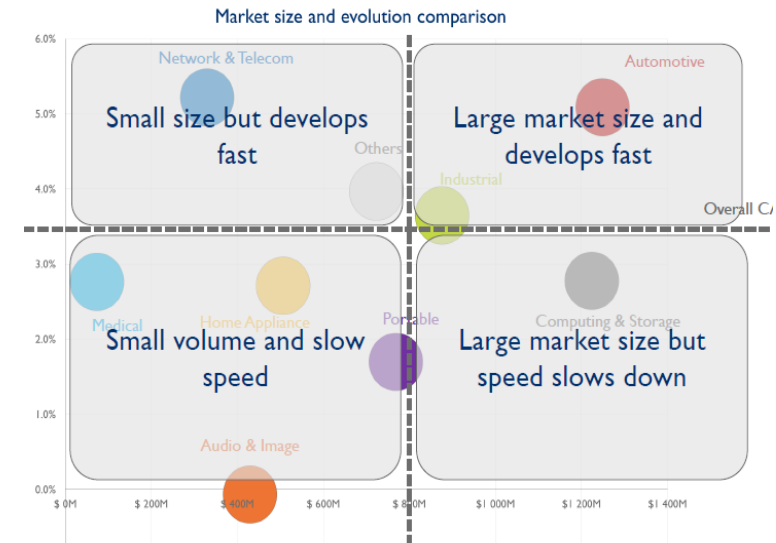
- Power Module (several dies)

- ▶ Inverters → renewable energy and EV



Demand Drivers:

- Climate change / Environmental Issues
 - EV/HEV
- Arrival and expansion of data era
 - Smartphones, AI, Autonomous Vehicle, 5G network, IoT



Source:

<https://www.electronicdesign.com/power/are-you-kidding-harvest-power-rust>
2018 Power Market Yole report , BCD Technology - STMicroelectronics



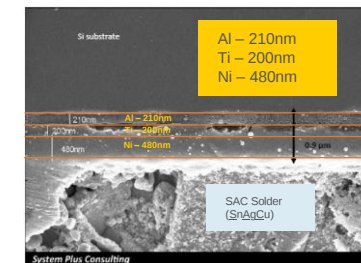
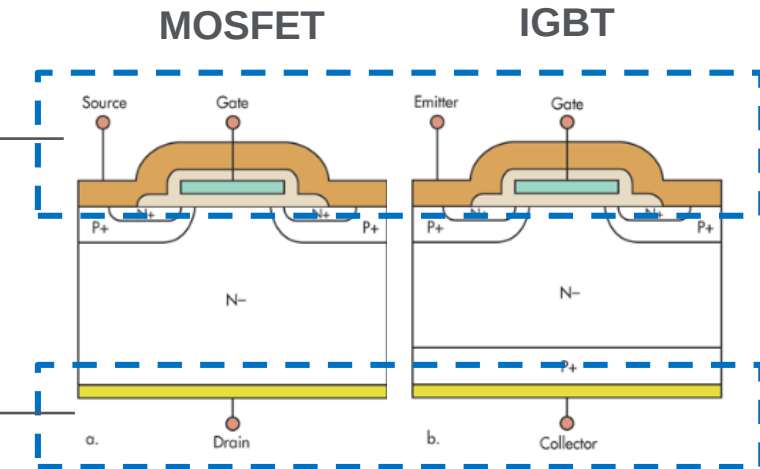
Power Device Metallization

■ Frontside Metallization: Thick Al

- ▶ Thick layer for high current carrying capability
- ▶ High thermal load

■ Backside Metallization: Al, Ti, Ni, NiV, Au, Ag

- Create ohmic contact between Si-solder metal stack interface
- Improve thermal management of the chip
- **(Ti, Al)** → Seed layer to Si forming ohmic contact
- **(Ti)** → Barrier and adhesion layer
- **(Ni, NiV)** → Solder layer (reacts easily with common soft solders)
- **(Ag, Au, Au alloys)** → protection/solder layer (prevent oxidation)
- Also used in HPC



Source:

<https://www.electronicdesign.com/power/are-you-kidding-harvest-power-rust>

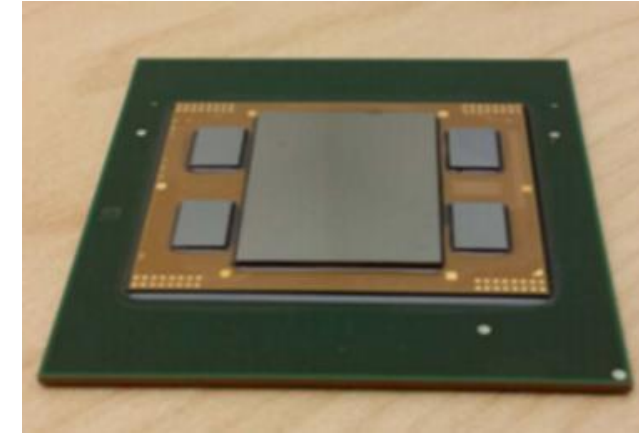
Teardown: Techinsights

Infineon SJ MOSFET

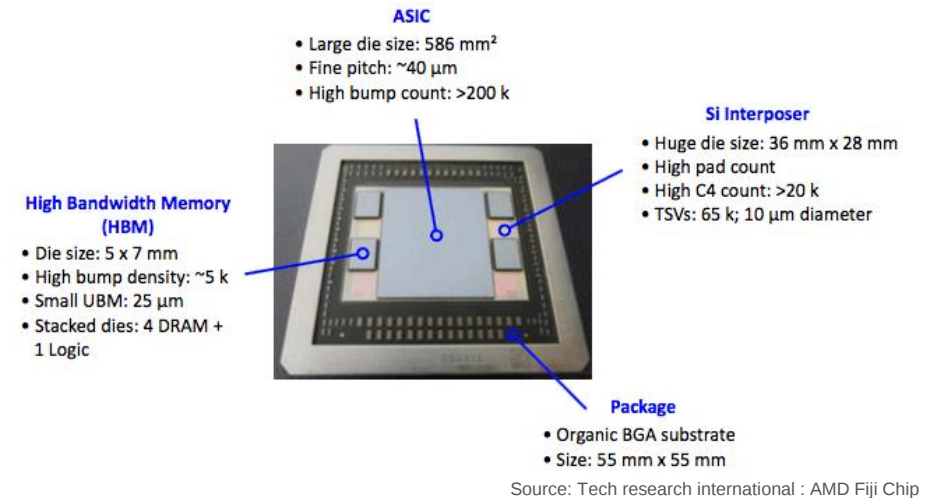


Backside Metal on 2.5D Packages

- Capabilities to do BSM at Package level with Tape and Film Frame Handling
- BKM's Developed for film stack stress optimization and adhesion performance
- Demonstrated Ti/NiV/Au film stacks on Packages with exposed Dies
- Capability for low temperature control of Package



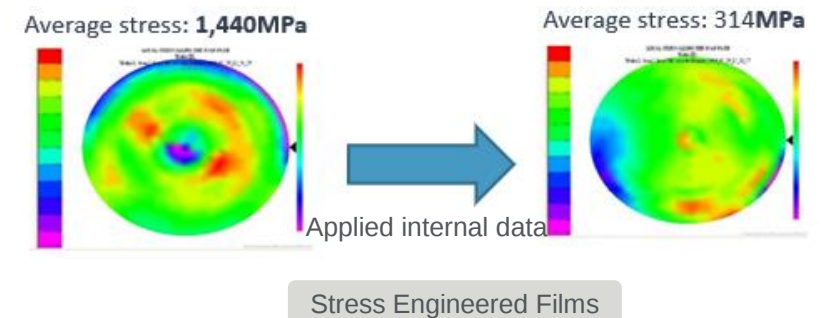
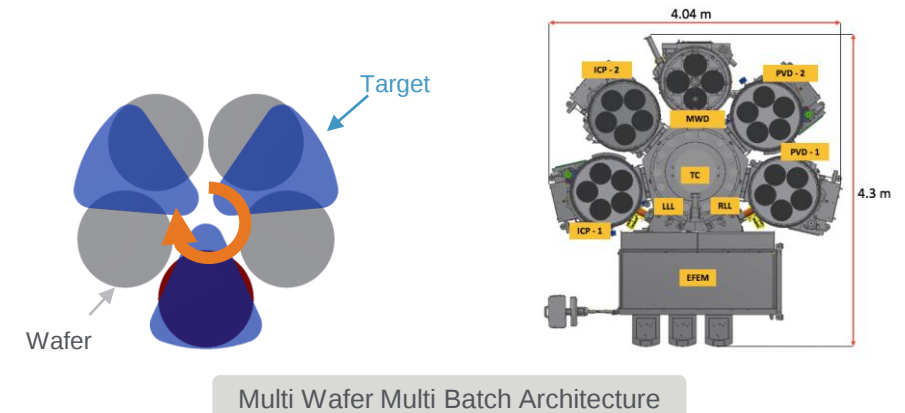
Source : Li, Li, et al "3D SiP with Organic Interposer for ASIC and Memory Integration," Proc 66th Electronic Components and Technology Conf, Las Vegas, NV, June 2016, pp. 1445-1450.



Axcela™ for BSM



- Lower cost batch process to enable low COO requirement
 - Multi film Dep in same chamber
 - Multiple material capability: Al, Ti, Ni/NiV, Au/Ag
- Flexible Architecture
 - Taiko / Glass Bonded / Tape ring Handling solutions
- Wafer handling solutions
 - Wafer flipping in FI
 - No Bevel/backside deposition
 - No Front side Contact
- Low thermal Budget <120C
- Stress engineering & control to meet application needs





Applied Materials

Your Partner For Technology Advancement | Packaging

