17TH INTERNATIONAL CONFERENCE ON • APRIL 12-15, 2021

DEVICE PACKAGING

A GLOBAL VIRTUAL EVENT • WWW.DEVICEPACKAGING.ORG

Design and Simulation of 3D TSV Inductor for IoT Applications

Bruce Kim, Ph.D.

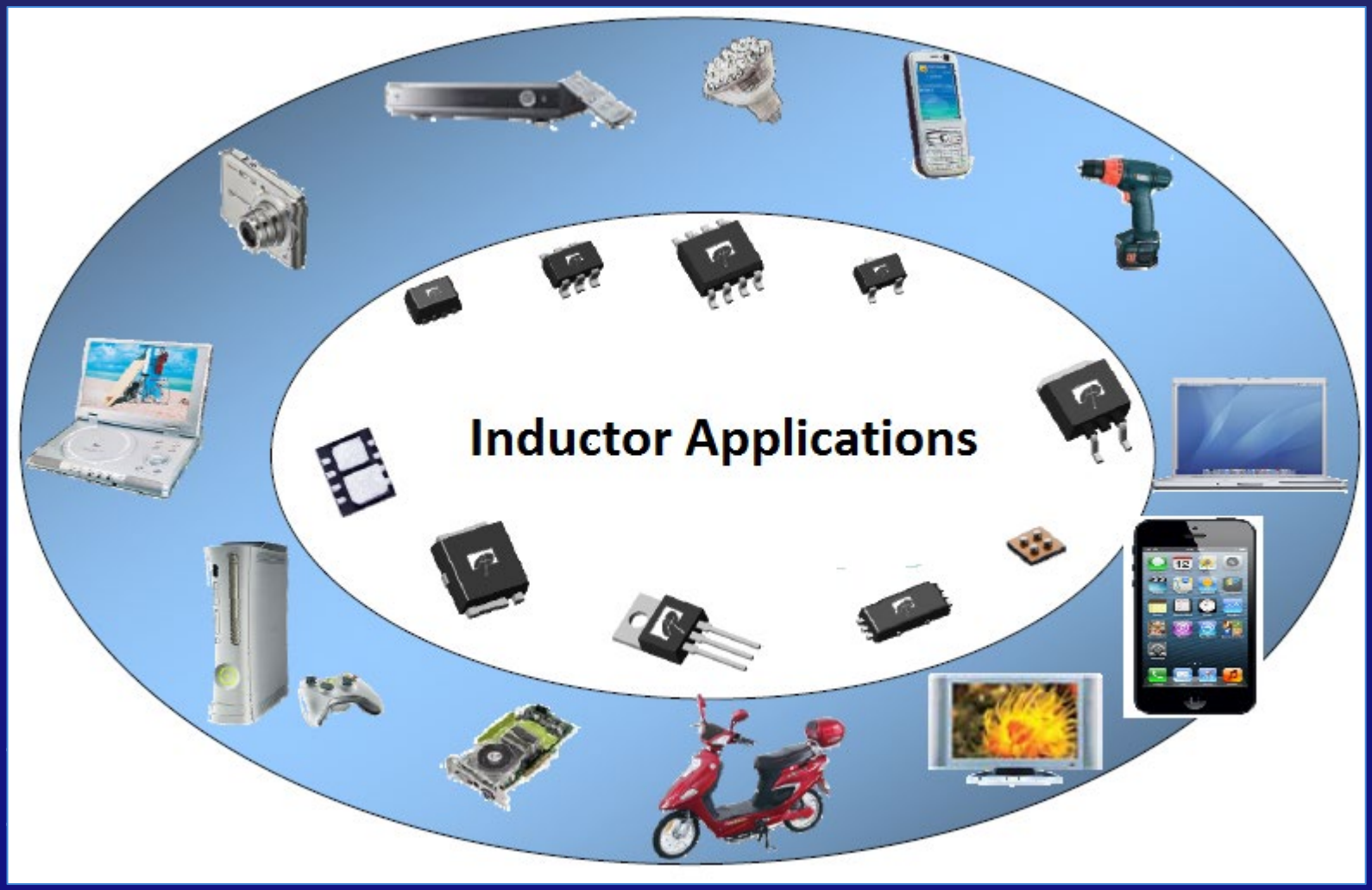
City University of New York

17th International Conference on Device Packaging
April 12-15, 2021

CUNY The City University of New York

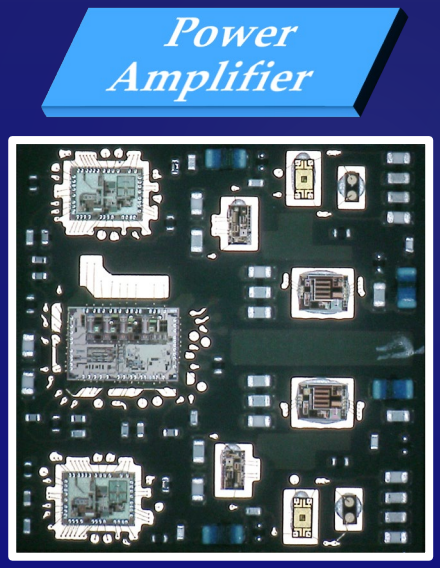
Outline

- Introduction
- Objectives
- Approach & Results
- Packaging
- Summary


Inductor Applications

Inductor

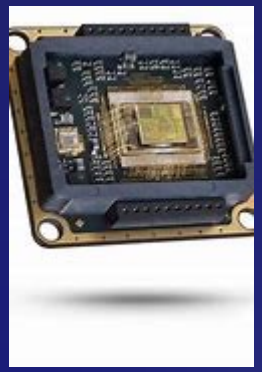
- One of the major passive component in RF application to dc -dc converter.

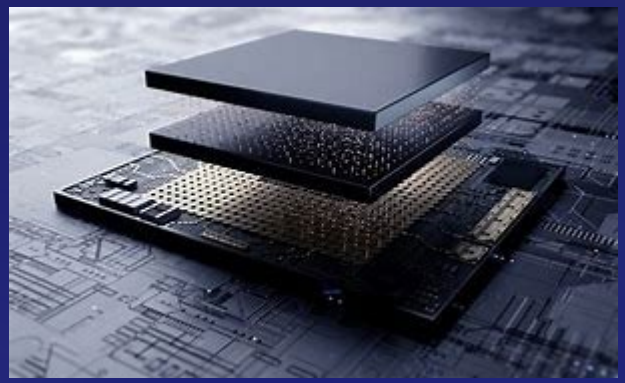


Conventional Passive Inductor

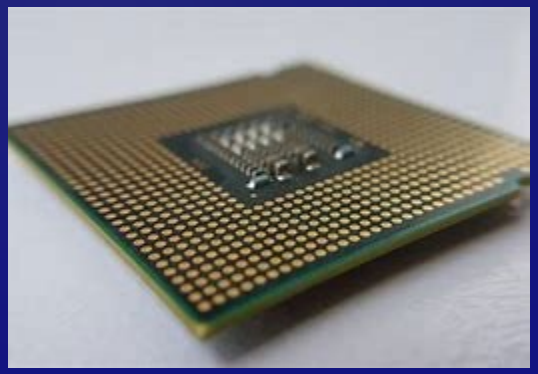
- Inductor size varies depending on applications.

Security of IoT



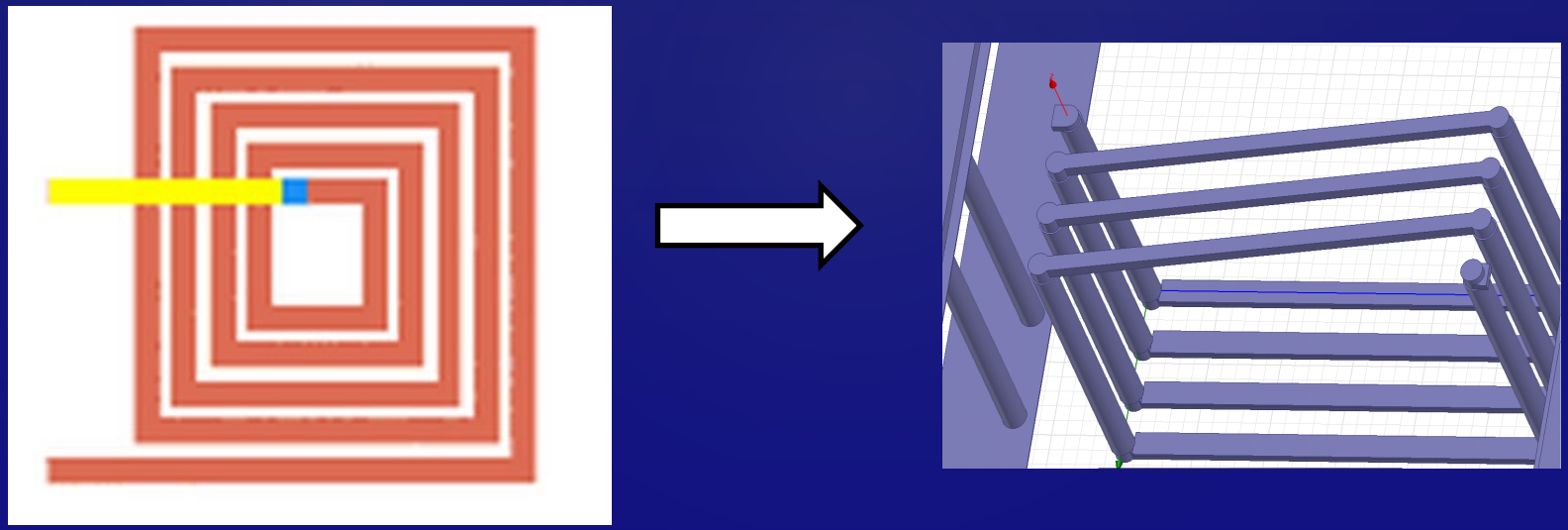


We need security.

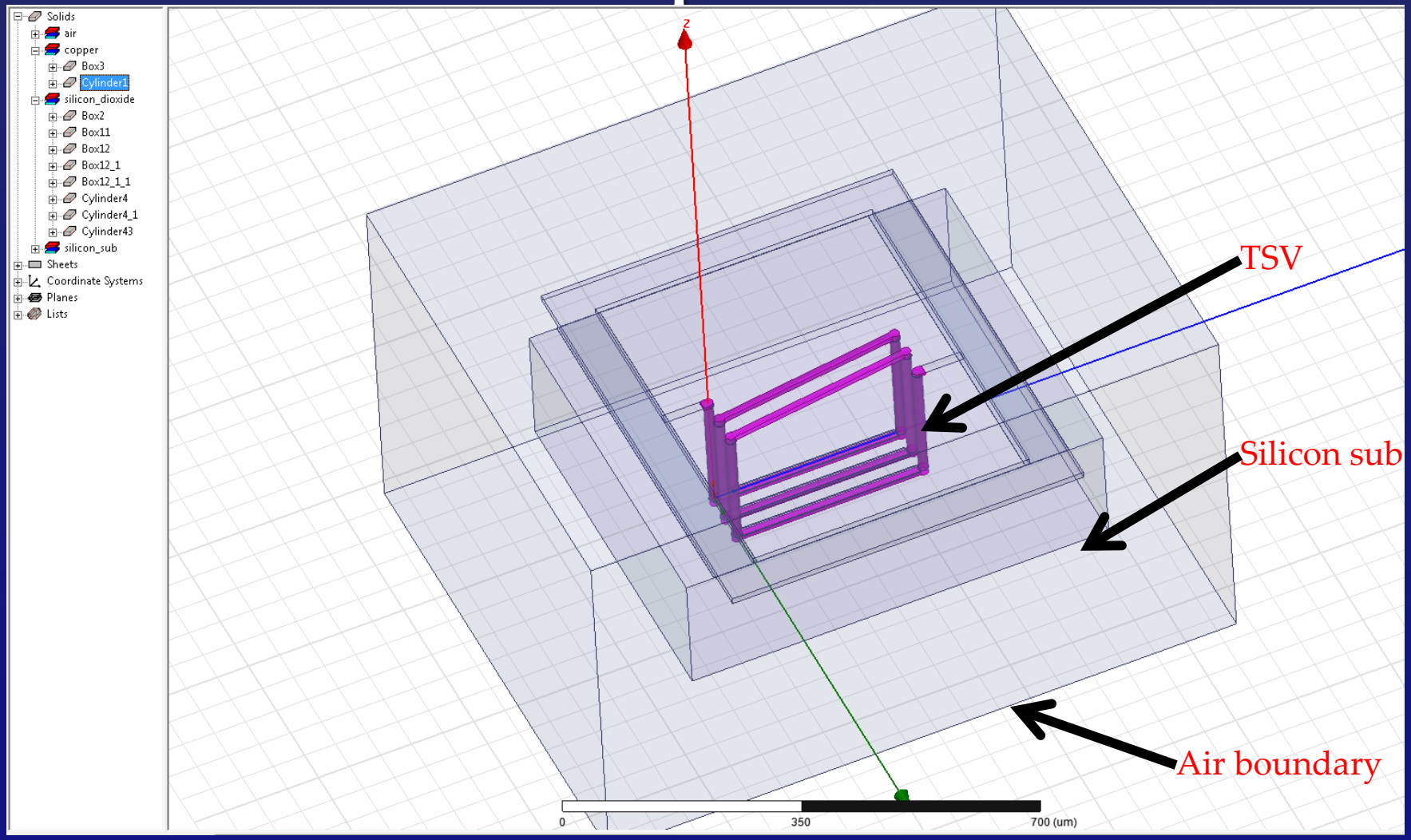


Motivation

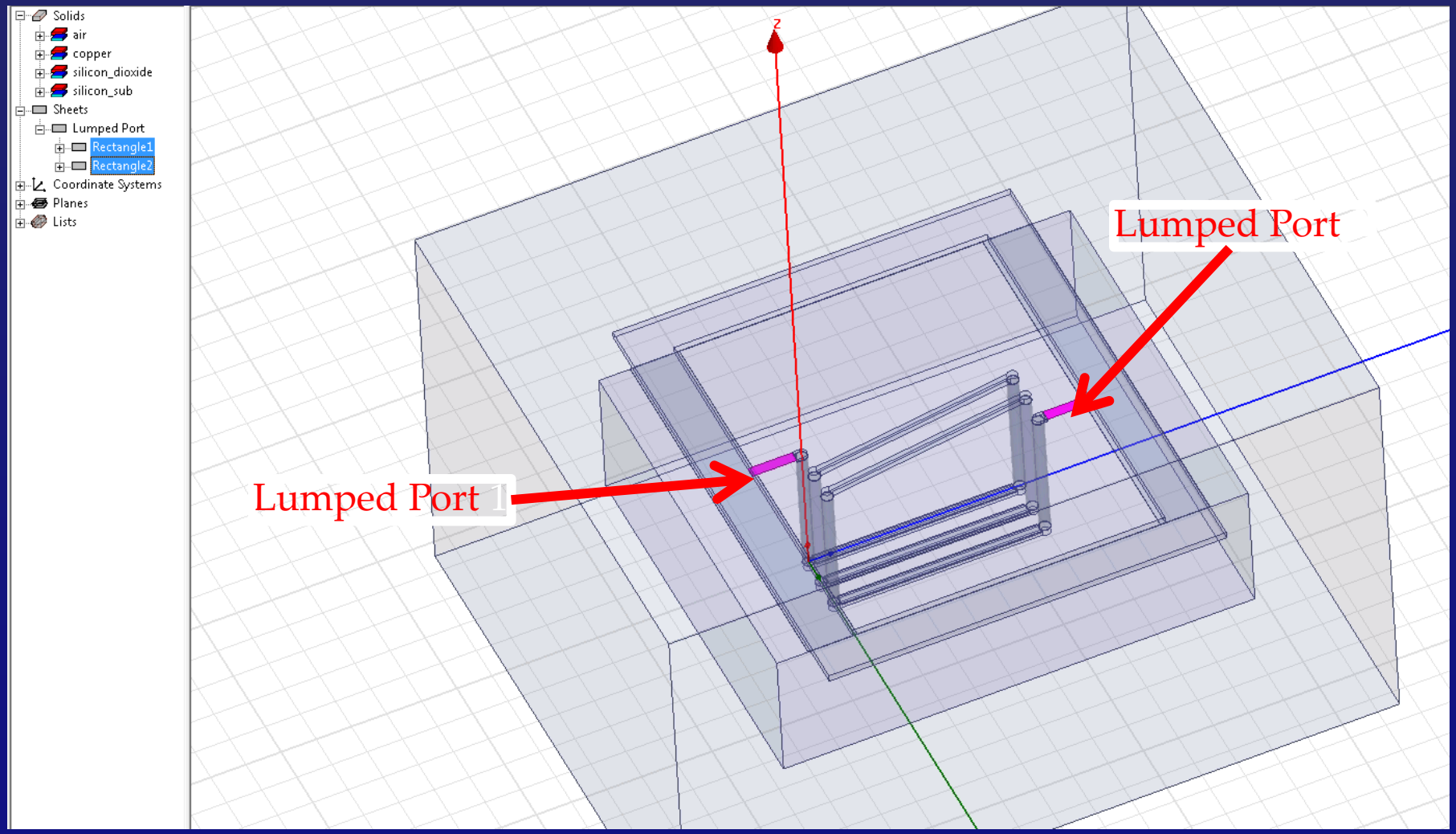
- Conventional 2D inductor needs larger footprint.
- High inductance density for 3D inductor.



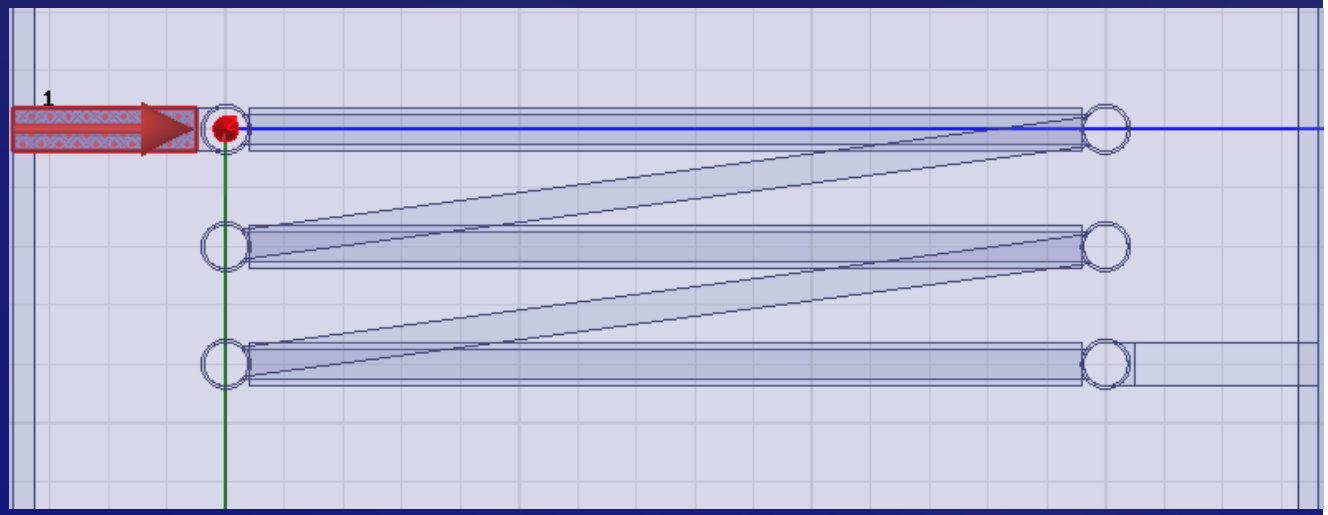
HFSS Setup

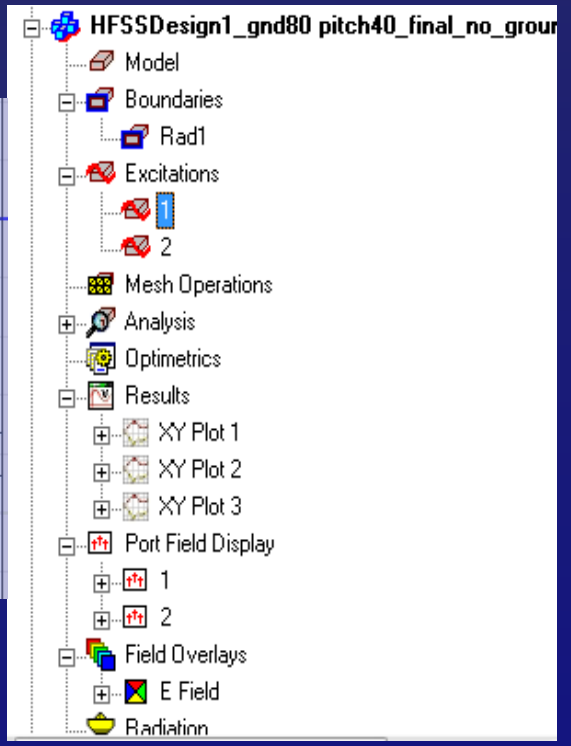

Solids
air
copper
Box3
Cylinder1
silicon_dioxide
Box2
Box11
Box12
Box12_1
Box12_1_1
Cylinder4
Cylinder4_1
Cylinder43
silicon_sub
Sheets
Coordinate Systems
Planes
Lists
Z
TSV
Silicon sub
Air boundary
0
350
700 (um)

HFSS Setup


Solids
air
copper
silicon_dioxide
silicon_sub
Sheets
Lumped Port
Rectangle1
Rectangle2
Coordinate Systems
Planes
Lists
Z
Lumped Port
Lumped Port 1

HFSS Setup



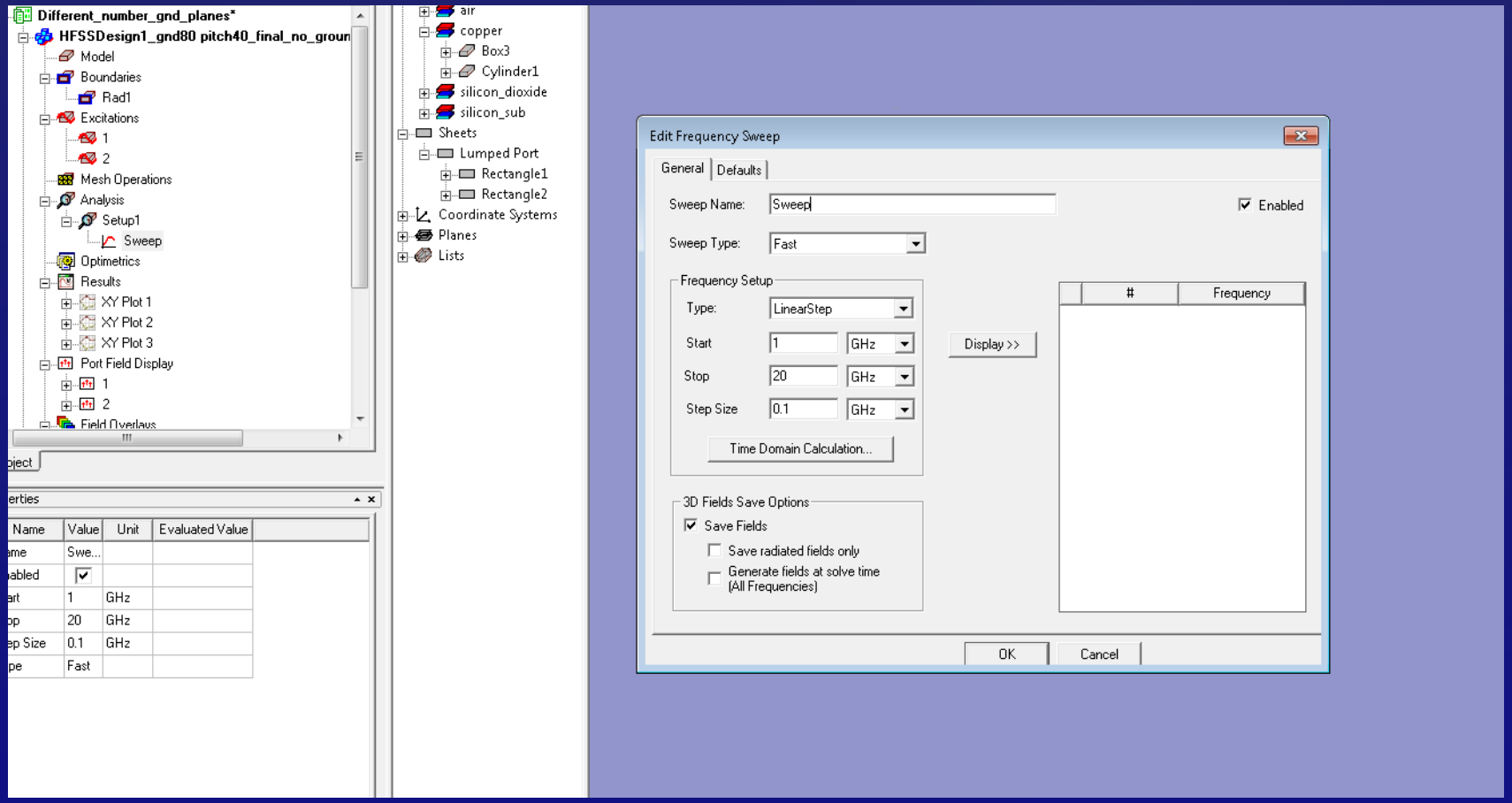


50Ω termination Lumped Ports

Electromagnetic excitations are provided at the ports

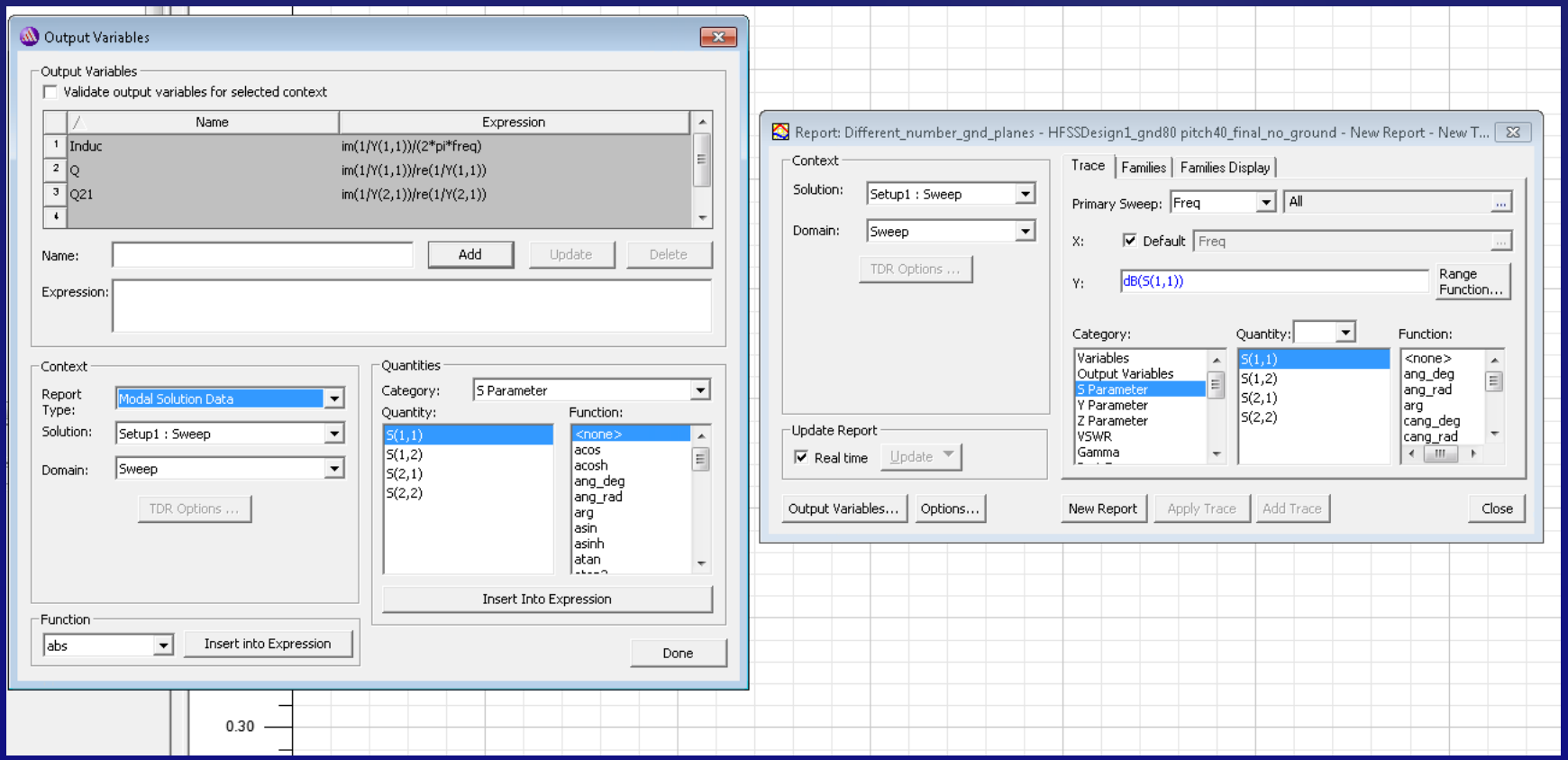
HFSS Setup

Parametric Frequency sweep from 1 to 20 GHz

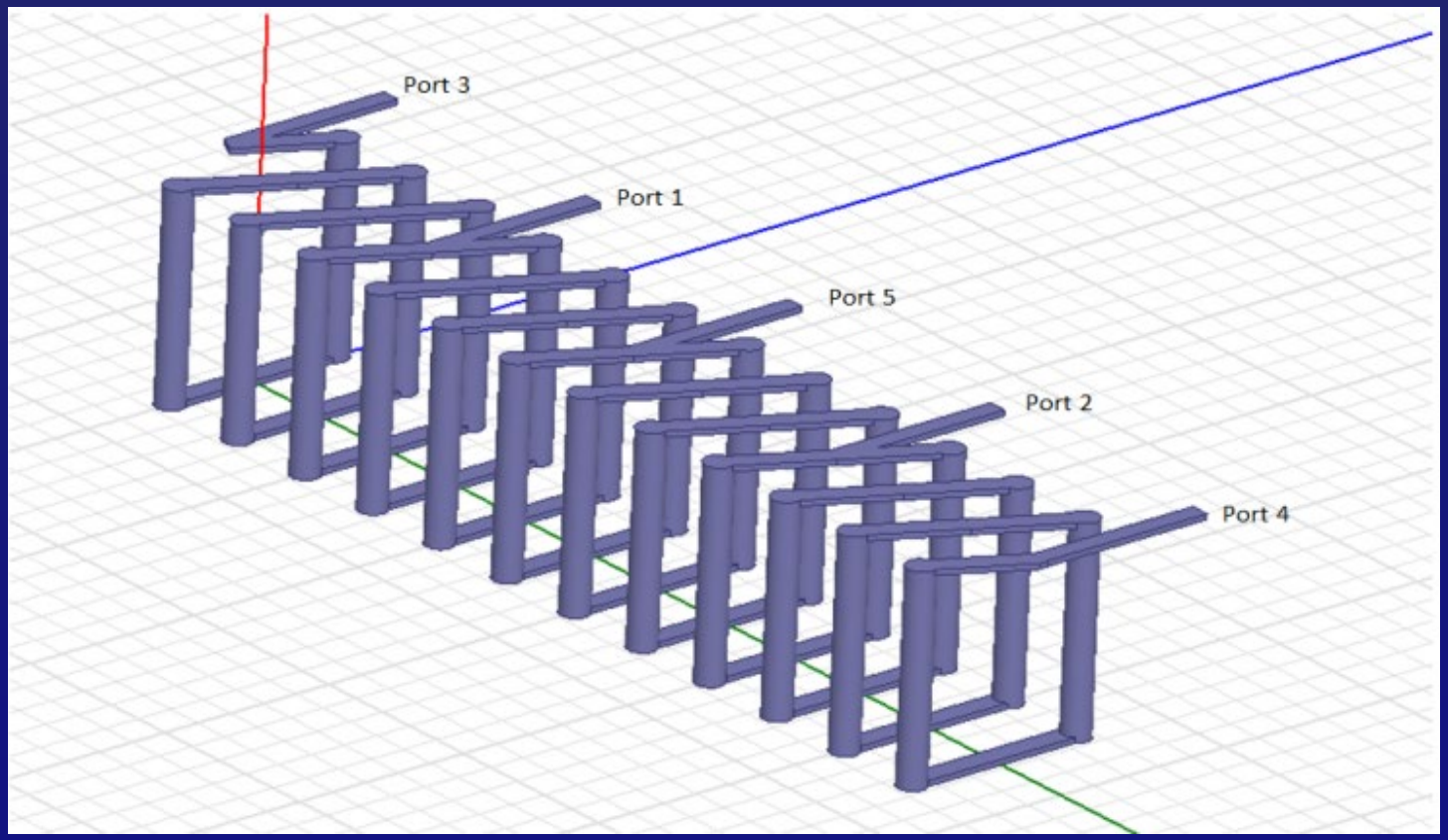


HFSS Setup

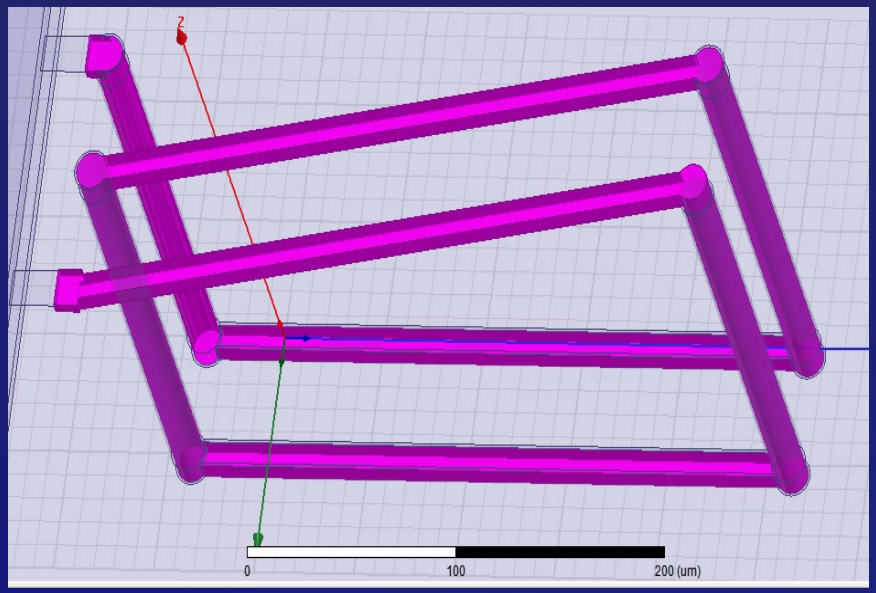
Inductance and Quality factor formula from Y parameters.



3D Design

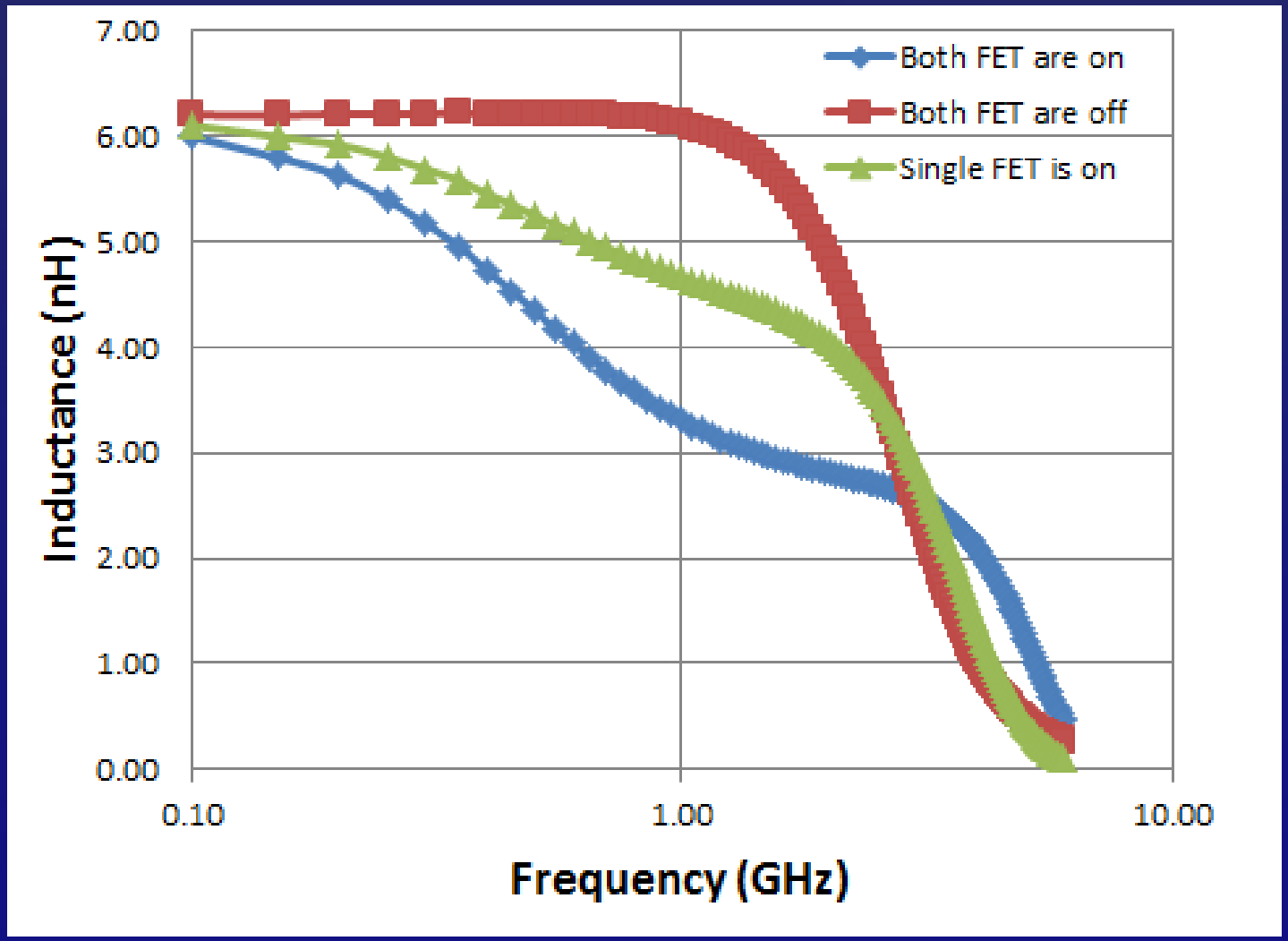


TSV Inductor



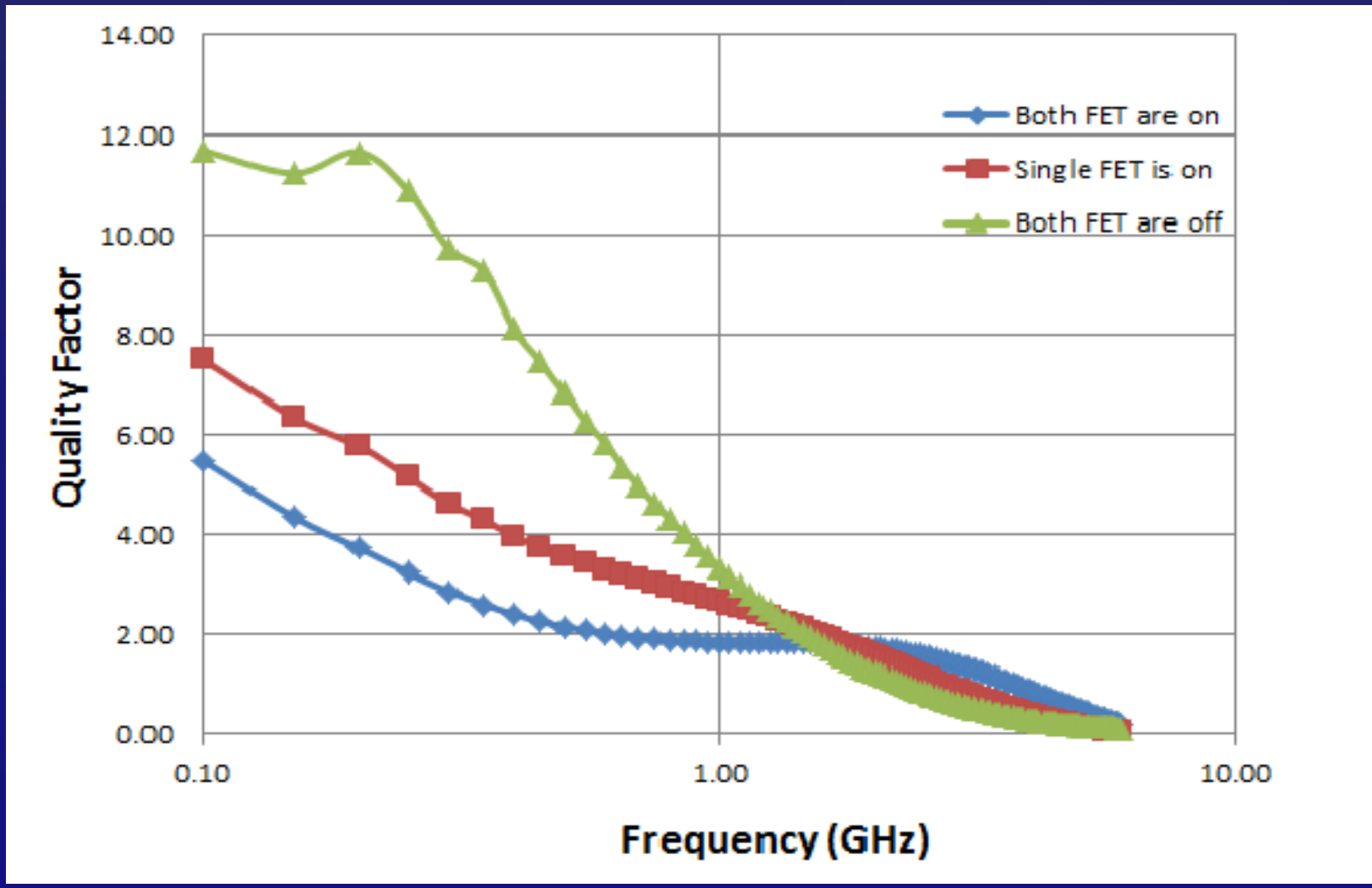
Design Parameters	dimensions
TSV Length	300 µm
TSV Diameter	40 µm
Metal Width	25 µm
Metal Thickness	8 µm
Minimum Spacing D	125 µm

Tunable Inductance

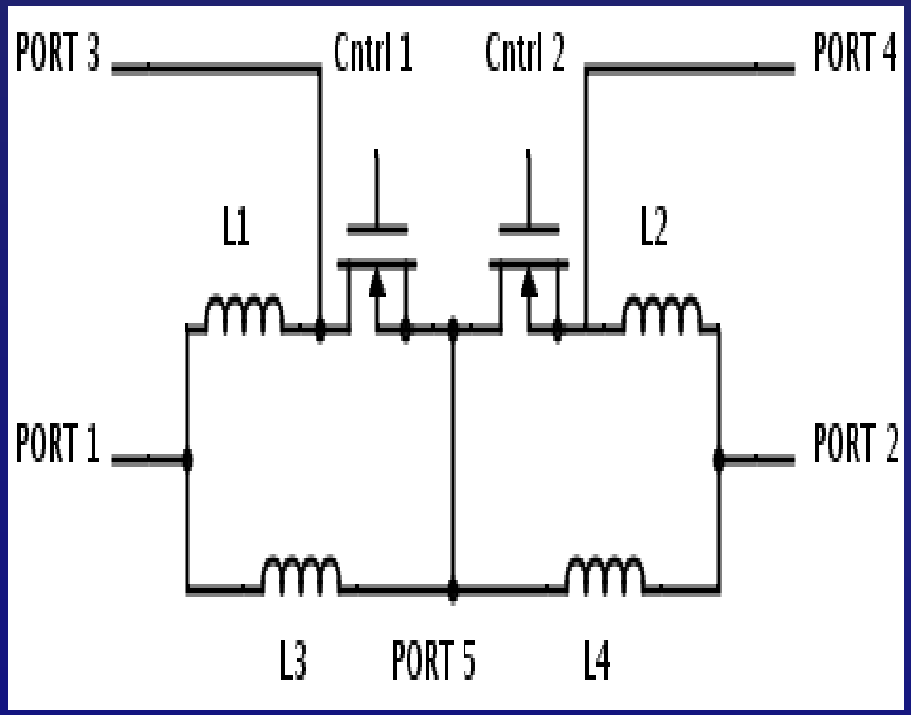


Source: B. Kim et. al. EPTC 2014.

Tunable Q Factor



Tunable Inductor

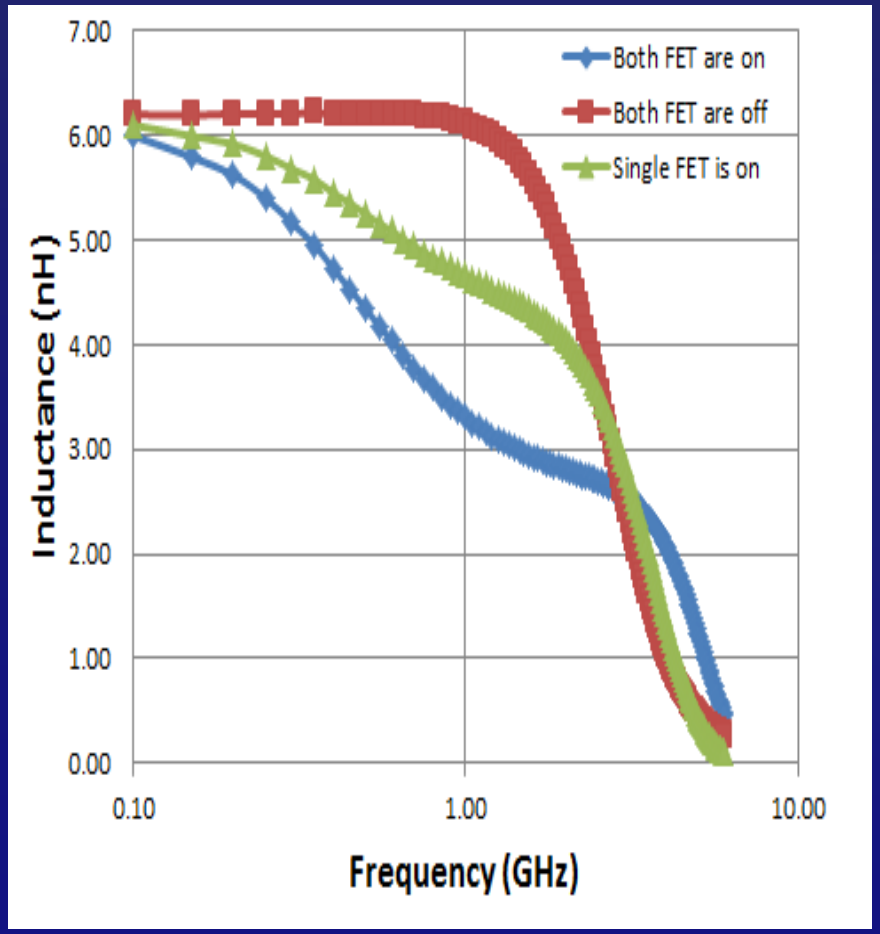


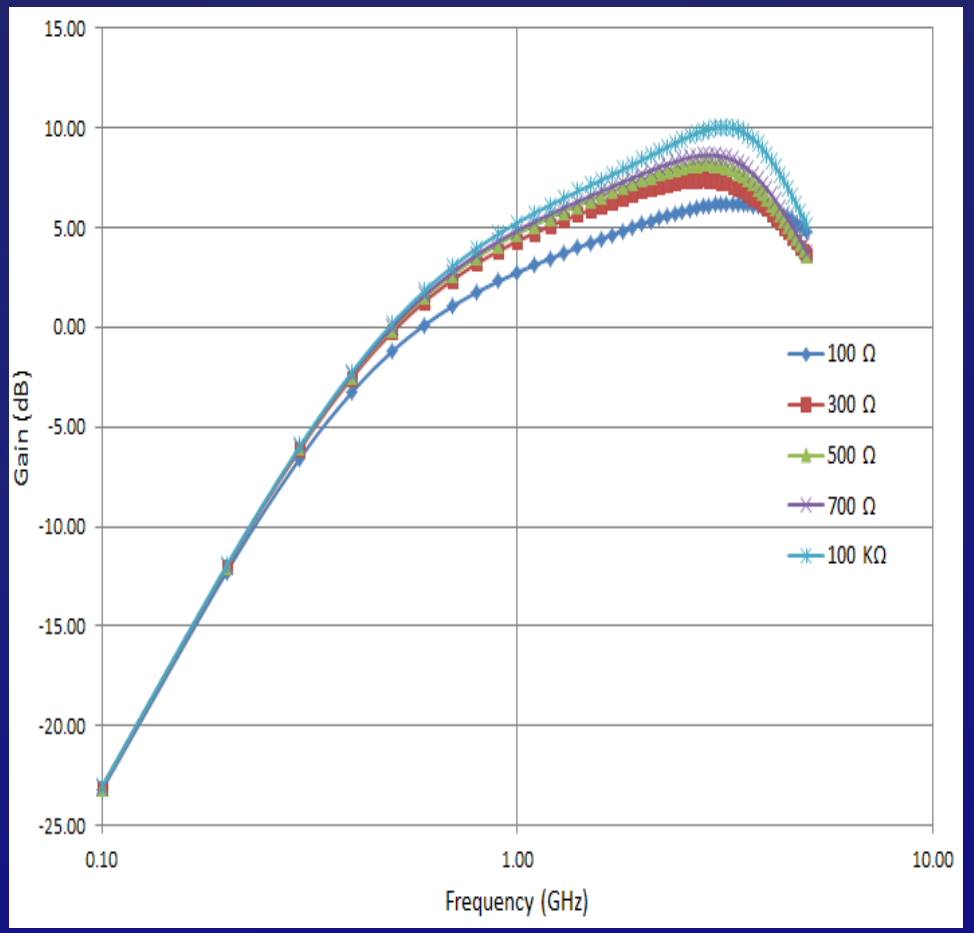
Control 1	Control 2	Equivalent Inductance
Low	Low	2L
High	Low	3L/2
Low	High	3L/2
High	High	L

Results for 700MHz LTE Band

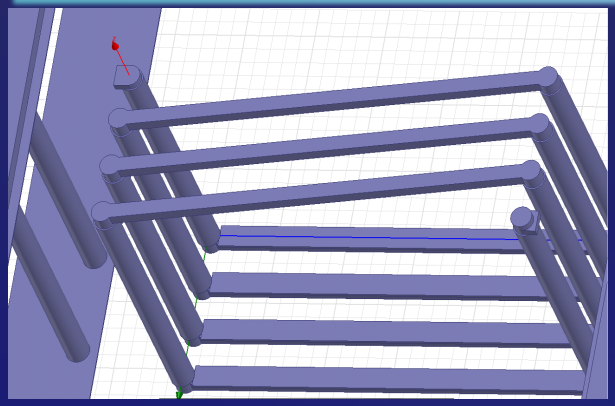
Control 1	Control 2	Inductance	Quality Factor
Low	Low	6.19 nH	4.98
High	Low	4.94 nH	3.11
Low	High	4.94 nH	3.11
High	High	3.78 nH	1.94

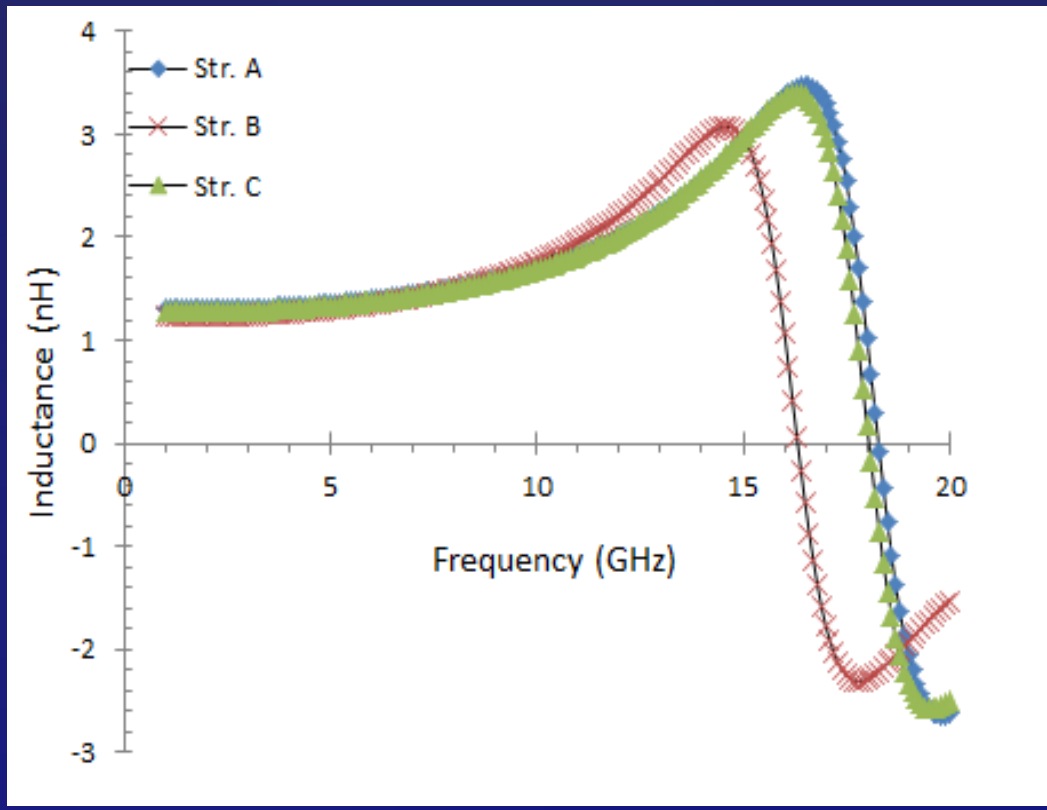
TSV Inductor Results

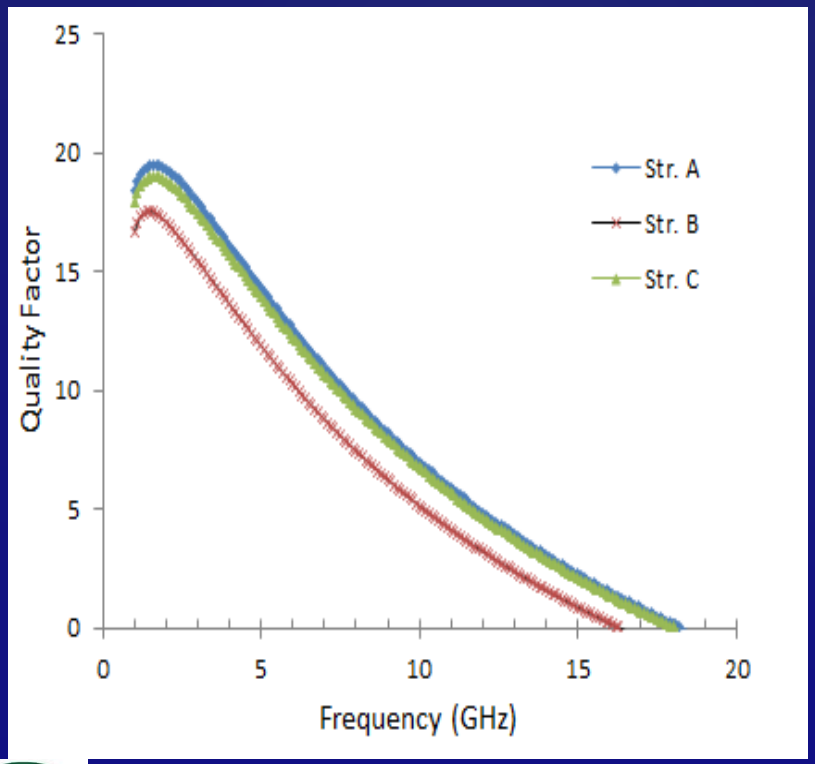




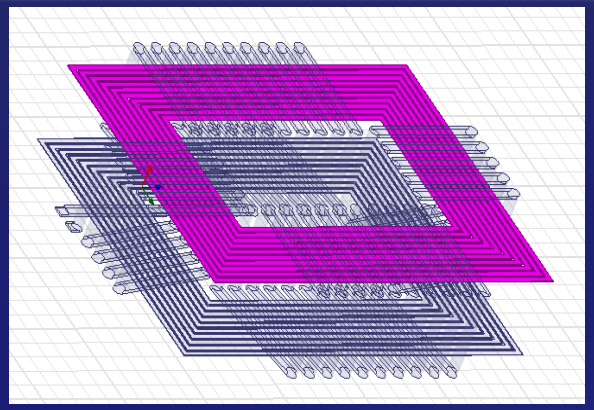
TSV Inductors



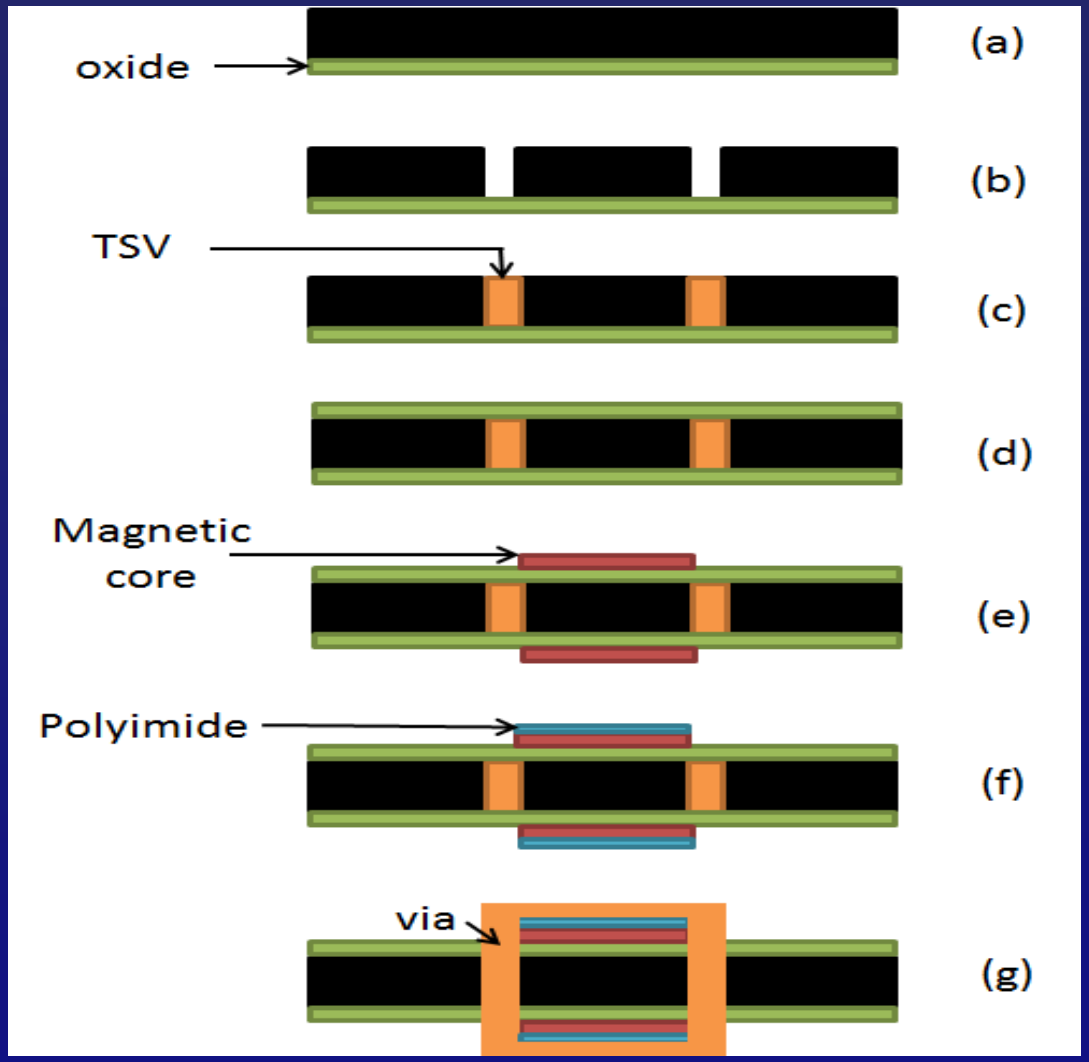




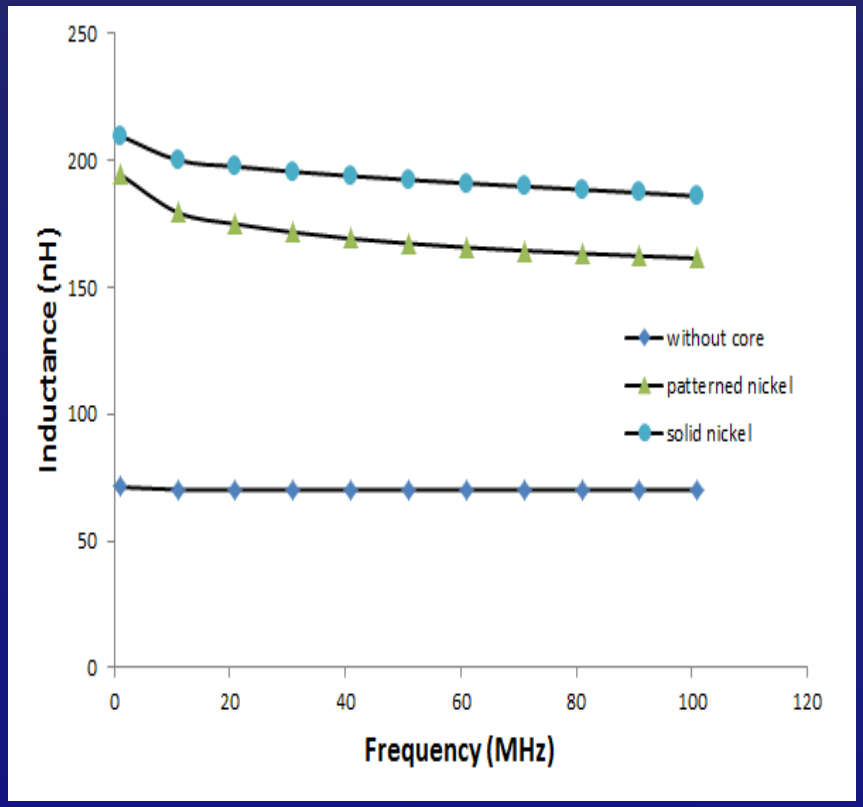
Fabrication of TSV Inductors

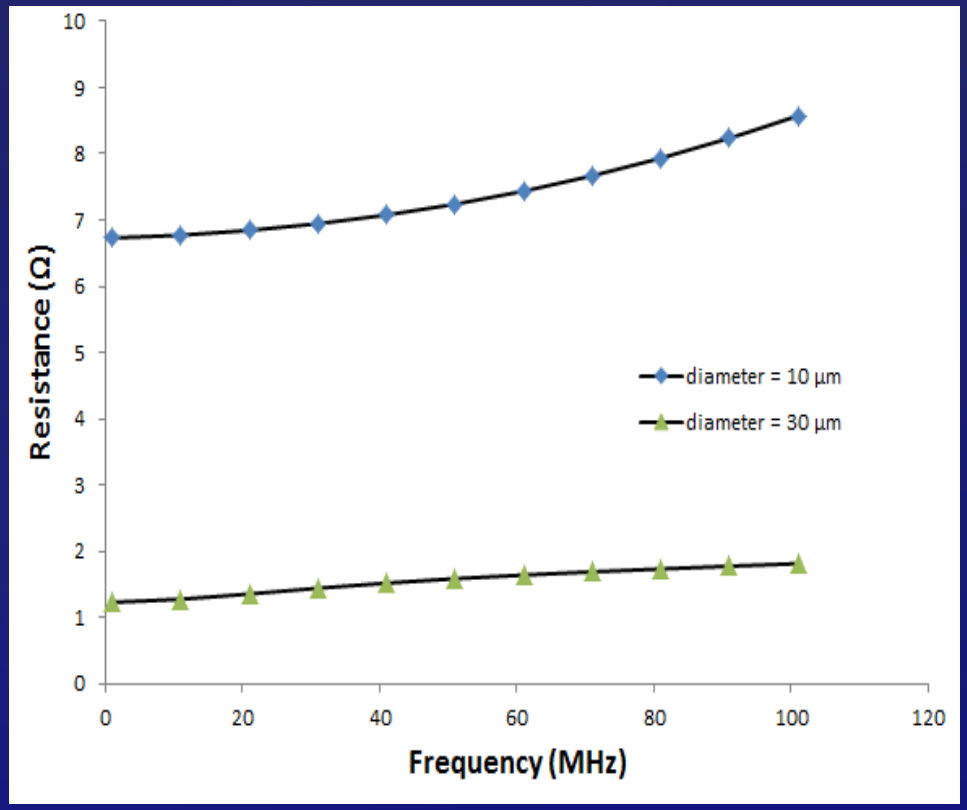


Design Parameter	Dimension (μm)
Radius of TSV	5, 15
Length of TSV	220
Dielectric liner thickness	1
Interconnect length	300
Interconnect width	10, 30
Interconnect thickness	8
Pitch between two loops	25
Lamination gap	5
Core ring width	15
Core ring thickness	2
Core ring length for single loop	1210-2670

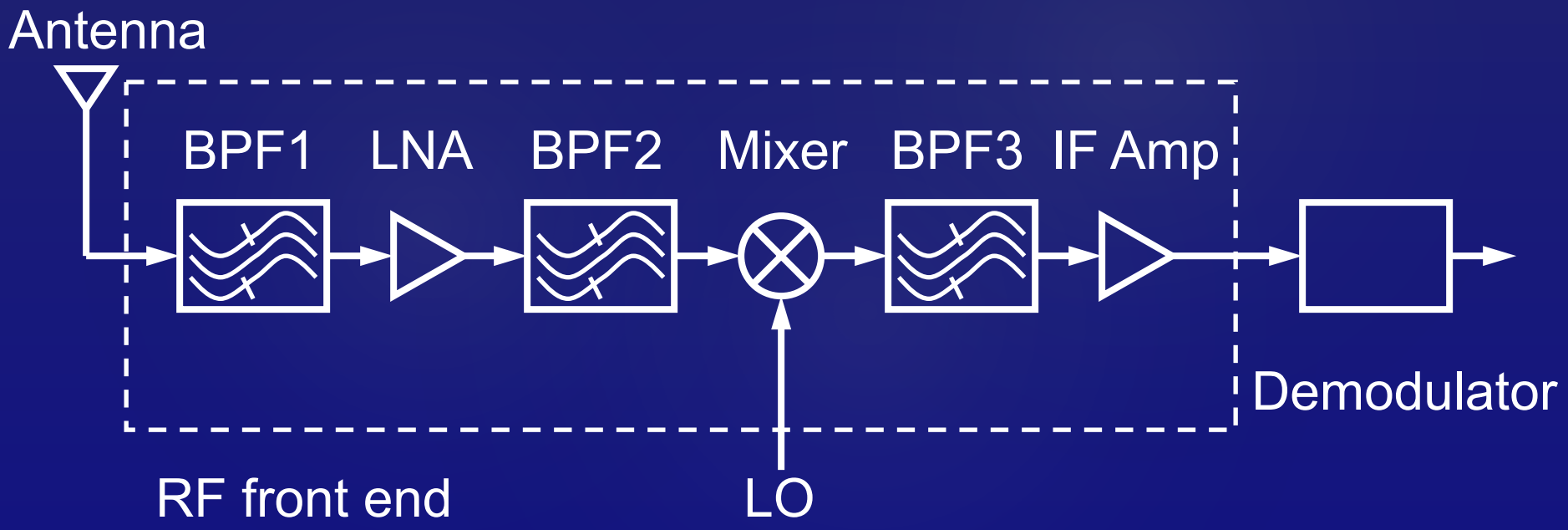


Simulation Results

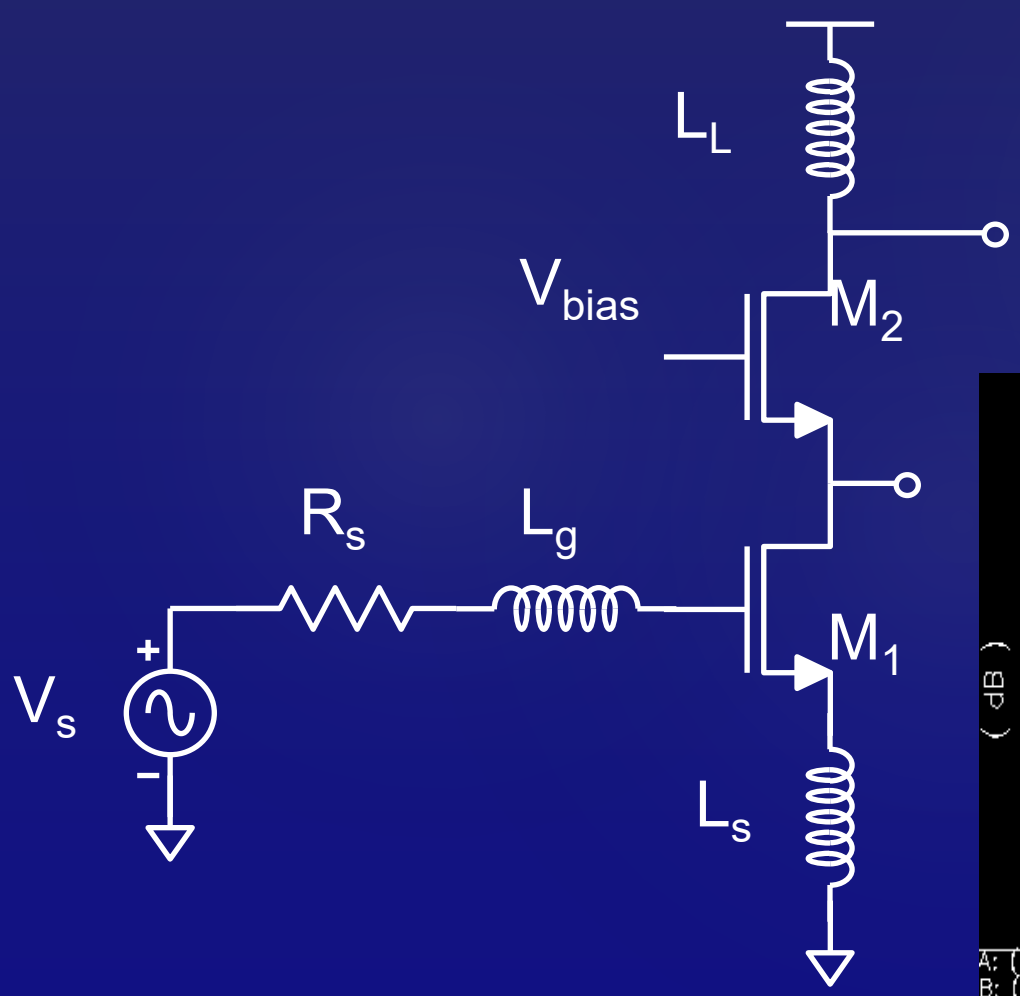




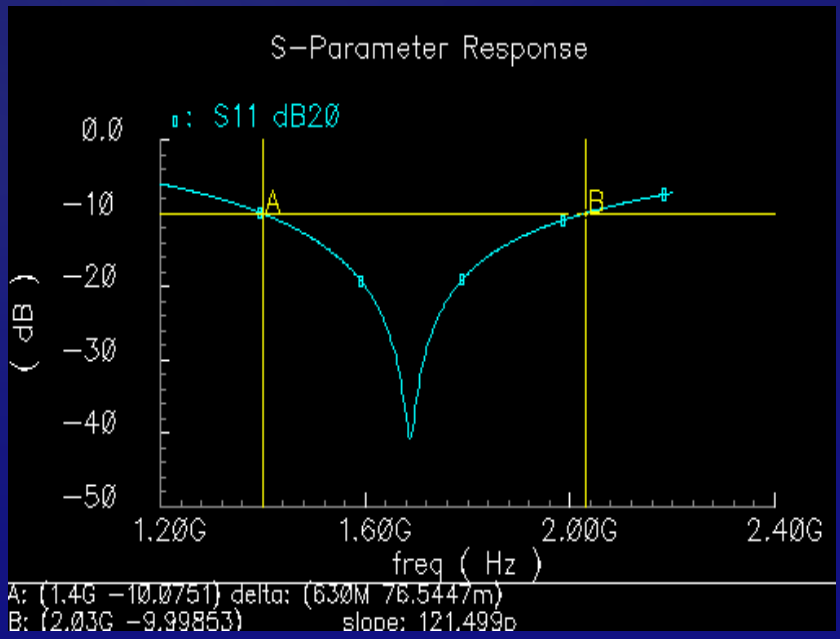
RF Receiver


Antenna
BPF1
LNA
BPF2
Mixer
BPF3
IF Amp
Demodulator
RF front end
LO

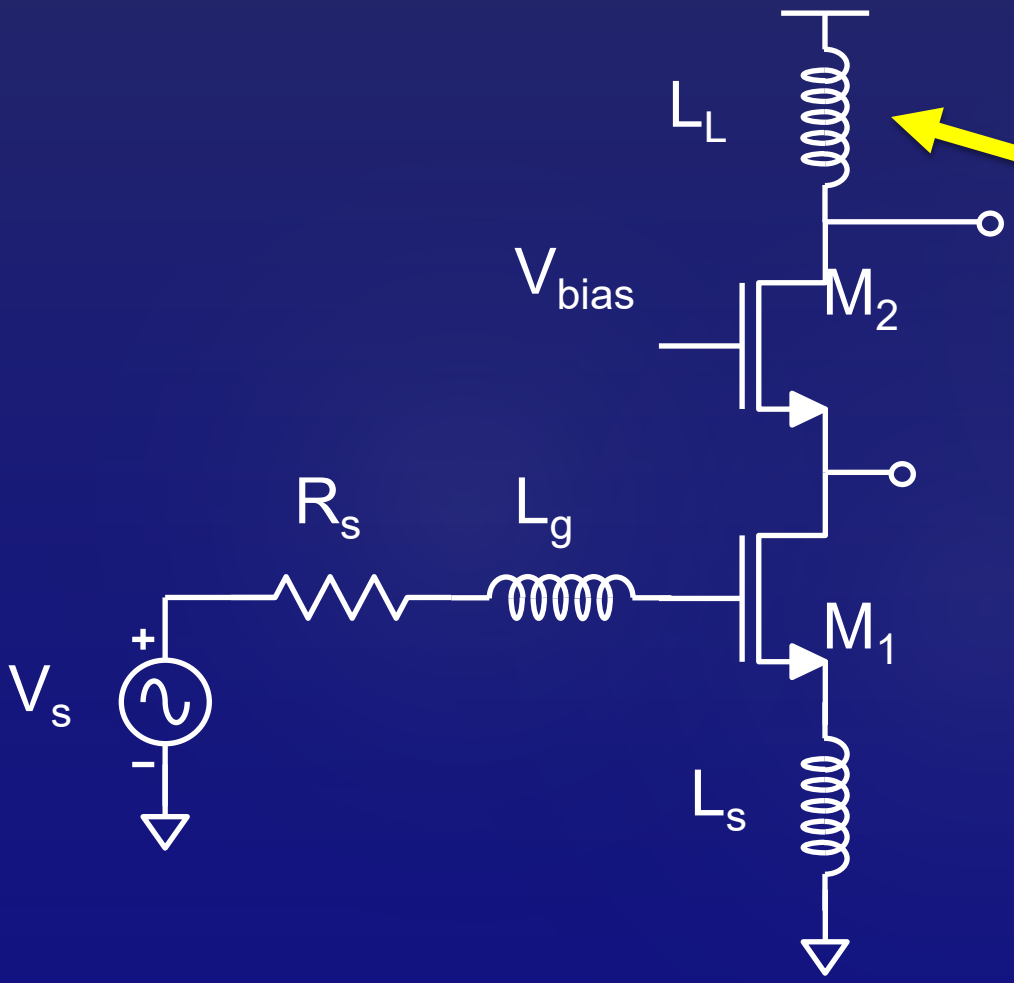
Cascode LNA Design

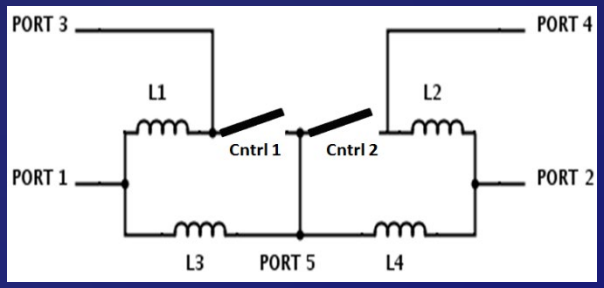


- The input return loss S11 is less than – 10dB at a frequency range between 1.4 GHz and 2GHz

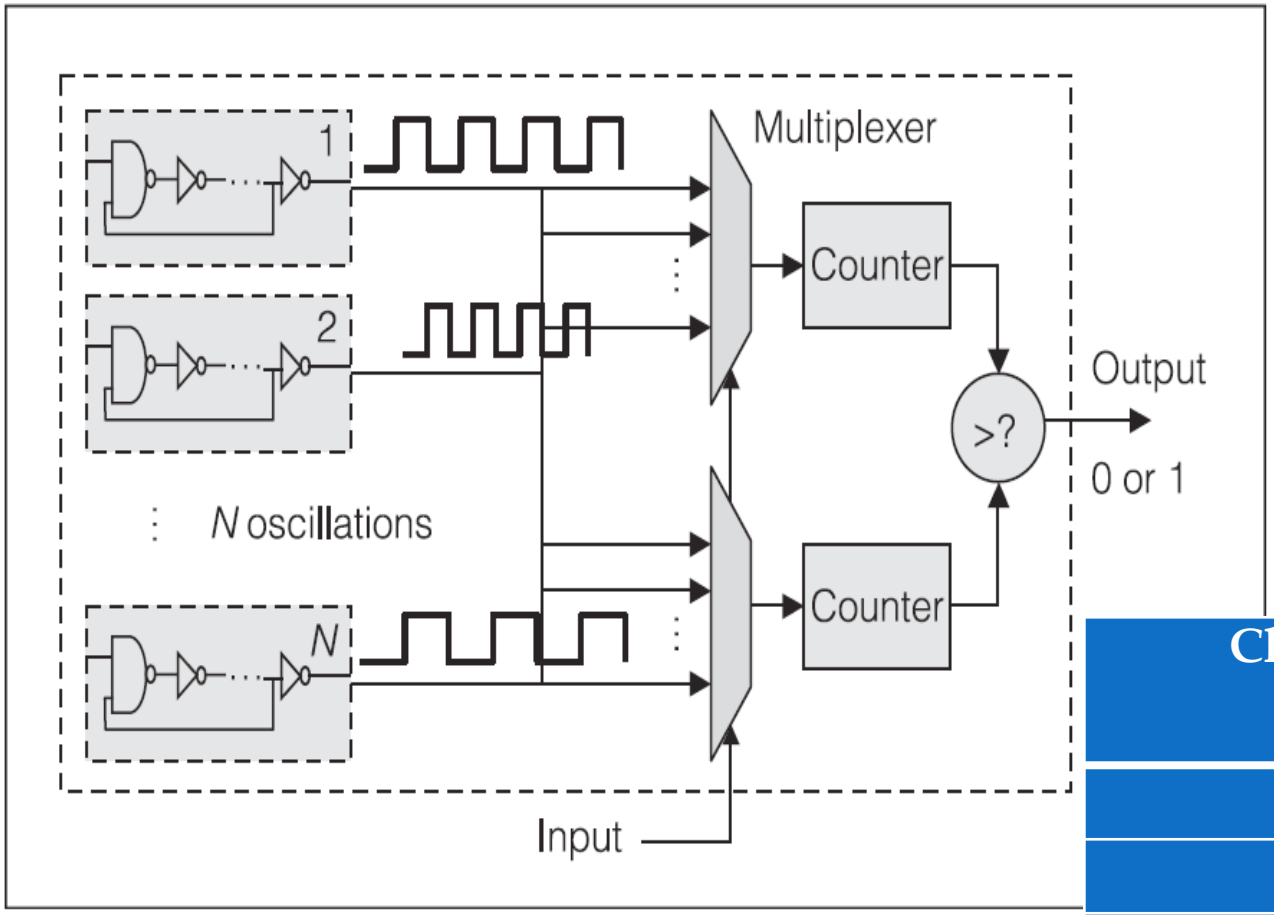


Security of IoT



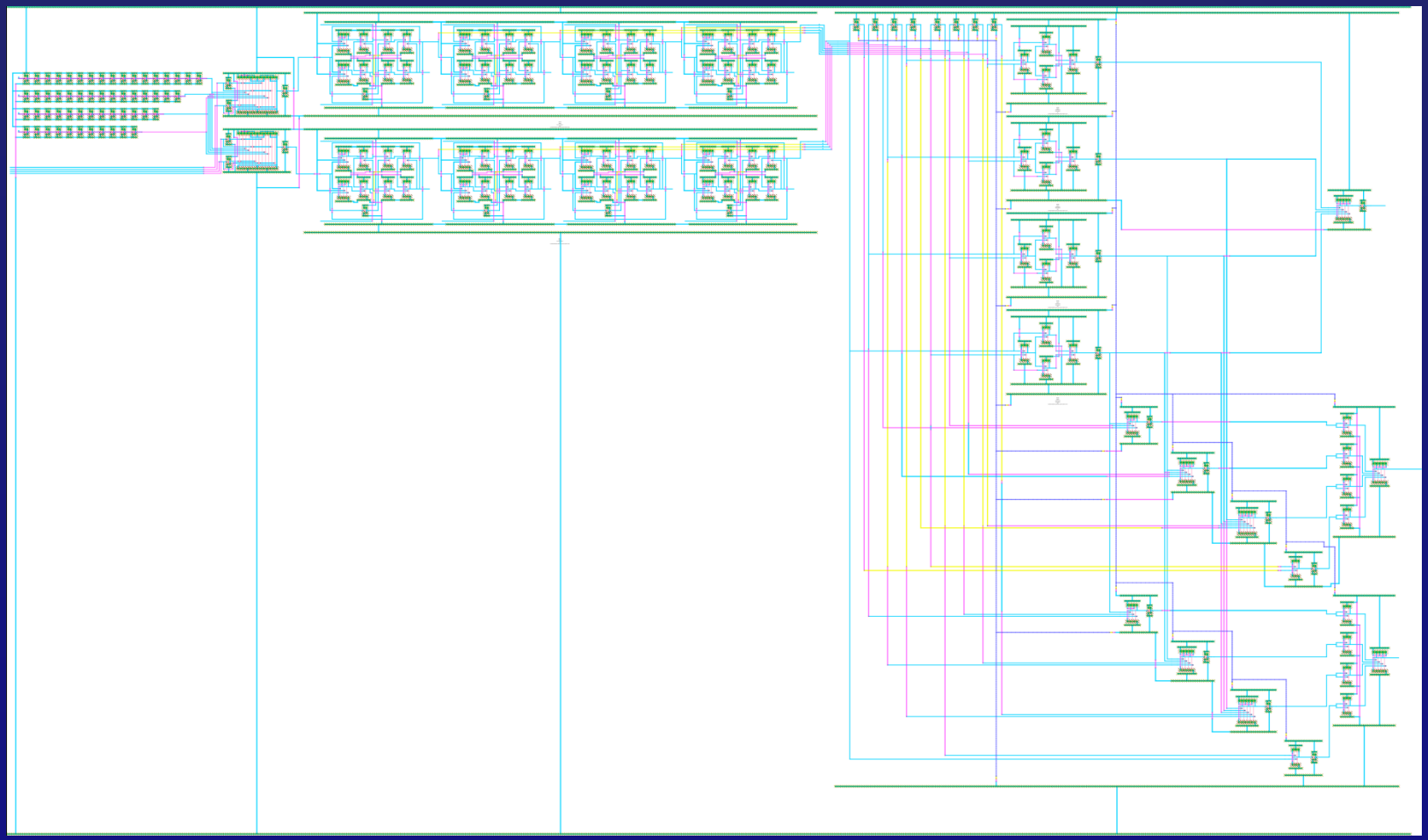


Physically Unclonable Function (PUF)

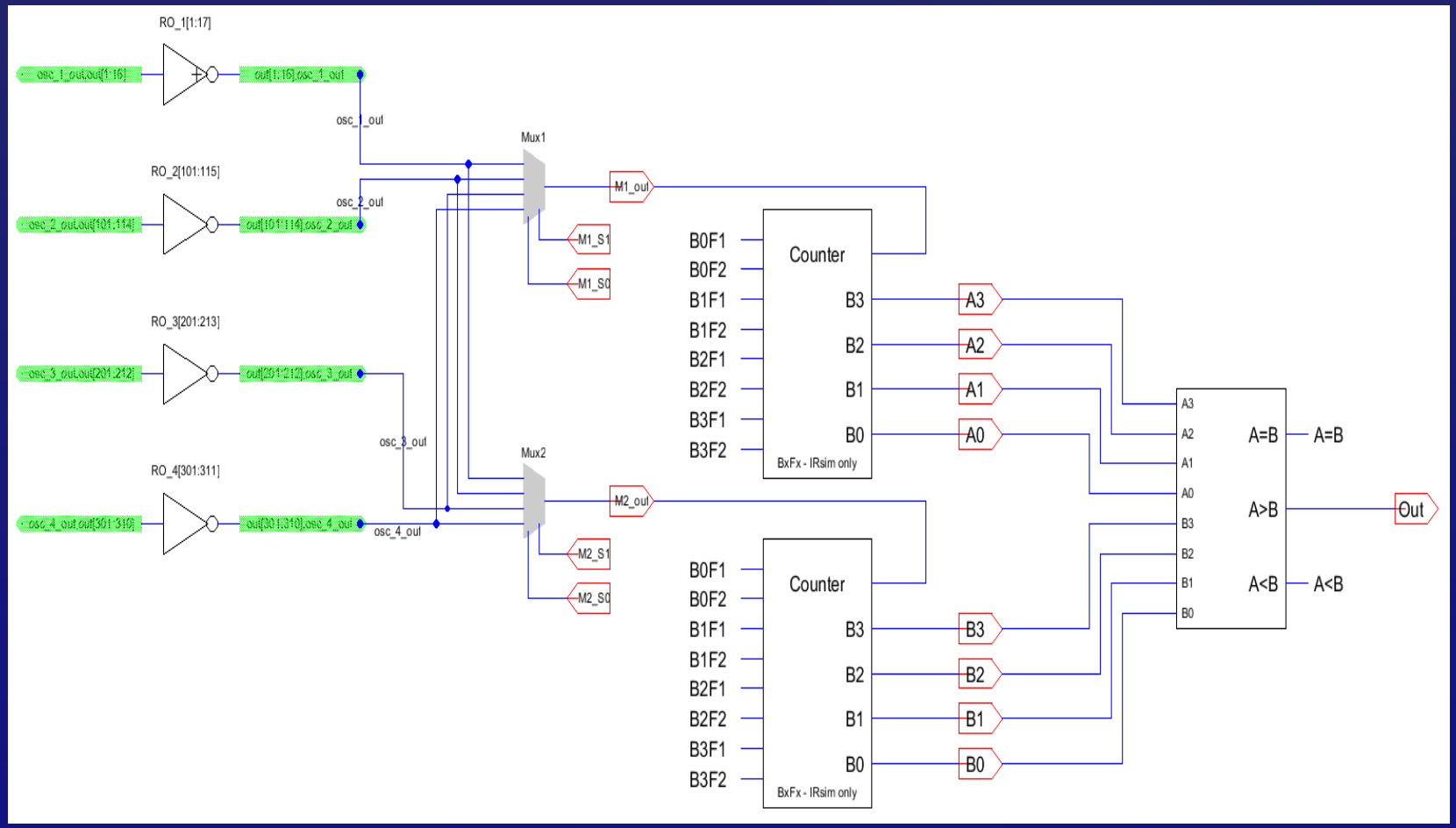


Challenge	Response
0001	0
0011	0
0111	0
1000	1
1001	1
1110	1

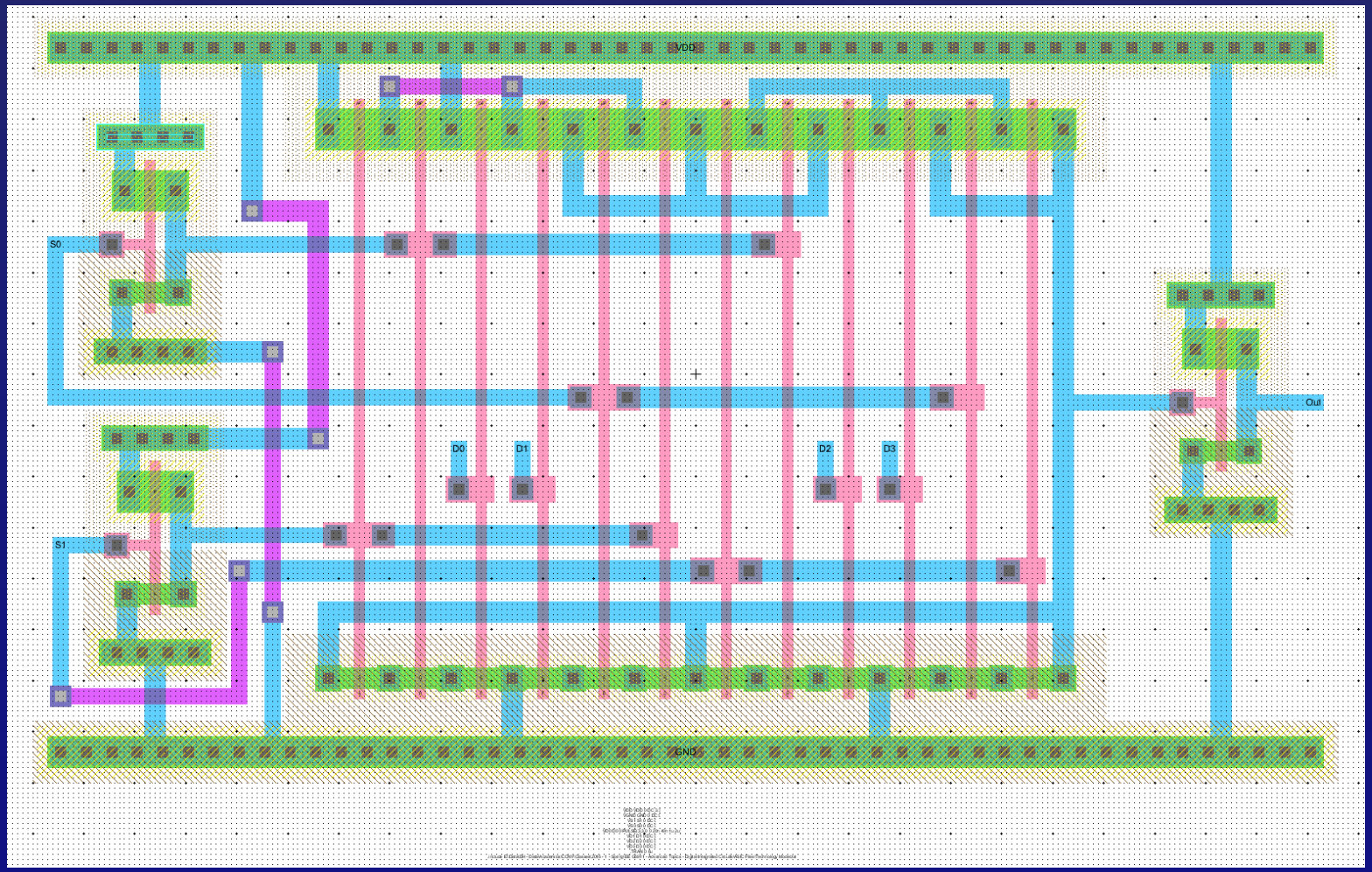
IC Design of PUF



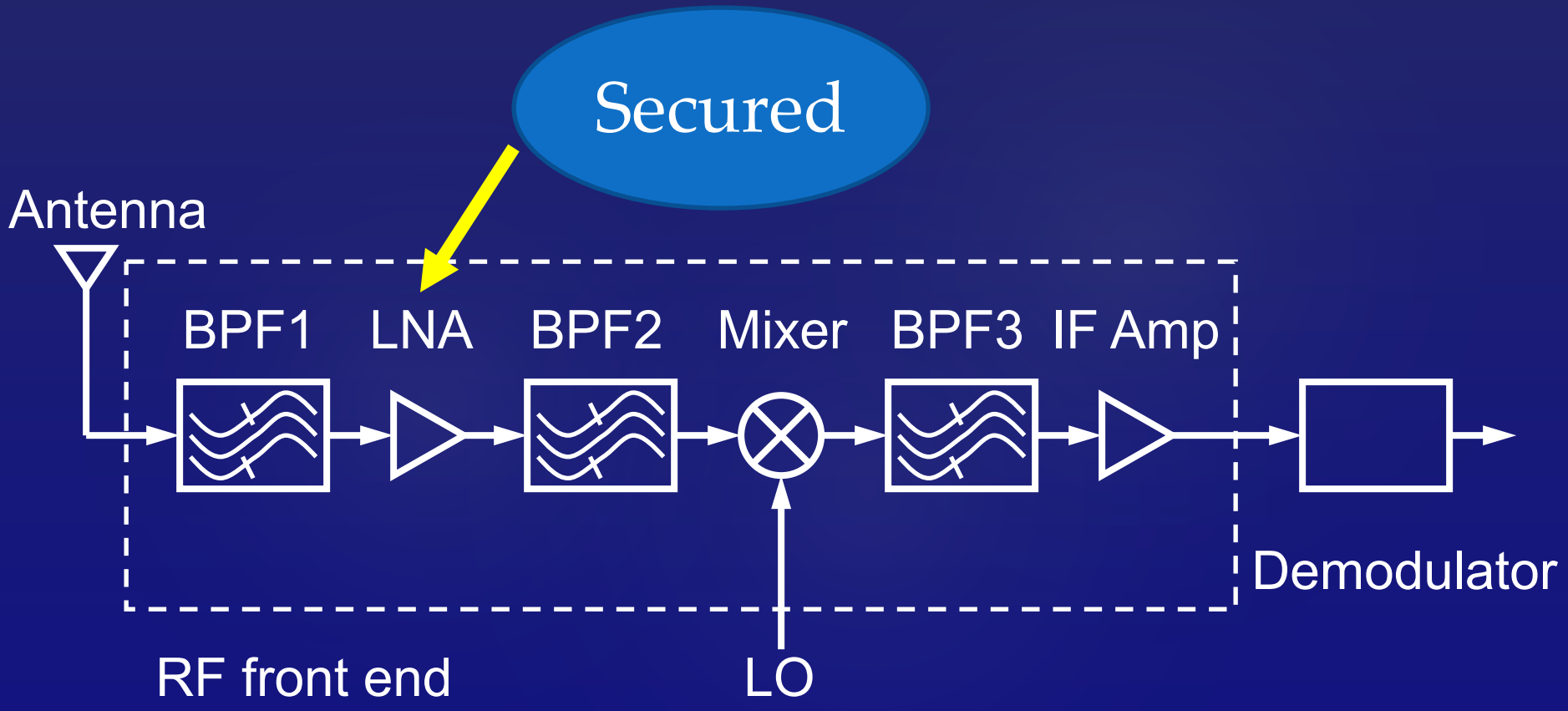
IC Design Schematic



IC Design Details of Counter



Secured RF Receiver



Packaging Challenges for TSV Inductors

- As the vertical area of the die is used in TSV based inductors, the inductance density is much higher than conventional 2D inductors.
- The substrate loss becomes high in case of TSV based inductors, for which the quality factor performance degrades.

Conclusions

- We designed 3D TSV Inductors for IoT
- We designed Tunable Inductors based on TSV Inductors
- We used Physically Unclonable Function to achieve security of IoT.