Substrates for Heterogeneous Integration

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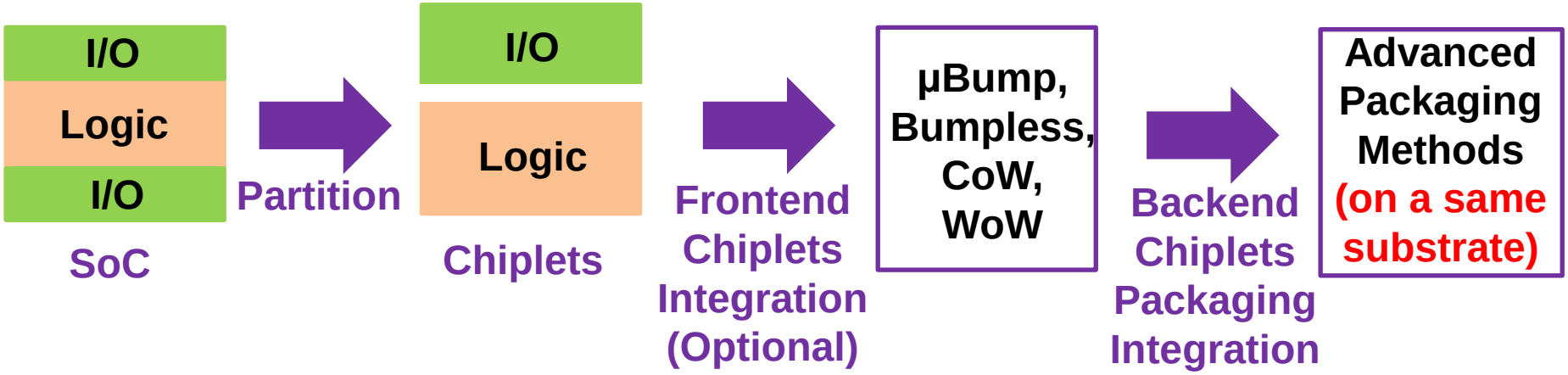
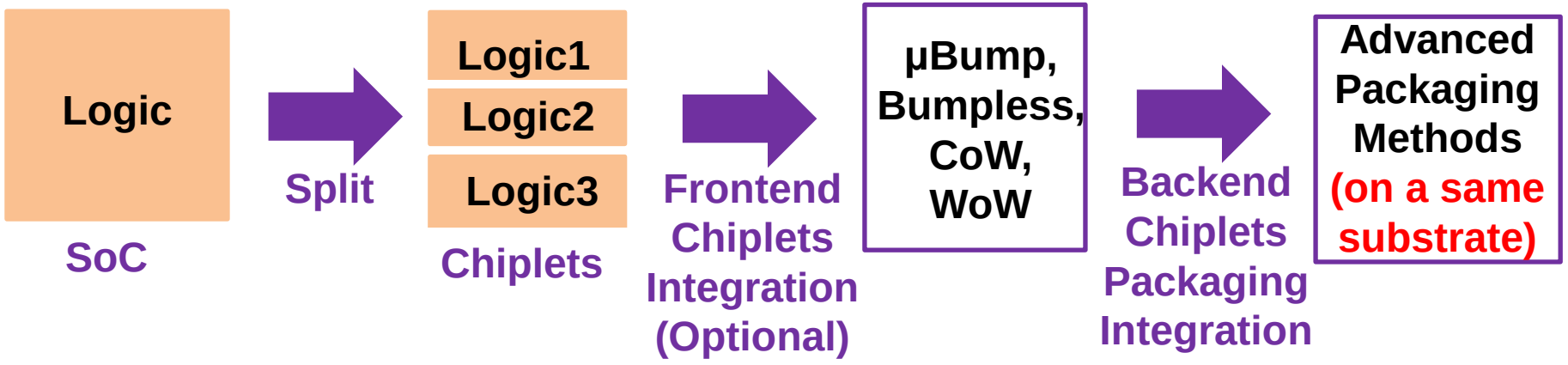
CONTENTS

Chiplets Heterogeneous Integration by Chip Partition and Chip Split

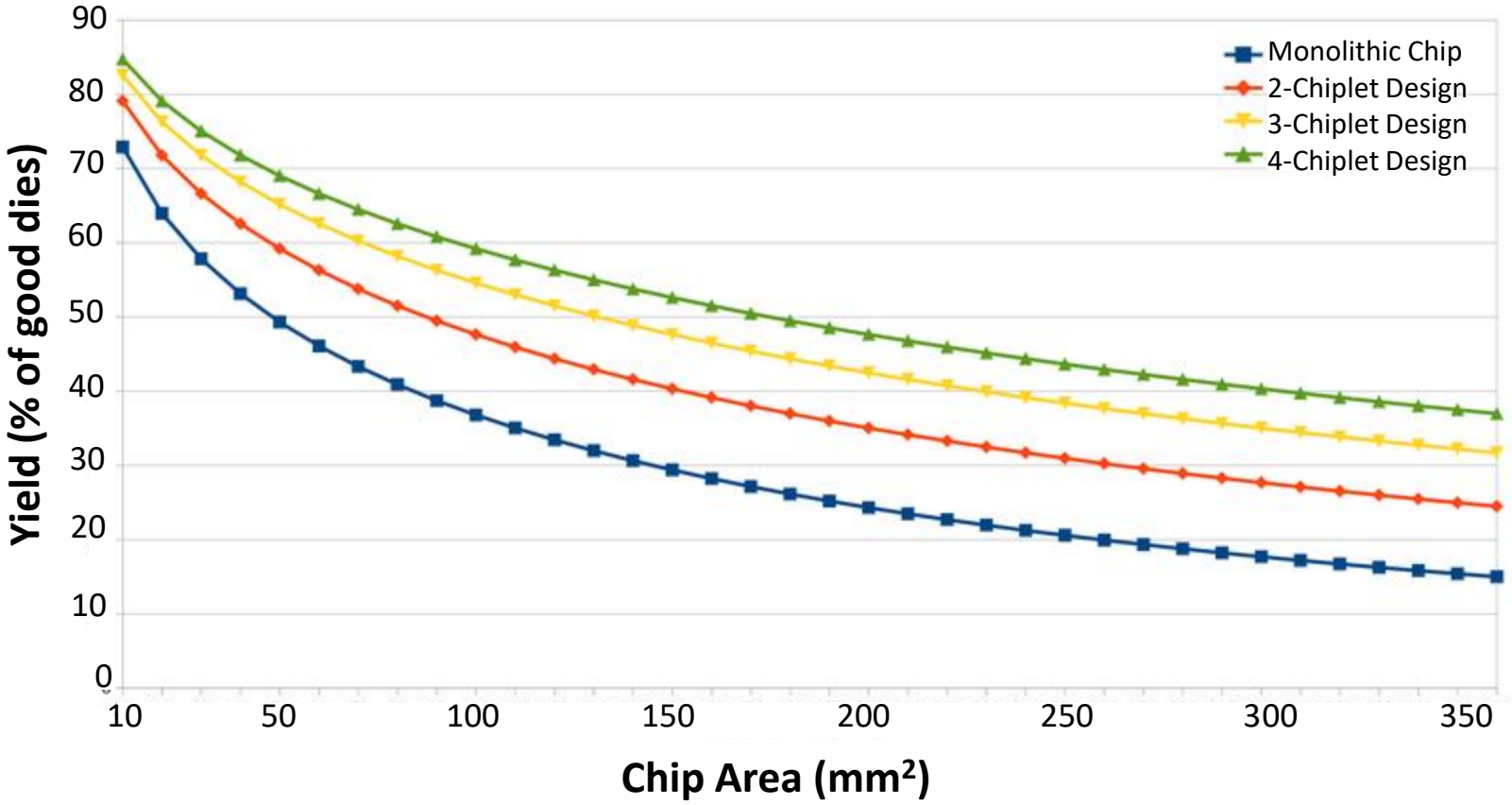


Heterogeneous Integration (Chip partition and integration)



Heterogeneous Integration (Chip split and integration)

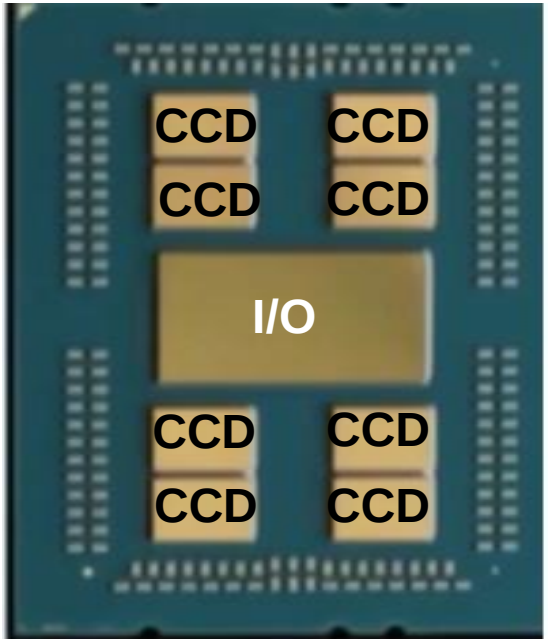
Yield (Cost) per Wafer vs. Chip Size for SoC and Chiplets



Sources: https://en.wikichip.org/wiki/chiplet, March 27, 2020.

AMD EPYC

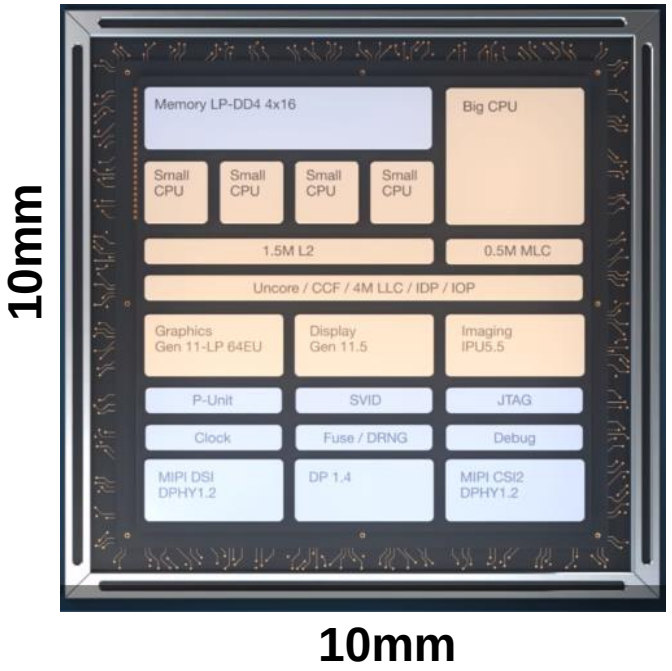
2D IC Integration on organic substrate



- The I/O and CCD (core complex die or CPU compute die) are partitioned
- The CCD is split into two chiplets (7nm process technology)
- The I/O chip is with 14nm process technology

Intel Lakefield

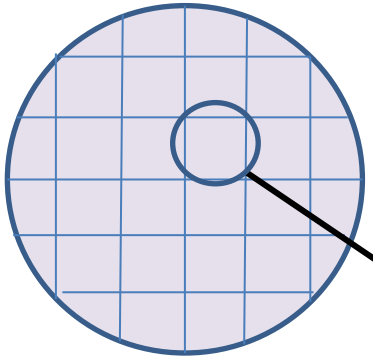
3D IC Integration on active TSV-interposer



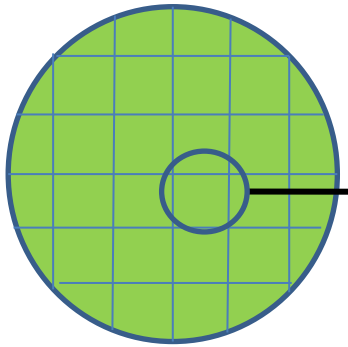
- The large CPU is split into 5 smaller CPUs (10nm process technology)
- The memory and graphics are partitioned
- All the tiles (or chiplets) are attached on an active interposer

Definition of Heterogeneous Integration (SiP)

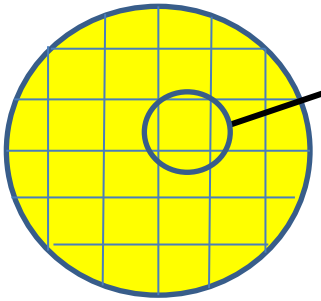
- Chip-1
- FAB-1
- 7nm
- 12”-wafer

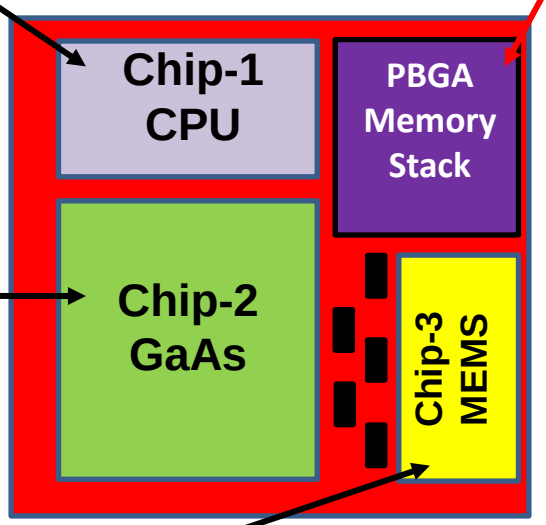


- Chip-2
- FAB-2
- 64nm
- 8”-wafer



- Chip-3
- FAB-3
- 100nm
- 6”-wafer





- Time-to-market
- Less IP issues
- Flexibility
- Low cost alternative than SoC
- Optimized signal integrity and power

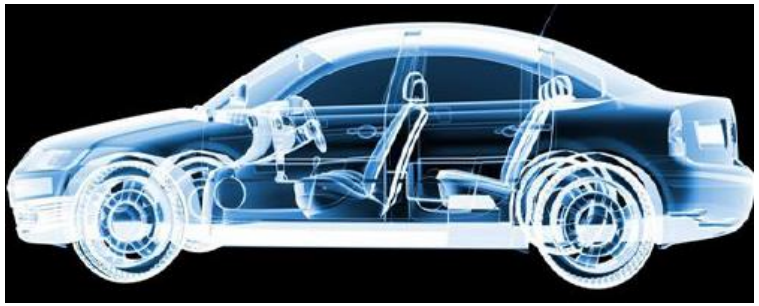
Heterogeneous integration uses packaging technology to integrate dissimilar chips, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem.

Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on Silicon Substrate (TSV-less Interposers)
- Heterogeneous Integrations on Fan-Out RDL Substrates
- Heterogeneous Integrations on Ceramic Substrates

Amkor Automotive SiP

- Large singulated body SiP
- Infotainment & ADAS
- Autonomous driving
- Computers in a car
- Increasing trend in designs

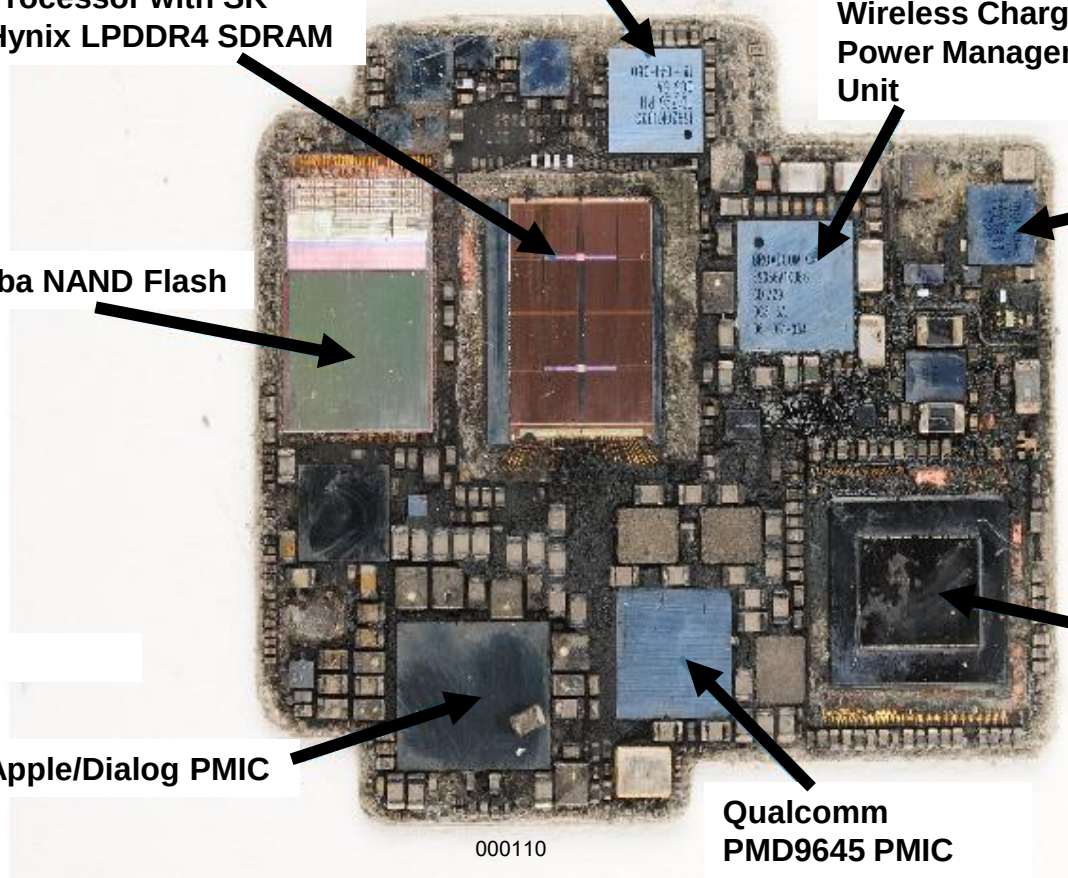


42.5 x 42.5 mm, Infotainment, Processor + DDR

55 x 72 mm, Network Switch, ASIC + Memory

Heterogeneous Integration on organic-substrate

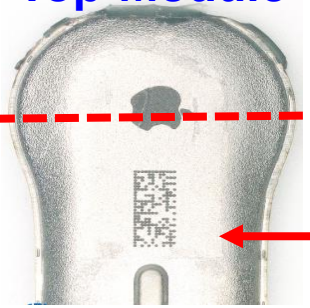
The Apple Watch is SiP and was Assembled by ASE (Universal Scientific Industrial – Shanghai)



Apple AirPods Pro
TWS (True Wireless Stereo)

Bottom-Module

Top-Module



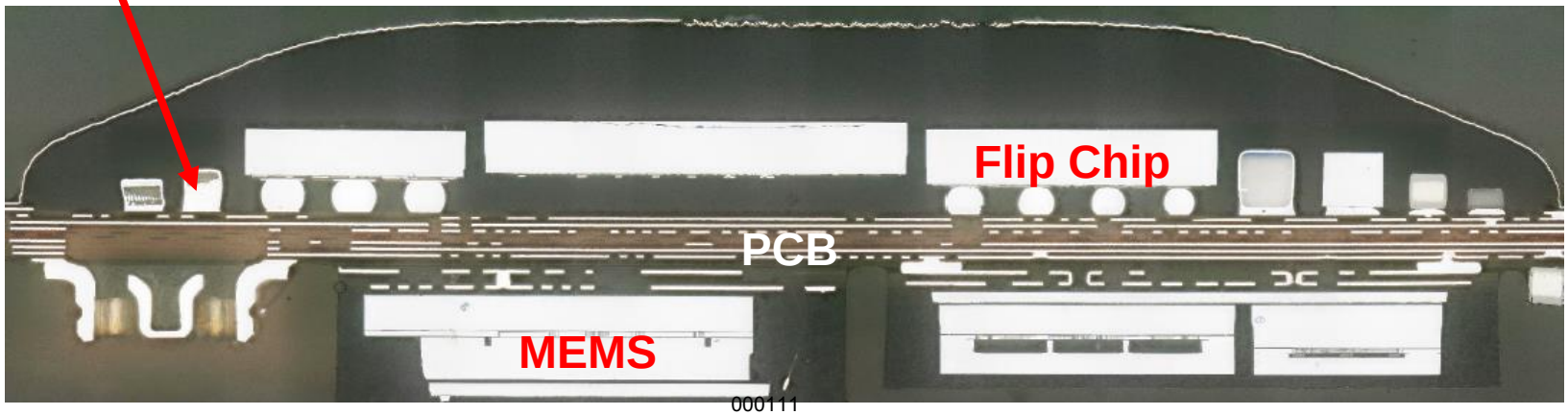
Cross Section

MEMS
Accelerometers

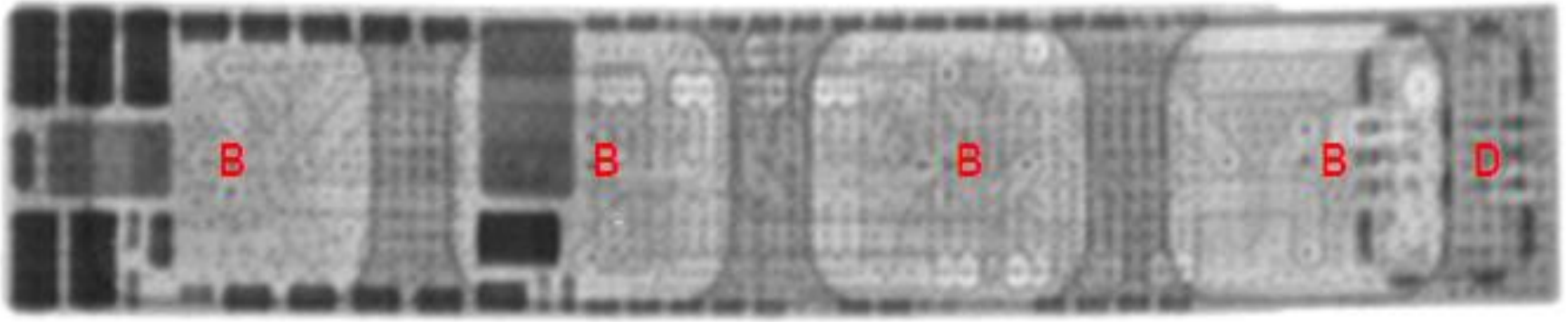
H1
(Processor)
Module

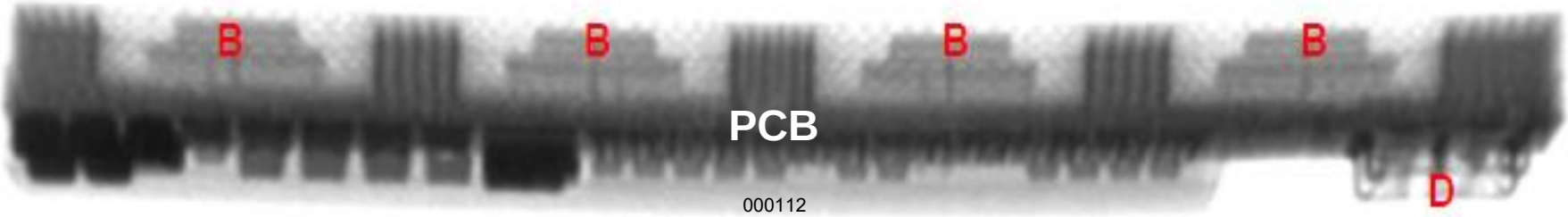
Audio
Module

SMT

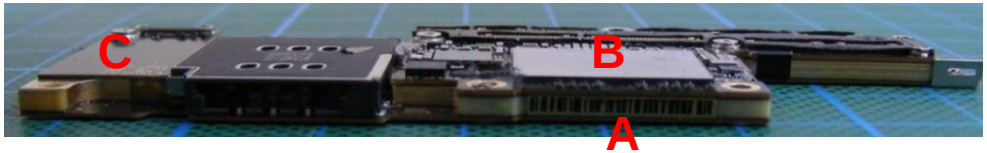


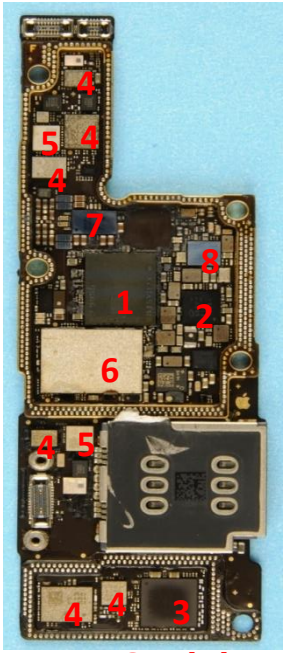
AiP (Antenna-in-package) in iPhone 12





Three Substrate-Like PCBs (SiPs) in iPhone

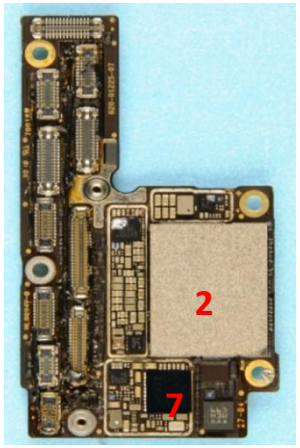


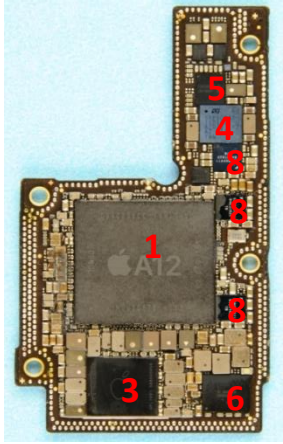


[1] Intel Baseband Chipset
[2] Intel PM IC
[3] Intel RF Transceiver
[4] Skyworks RF FEM
[5] Murata RF FEM (front-end module)
[6] USI WiFi/BT Module
[7] Broadcom Wireless Charger
[8] NXP NFC Controller

Rear PCB (A)

- 8L HDI, 4mSAP layers, 16cm^2
- Single-Sided Assembly
- Baseband, RF, WiFi/BT
- All components face inward

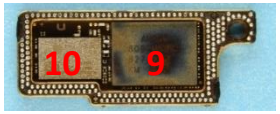




[1] Apple A12 Chipset
[2] Flash Memory
[3] Power Manager
[4] ST Power Manager
[5] Power Manager
[6] TI Battery Charger
[7] Audio Codec
[8] Audio Amplification
[9] Avago RF FEM
[10] Skyworks RF FEM

Front PCB 1 (B)

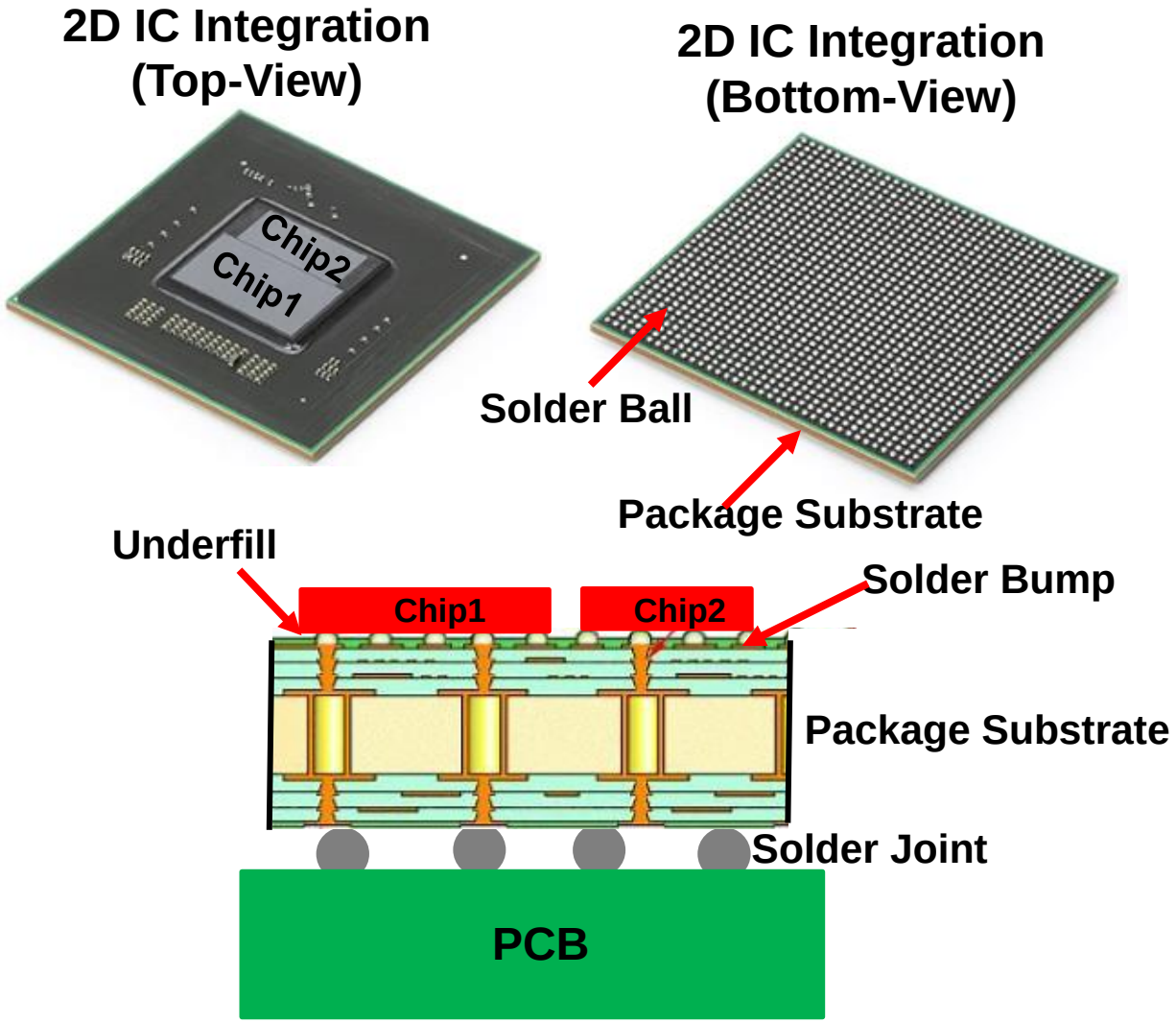
- 10L HDI, 6 mSAP layers, 10cm^2
- Double-Sided Assembly
- A12 CPU, Memory, Connectors
- A12 CPU faces inward



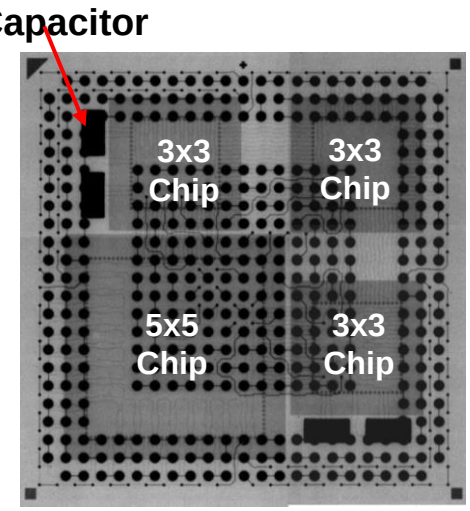
Front PCB 2 (C)

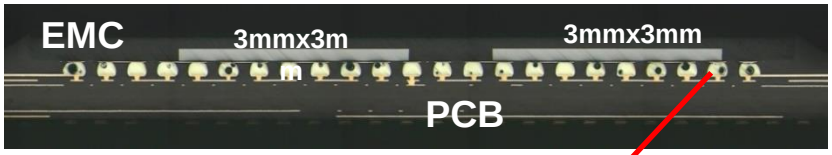
- 6L HDI, 2 mSAP layers, 2cm^2
- Double-Sided Assembly
- RF FEM, Connectors
- RF FEM face inward

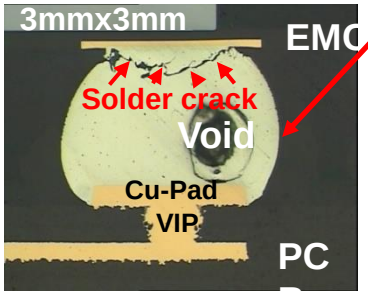
Flip Chip 2D IC Heterogeneous Integration on Organic Substrate

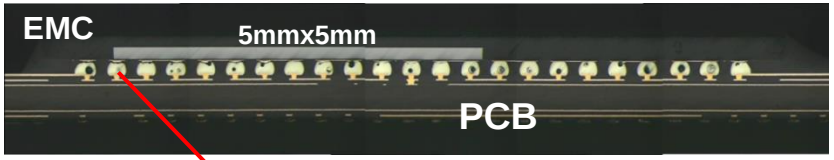


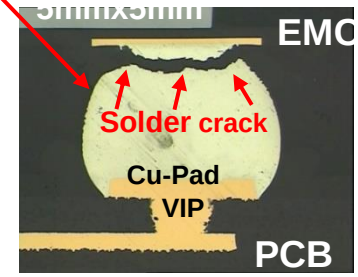
Fan-Out 2D IC Heterogeneous Integration of 4 Chips and 4 Capacitors on PCB

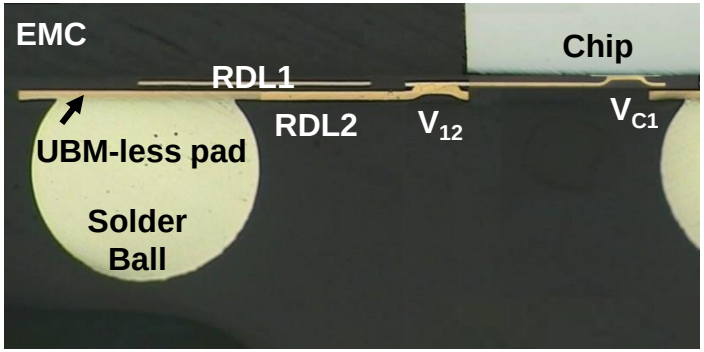






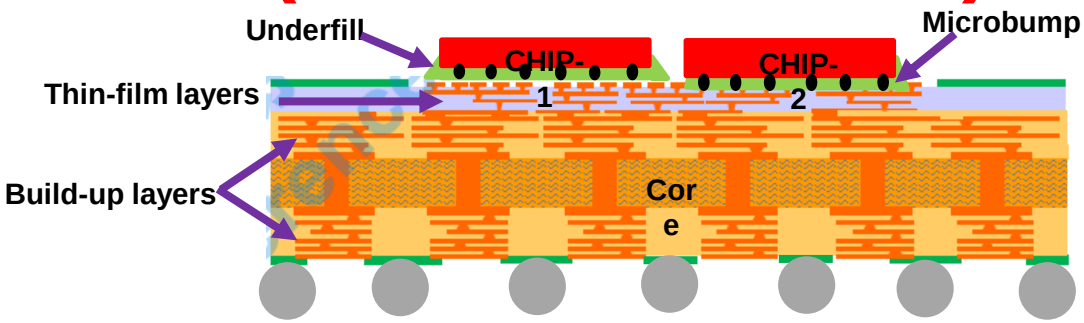


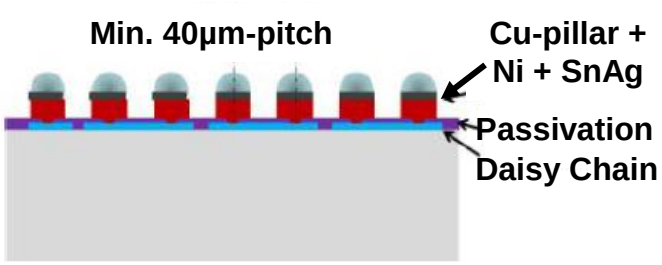




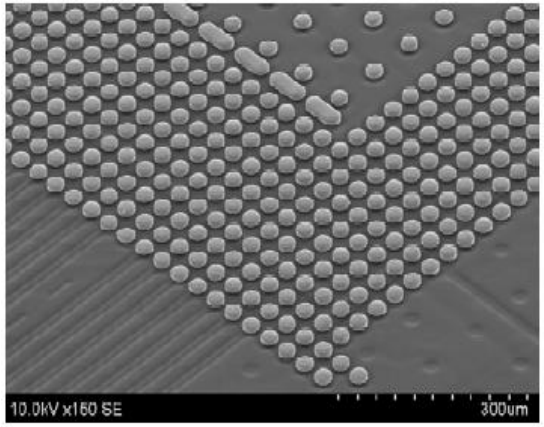
Thermal Cycling Test Results

2.1D IC Heterogeneous Integration (Shinko's i-THOP)

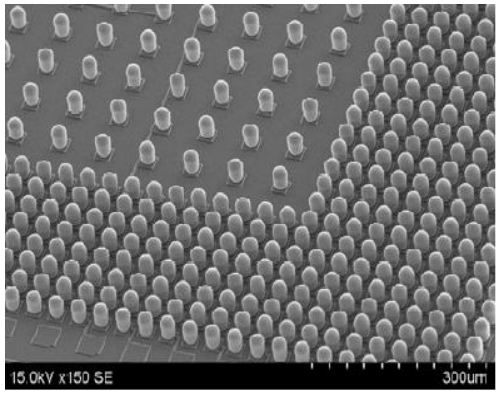




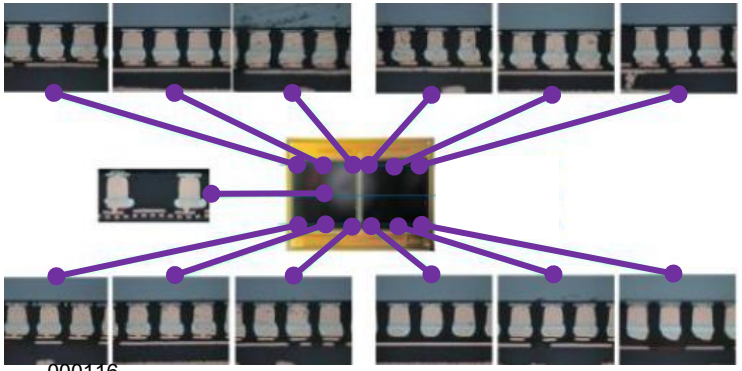
Schematic image of the test chip



40μm pitch flip chip bonding pads (25μm-diameter)



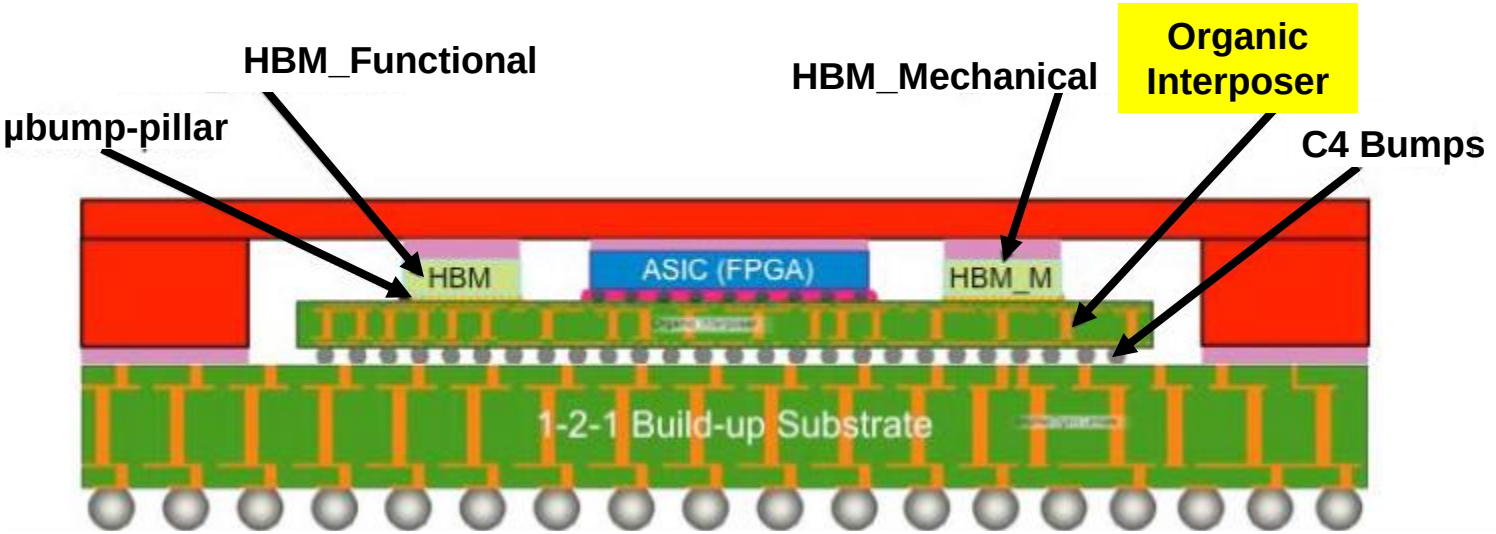
SEM image of test chip with μbumps

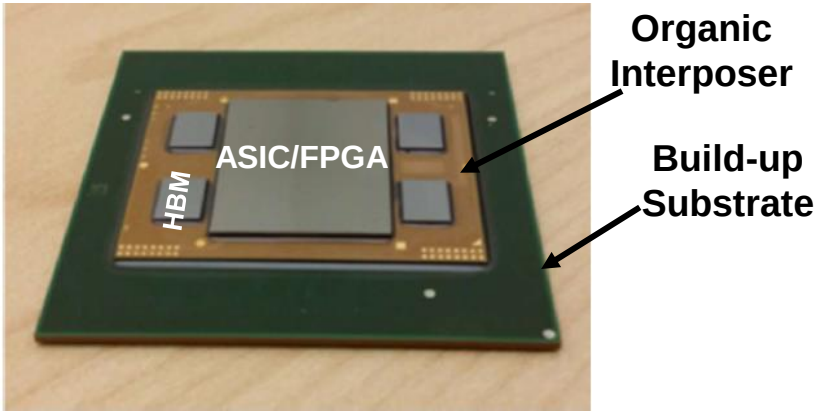


i-THOP (integrated thin-film high density organic package)

2.3D IC Heterogeneous Integration (Organic Interposer)

Li Li, Pierre Chia, Paul Ton, Mohan Nagar, Sada Patil, Jie Xue
Cisco Systems, Inc.
San Jose, CA 95134, U.S.A., e-mail: lili2@cisco.com

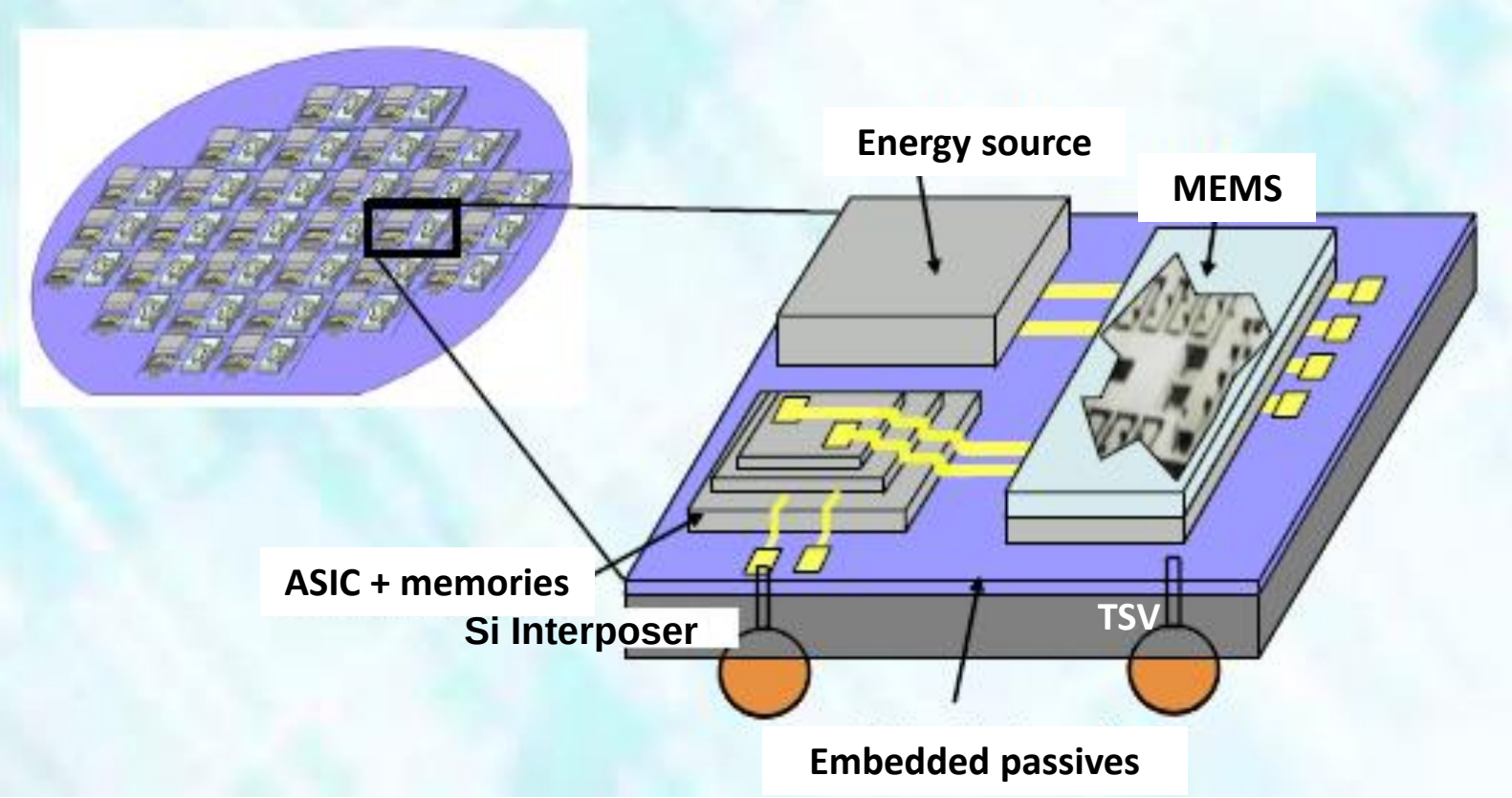




Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on Silicon Substrate (Bridges)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

Leti's Heterogeneous Integration: System-on-Wafer (SoW) – 2.5D IC Integration

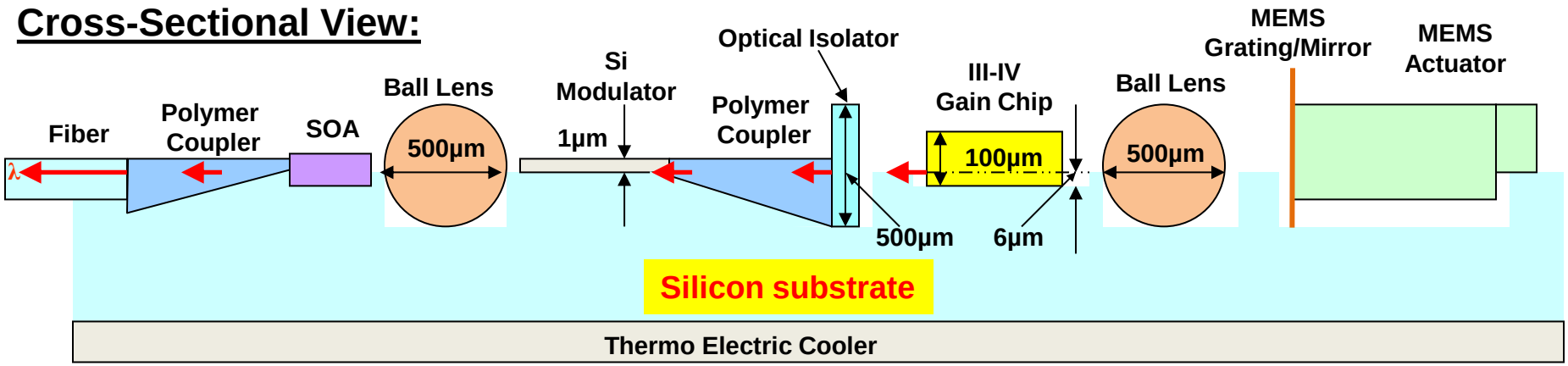


Heterogeneous Integration on Si-substrate
(TSMC called this: CoWoS)

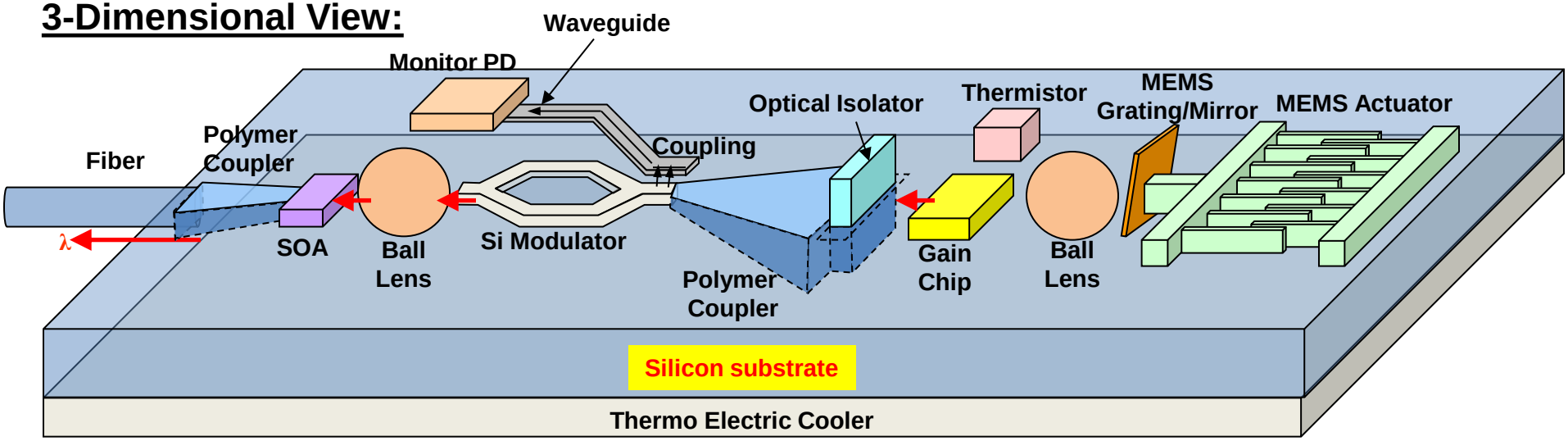
IEEE/ECTC2005 and 2006

IME's MEMS Based Tunable Laser Source, Gain Chip, and Si-Modulator on Si-Substrate

Cross-Sectional View:

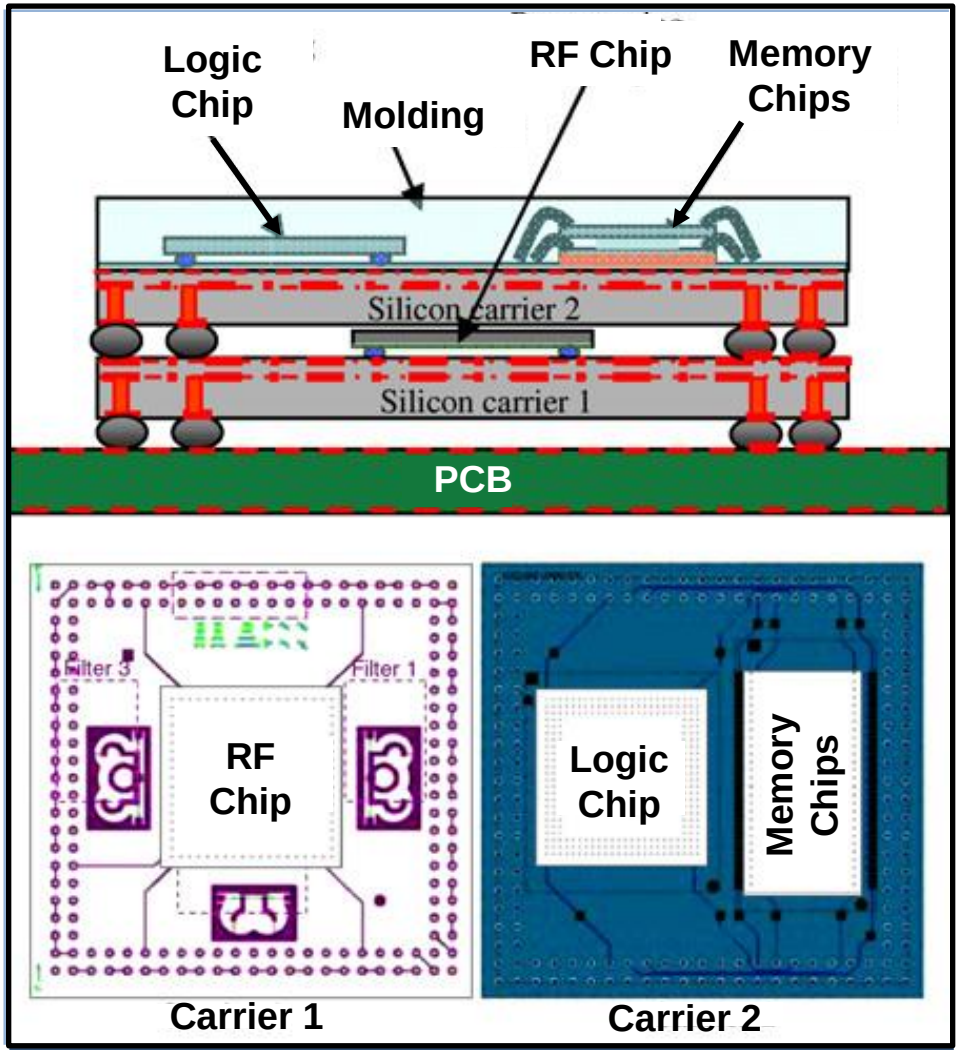


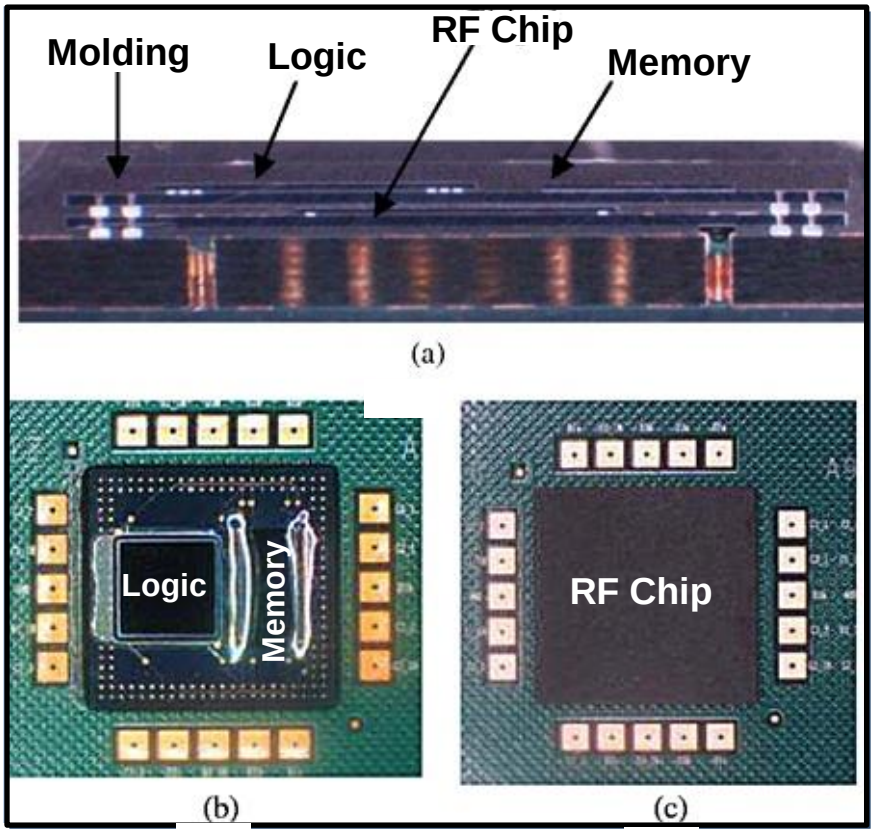
3-Dimensional View:



Heterogeneous Integration on Si-Substrate

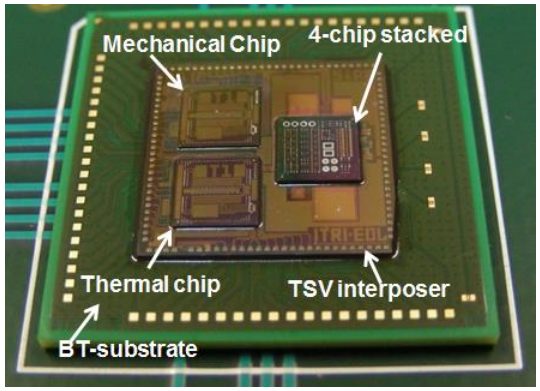
IME's Heterogeneous Integration of RF Chip, Logic chip, and Memory chips

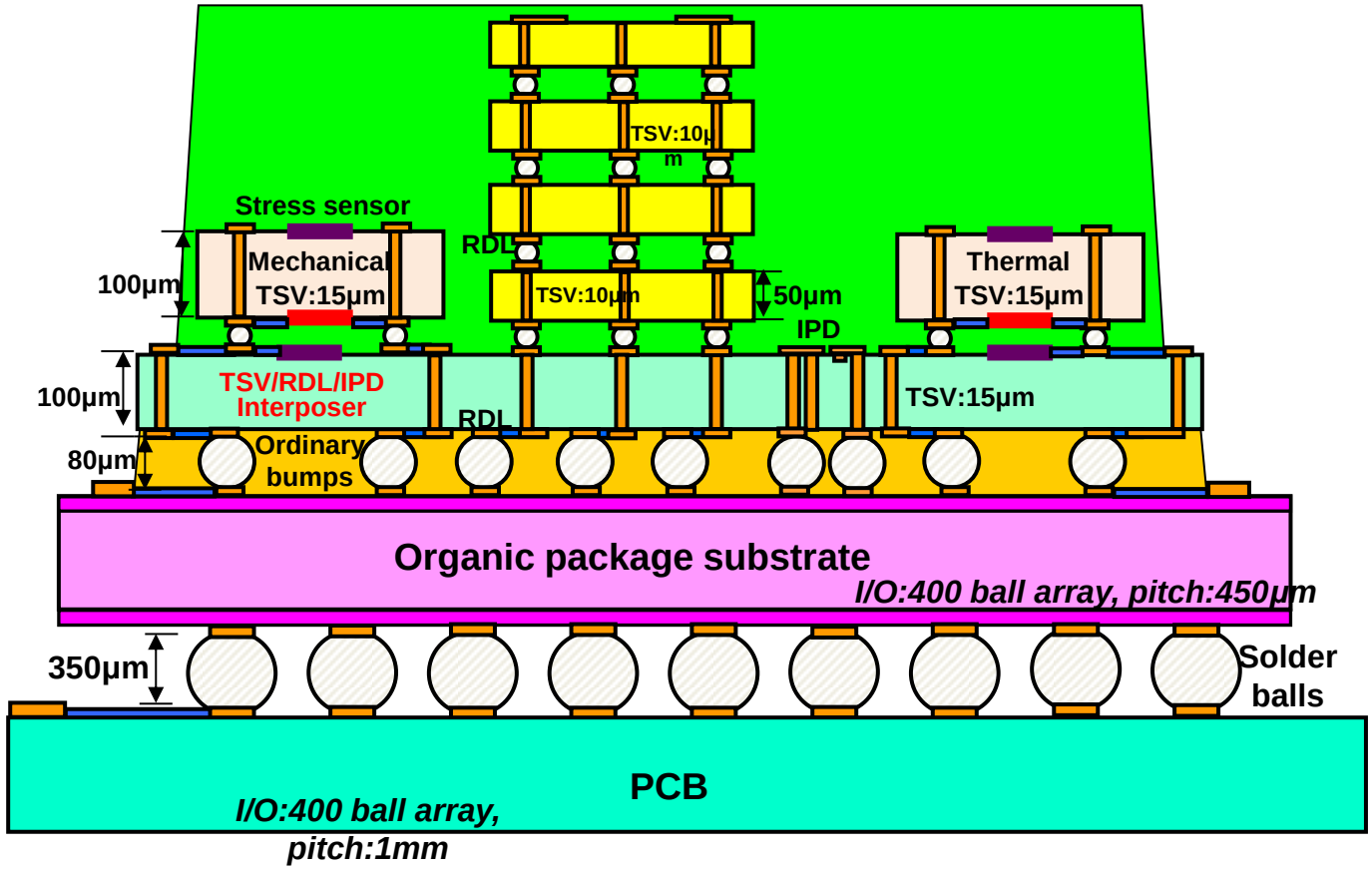




ECTC2008 and IEEE Trans. 2010.

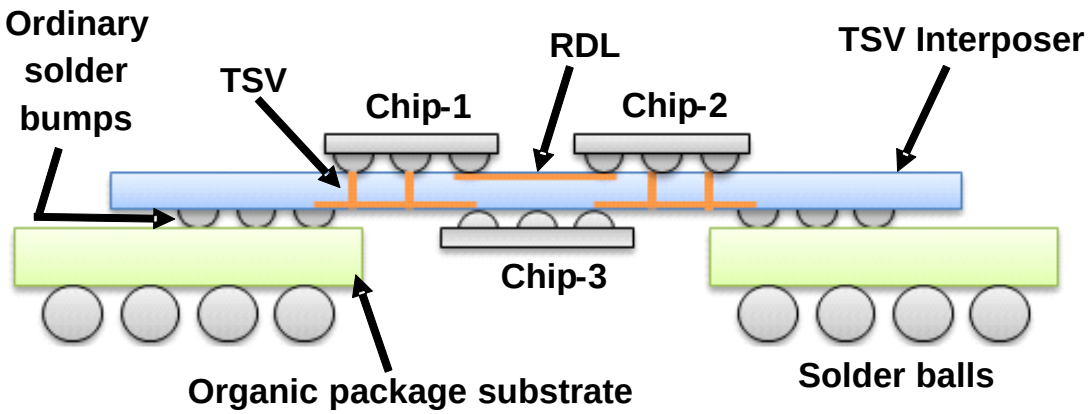
ITRI's 2.5D IC Integration

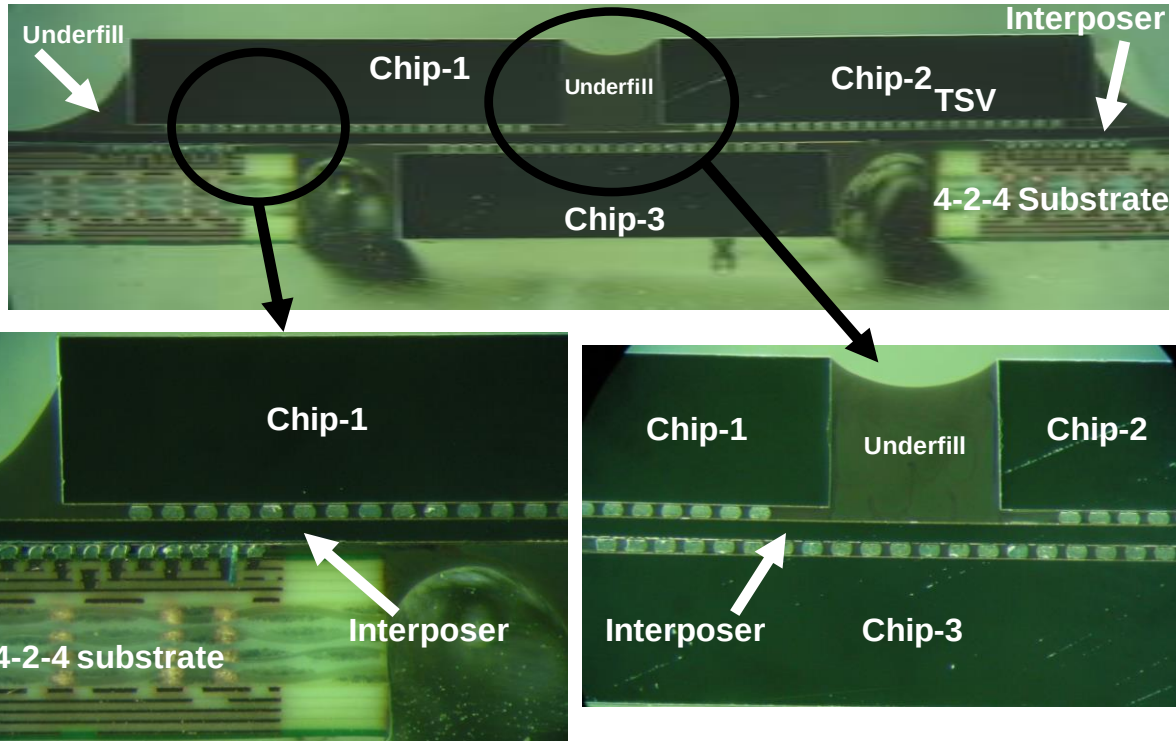




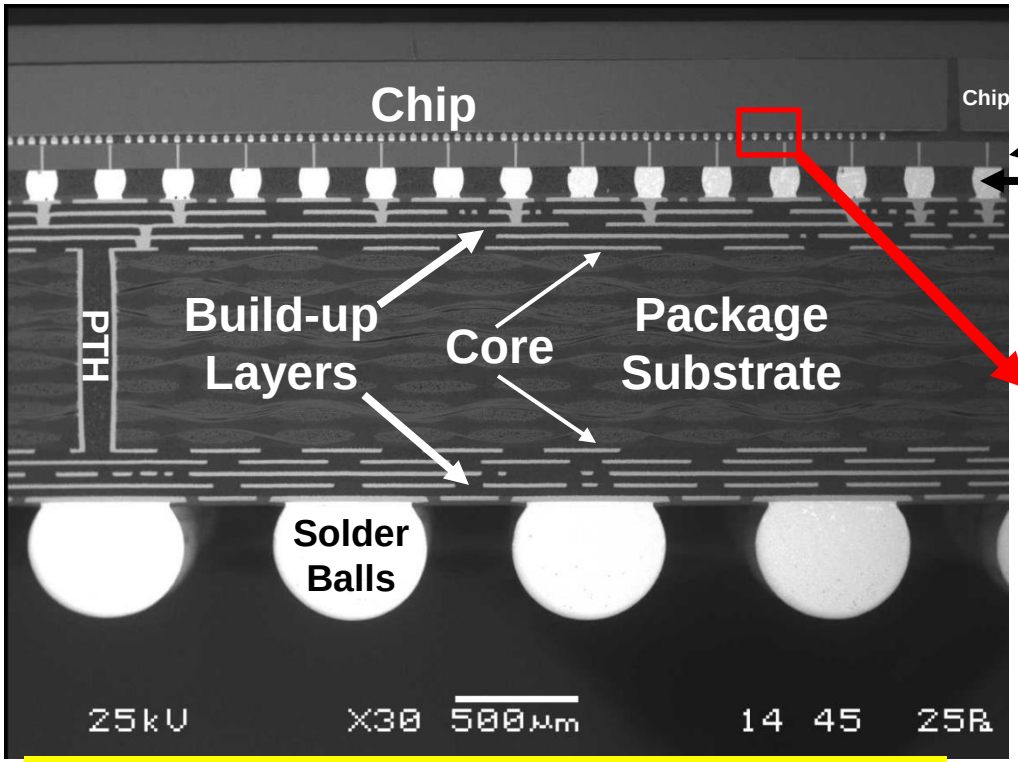
IMAPS Trans. 2011 and ECTC2012

ITRI/Rambus' Heterogeneous Integration of Chips

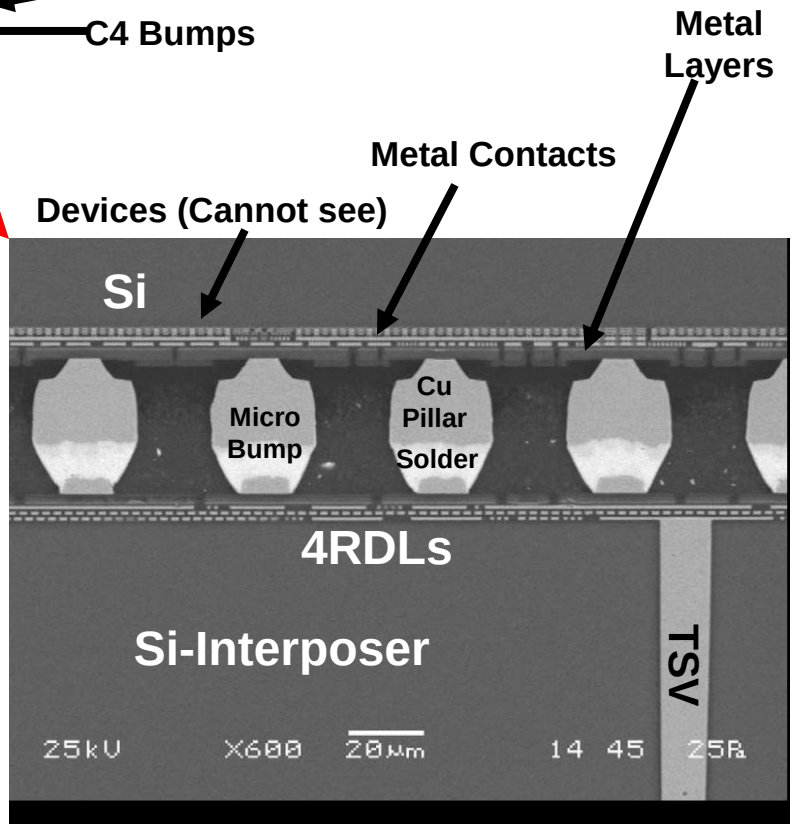




2.5D IC Integration with FPGA (Xilinx/TSMC)



CoWoS (chip on wafer on substrate)

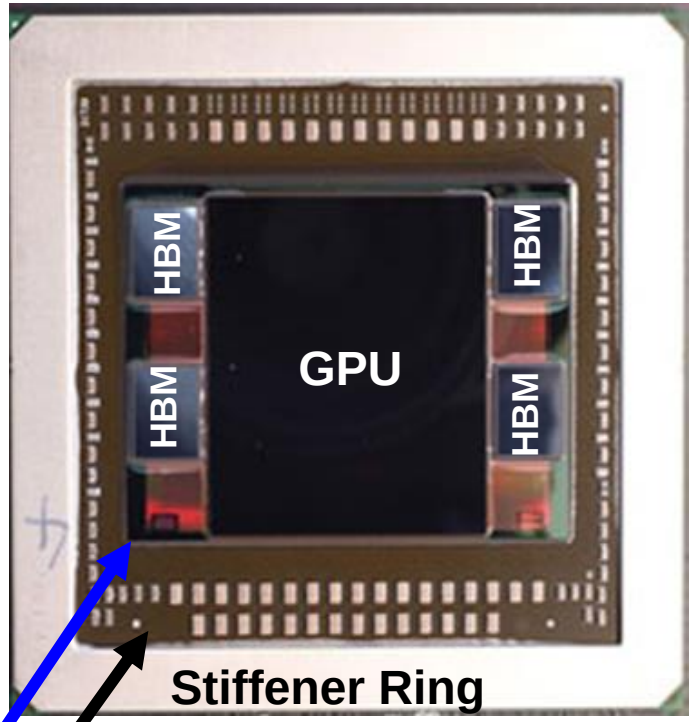


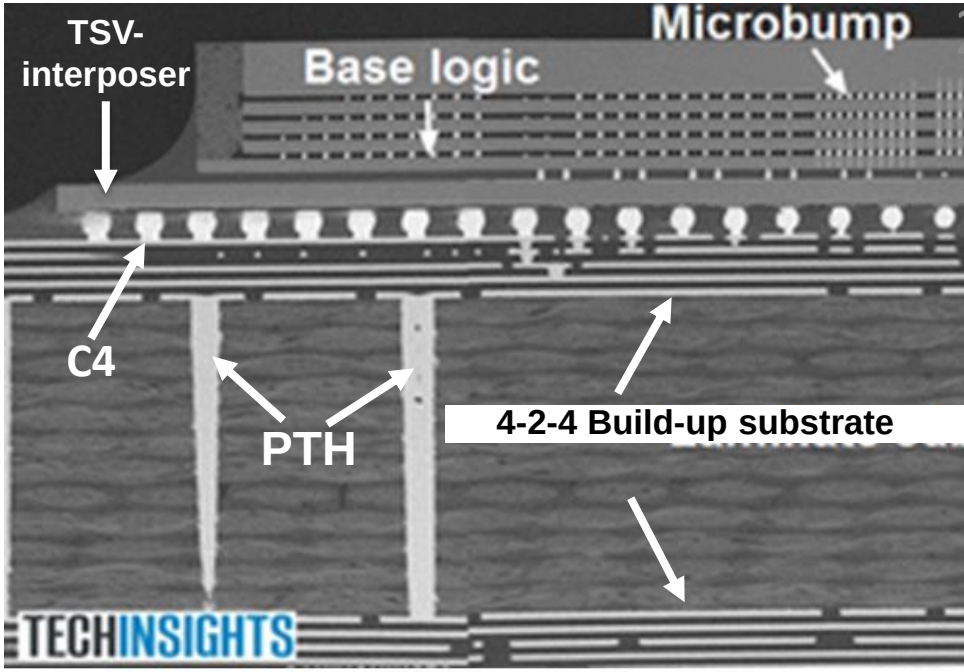
Xilinx Virtex-7 HT FPGAs shipped in 2013.

- RDLs: 0.4µm-pitch line width and spacing
- Each FPGA has >50,000 µbumps on 45µm pitch
- Interposer is supporting >200,000 µbumps

AMD's GPU (Fiji), Hynix's HBM, and UMC's Interposer

The GPU (23mm x 27mm) is fabricated by TSMC's 28nm Process technology



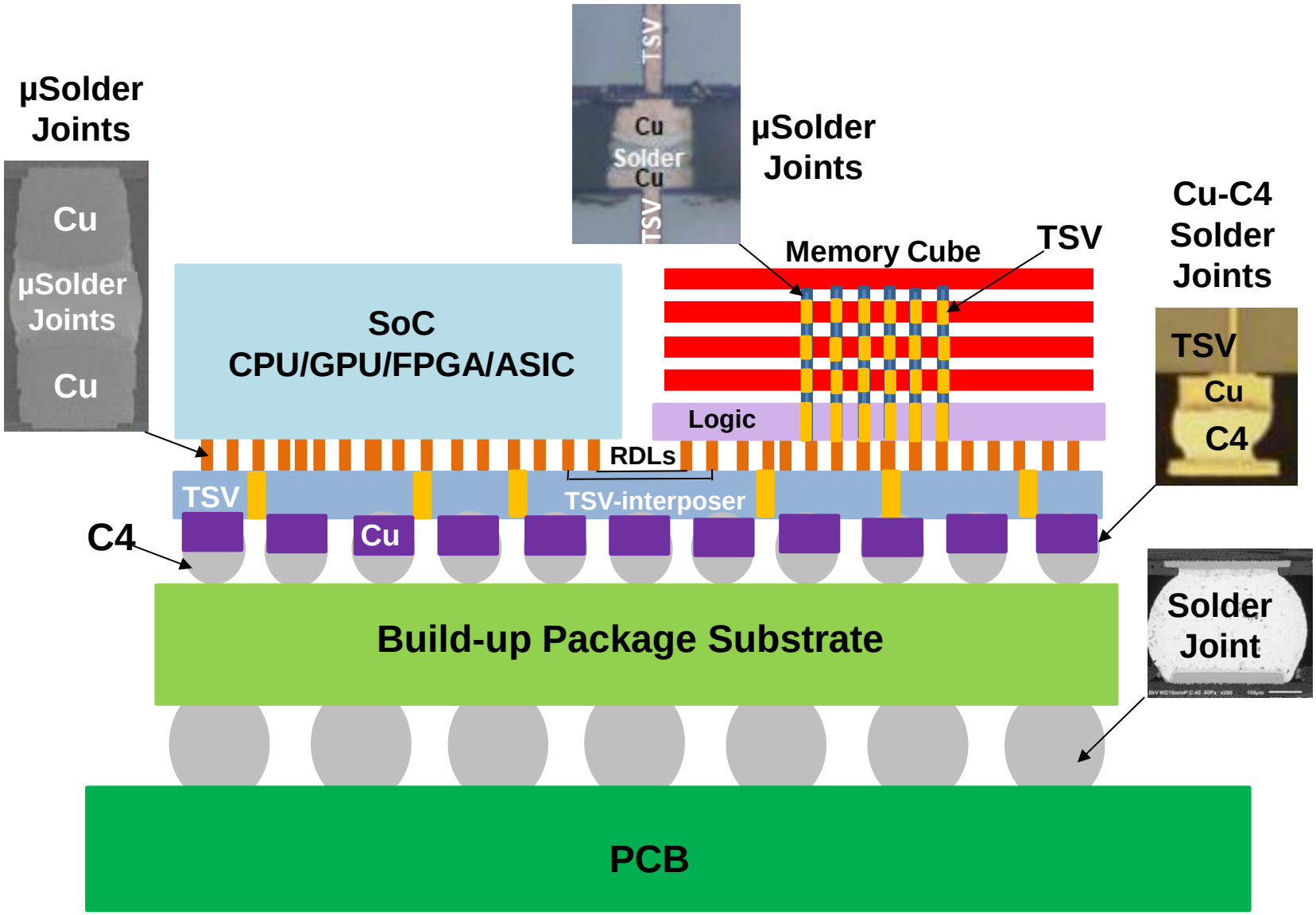


The Organic Substrate (54mm x 55mm) is with 2111 balls at 1.2mm pitch

The Si-interposer (28mm x 35mm) is fabricated by UMC's 65nm process technology

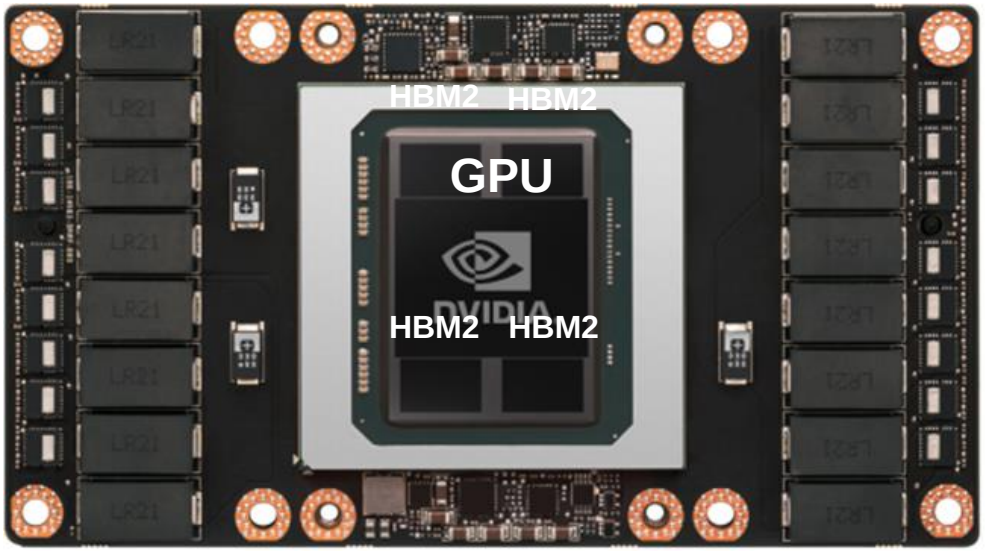
Shipped 2015

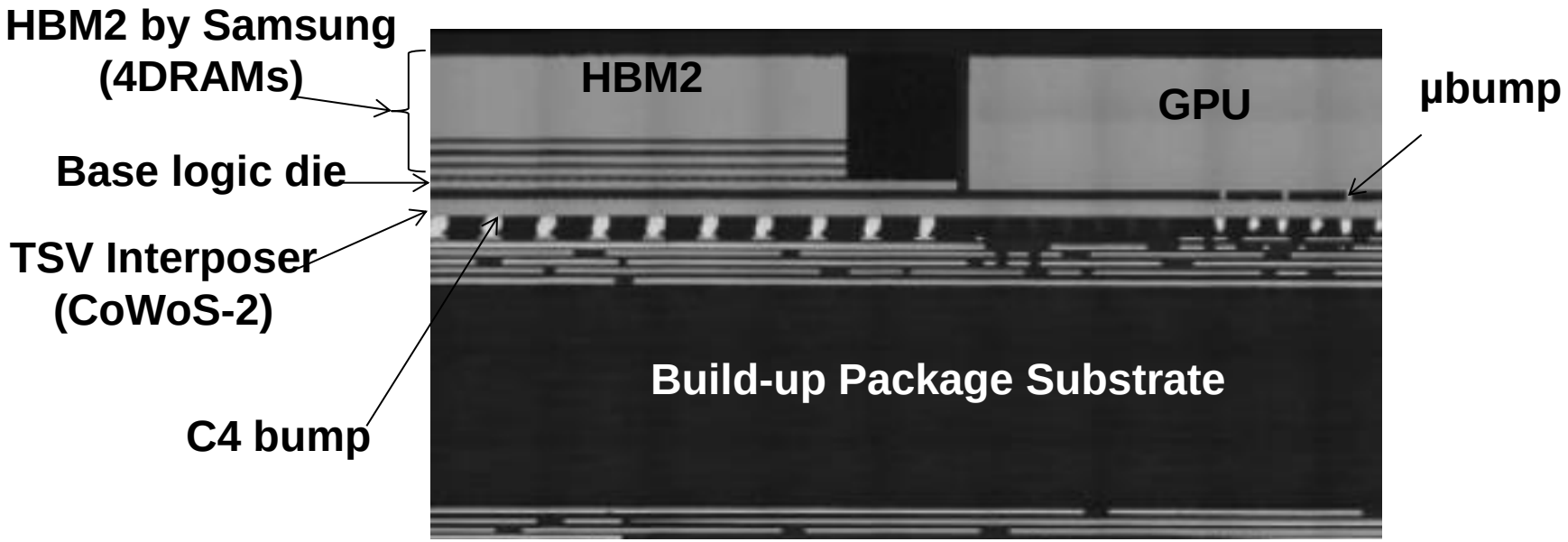
TSMC's CoWoS-2 for HPC Driven by AI and 5G



Semiconductors for HPC applications driven by AI and 5G

NVidia's P100 with TSMC's CoWoS-2 and Samsung's HBM2



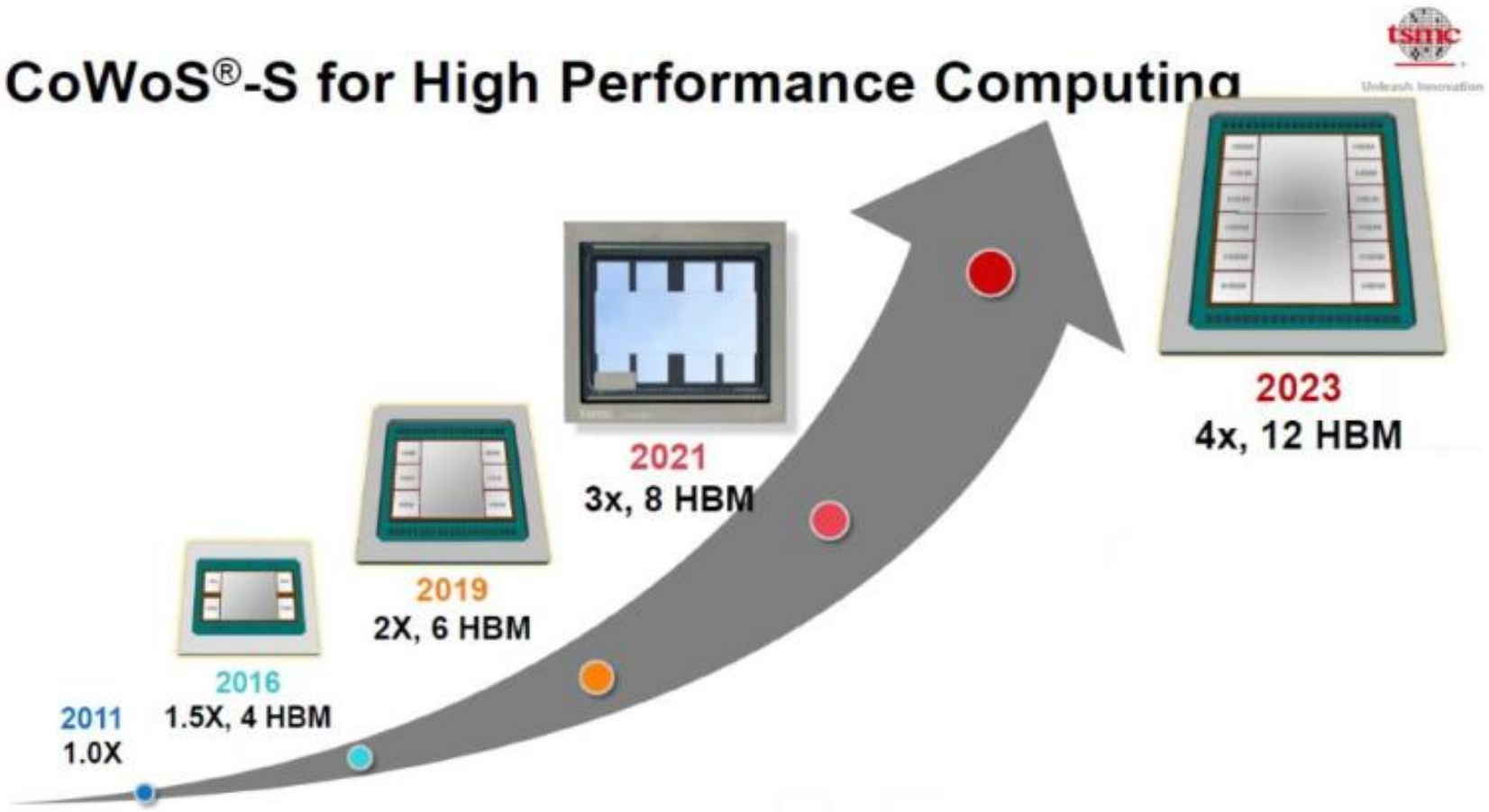


Shipped 2016/17

000127

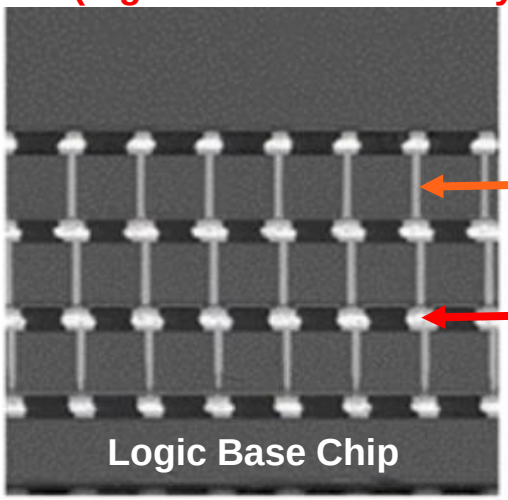
Heterogeneous Integration on Si-Substrate

TSMC's Roadmap on CoWoS



3D IC Integration: HBM

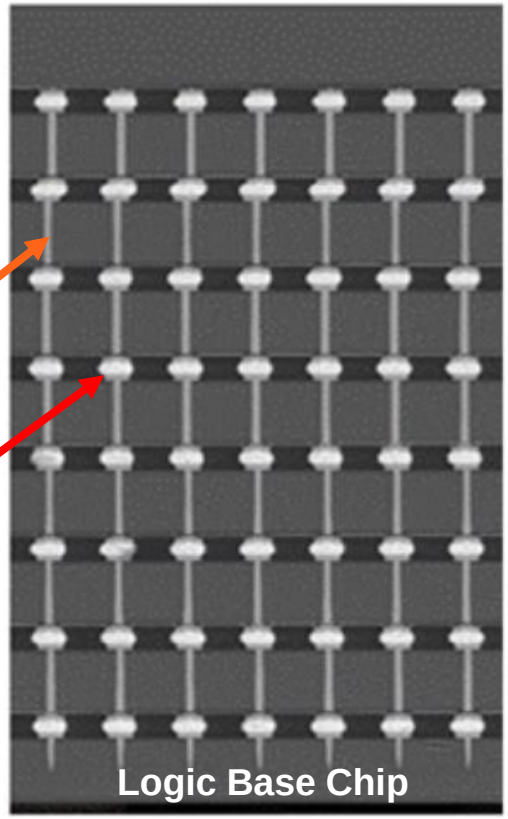
HBM (high bandwidth memory)



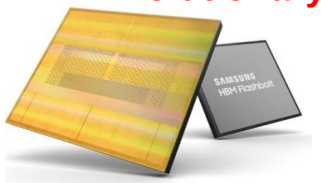
TSV

µSolder Joint

HBM2



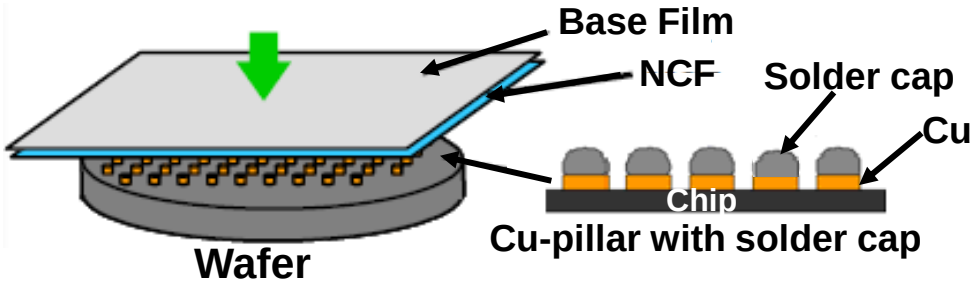
HBM2E
(HBM2 Evolutionary)



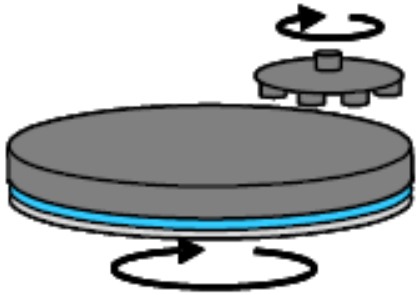
	HBM	HBM2 (Original)	HBM2/HBM2E (Current)	HBM3 (Upcoming)
Max Pin Transfer Rate	1Gbps	2Gbps	2.4Gbps	?
Max Capacity	4GB	8GB	24GB	64GB
Max Bandwidth	128GBps	256GBps	307GBps	512GBps

Hybrid Memory Cube (HMC) Aug 28, 2018 to HBM

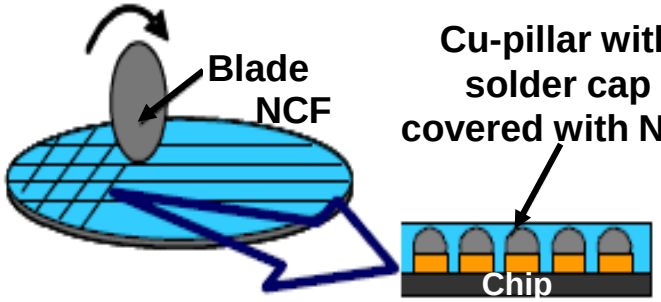
TCB with Non-Conductive Film



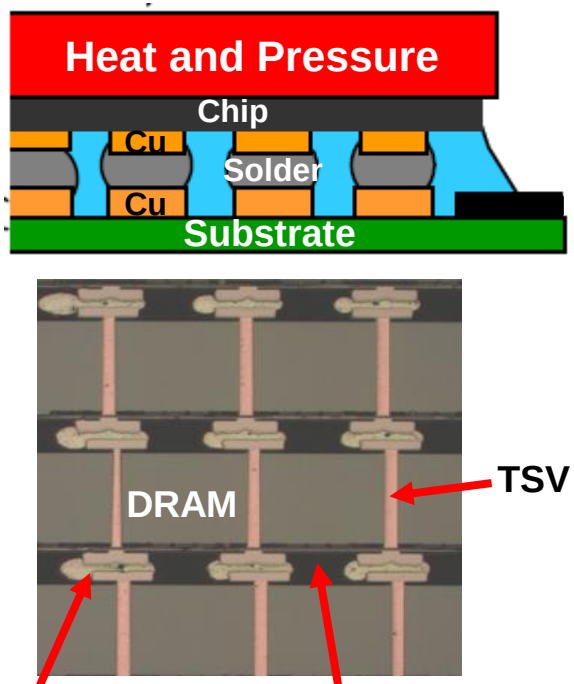
NCF Lamination for wafer



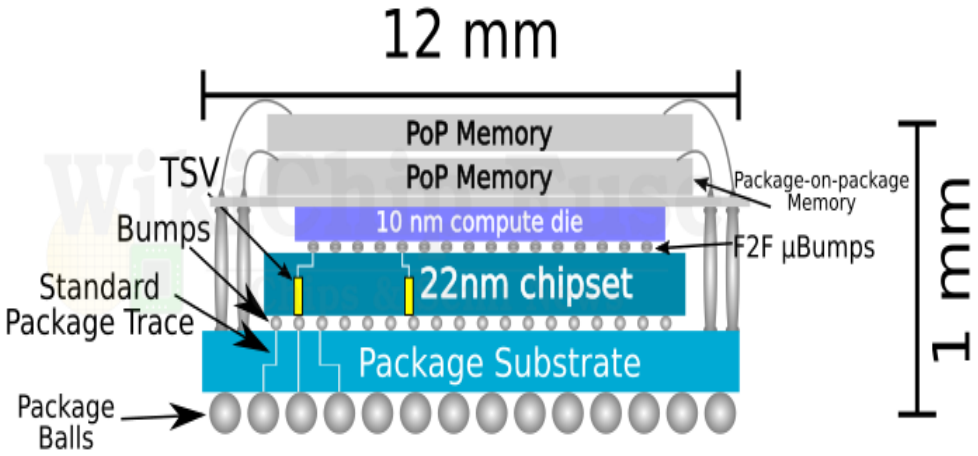
Cutting to wafer size and backgrinding

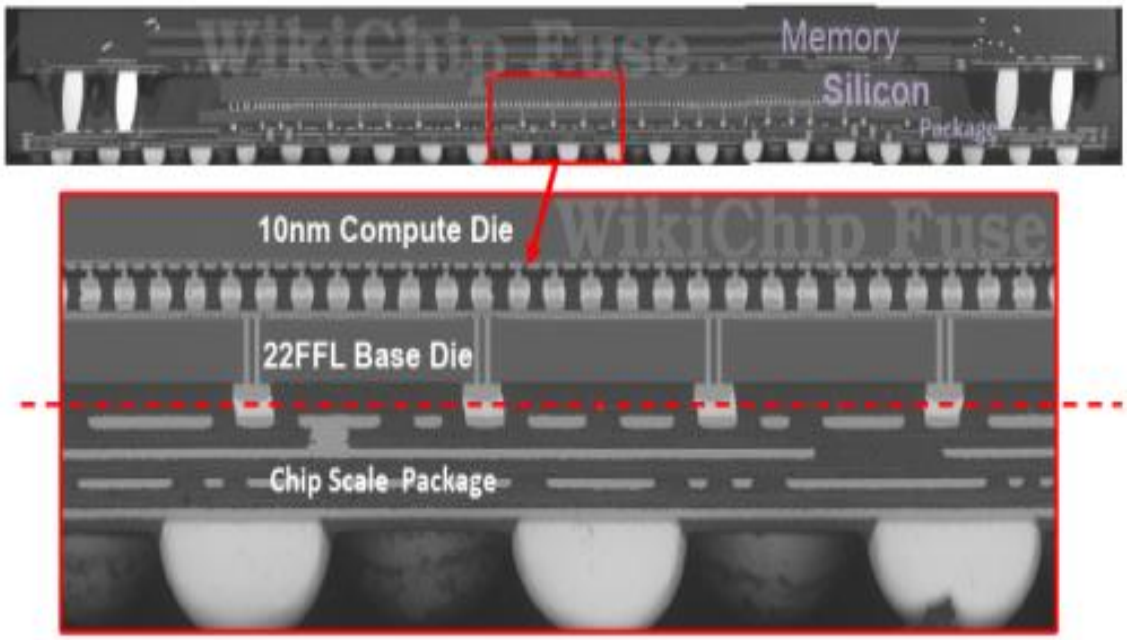


Removing based film and dicing the bumped wafer with NCF



FOVEROS (Lakefield for NBs) – Computer Chiplets Fabricated by Intel's 10nm process technology





3D IC Integration

10mm

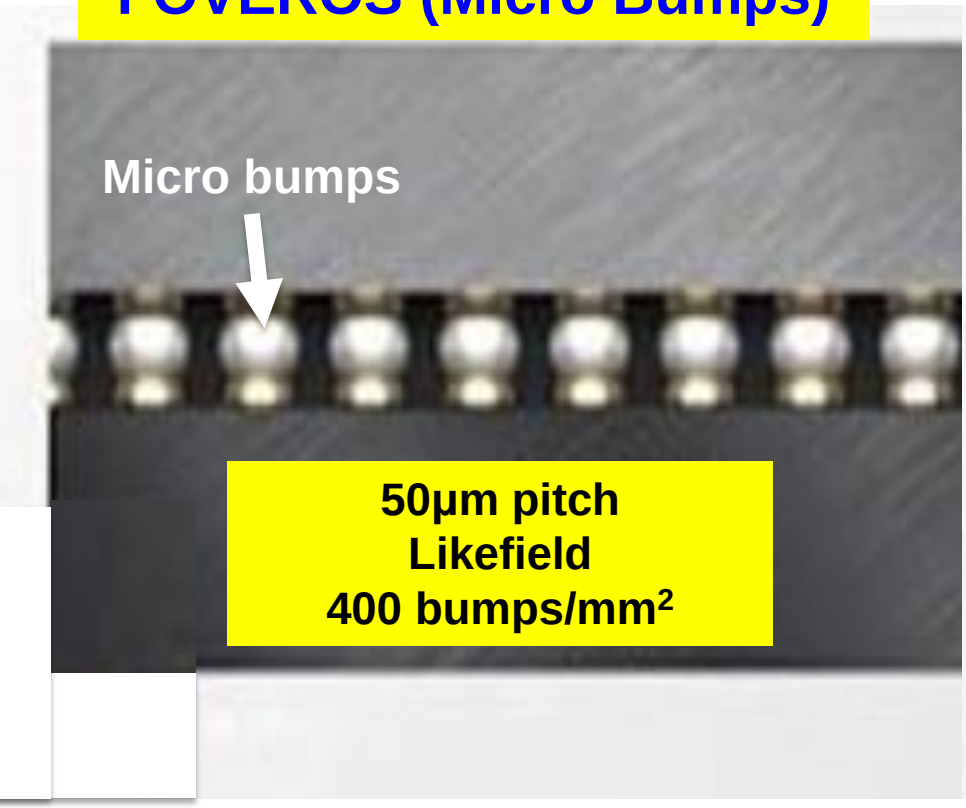
10mm

Intel Shipped in July 2020

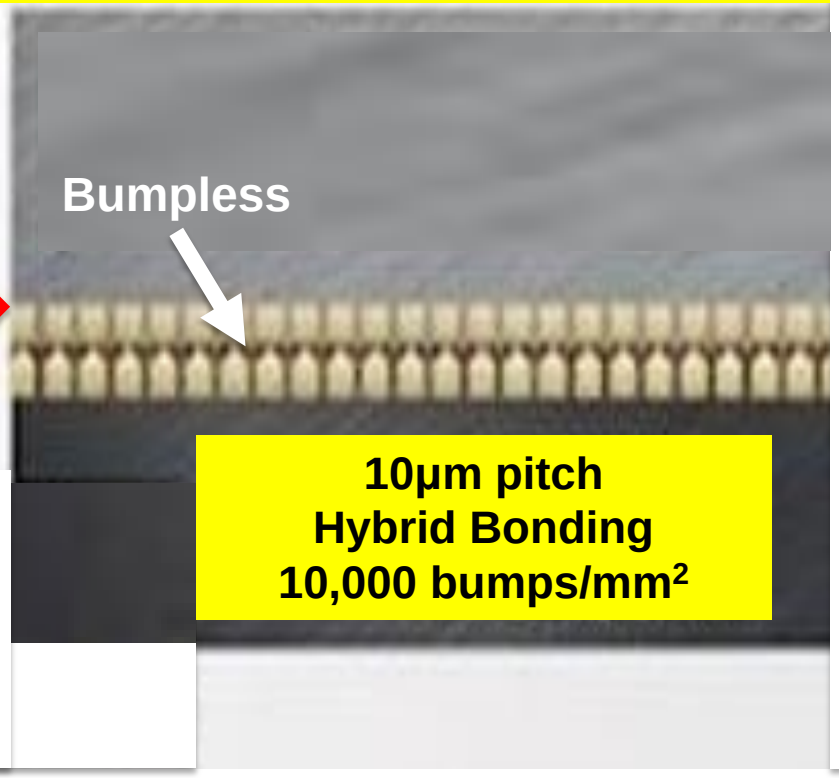
Intel's Hybrid Bonding

3D IC Integration

FOVEROS (Micro Bumps)



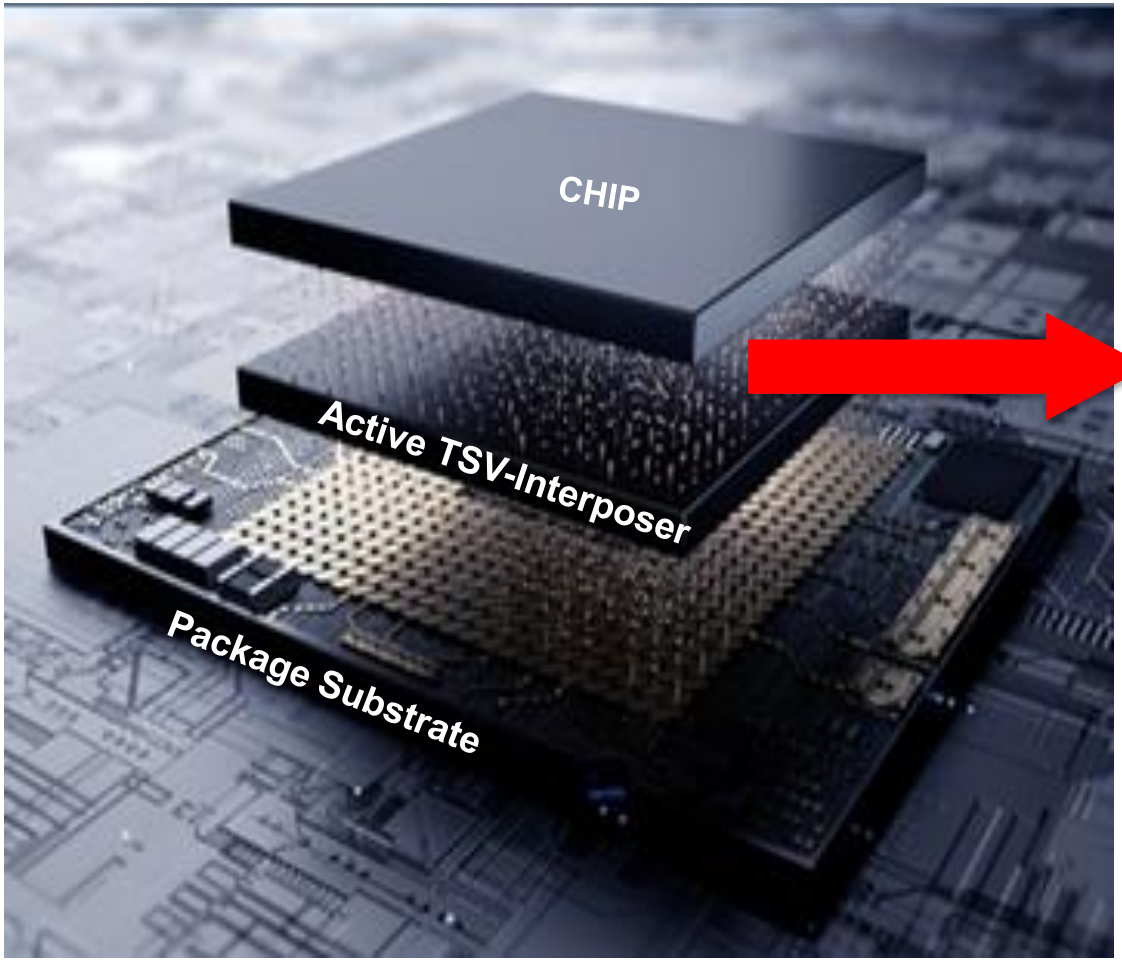
FOVEROS (Hybrid Bonding)



Intel Architecture Day, August 13, 2020

Chip design using 3D stacking architecture with Samsung's X-Cube technology

3D IC Integration



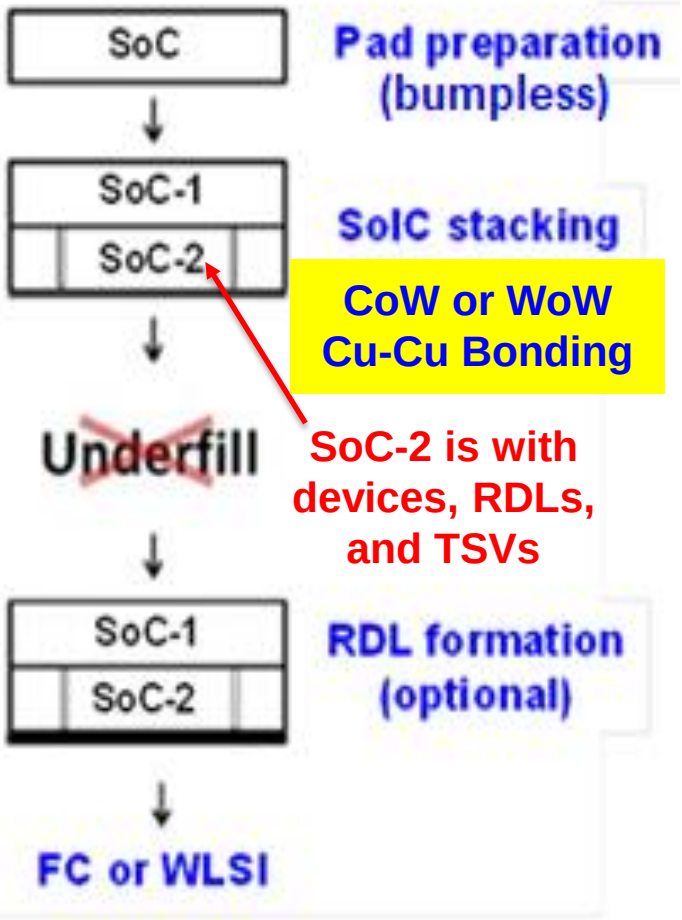
IEEE HOT CHIPS Symposium, Aug. 18, 2020

TSMC's 3DFabric

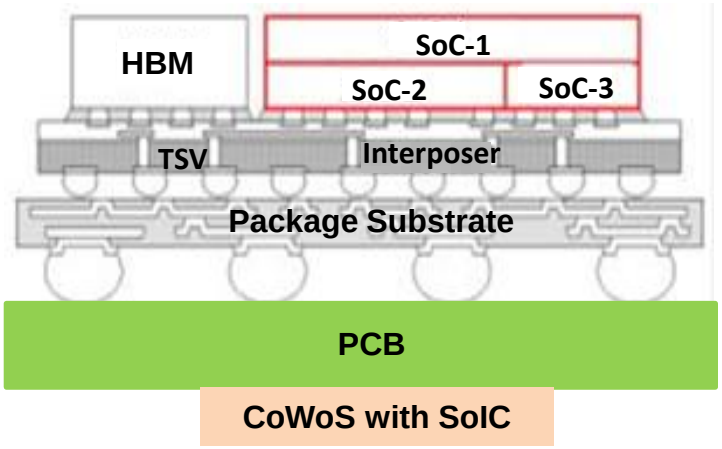
3DFabric is a 3D IC technology platform, which is an integration of SoIC, InFO, and CoWoS

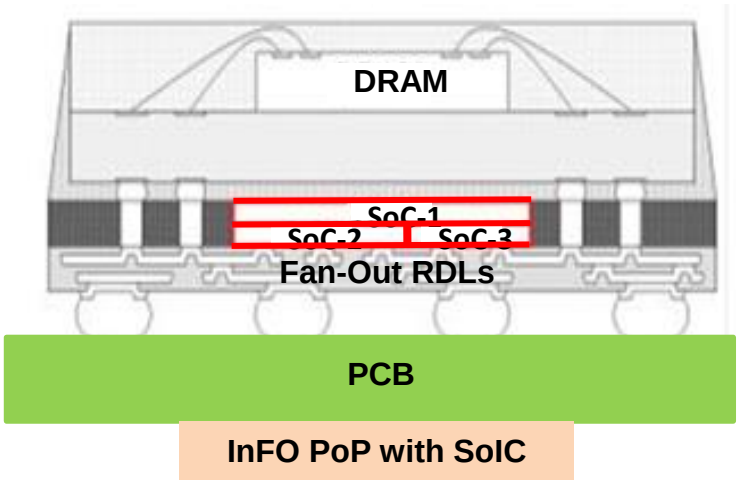
Frontend

SoIC



Backend





TSMC Annual Technology Symposium, August 25, 2020

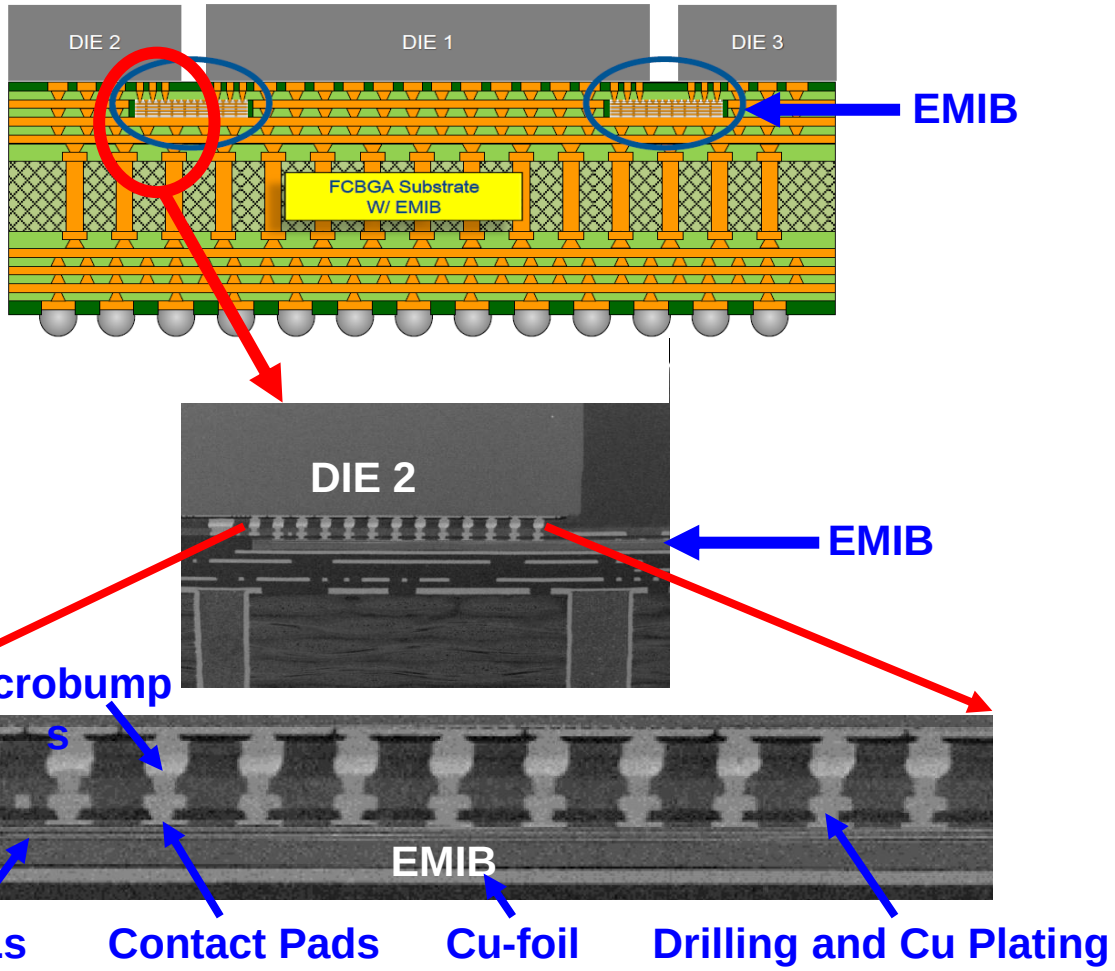
Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposer (Bridges)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

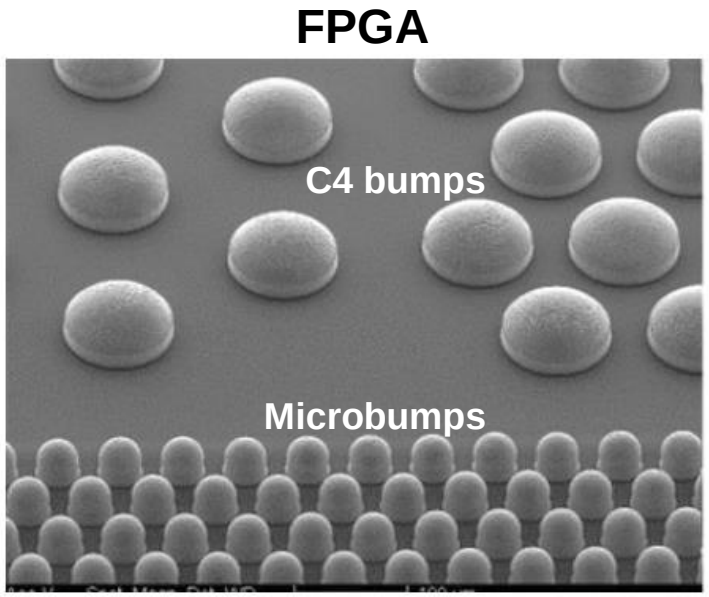
Embedded Multi-Die Interconnect Bridge (EMIB) – A High Density, High Bandwidth Packaging Interconnect

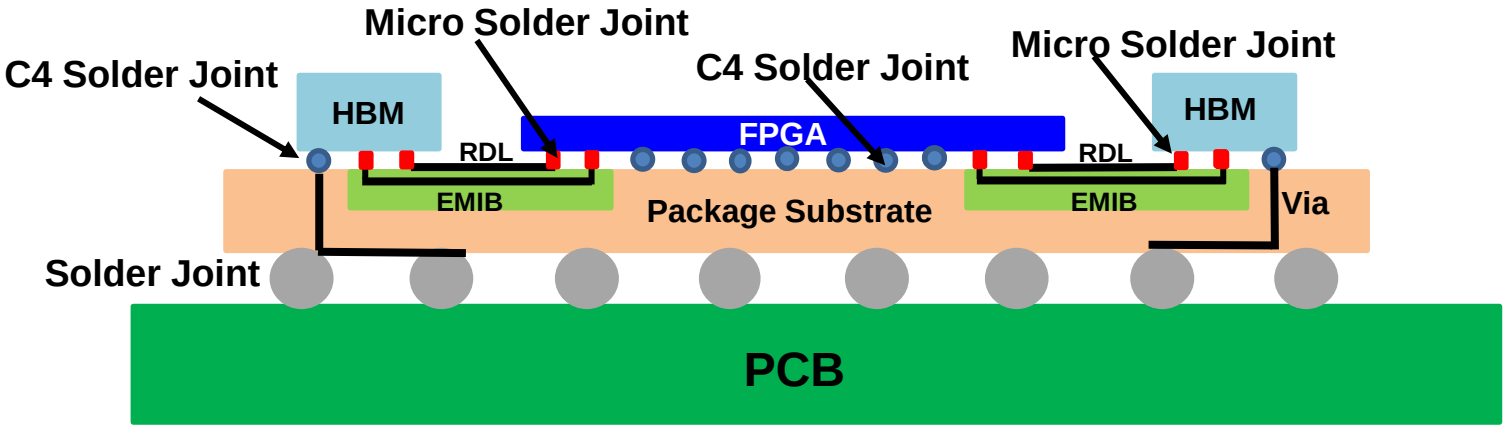
Ravi Mahajan, Robert Sankman, Neha Patel, Dae-Woo Kim, Kemal Aygun, Zhiguo Qian, Yidnekachew Mekonnen, Islam Salama, Sujit Sharan, Deepti Iyengar, and Debendra Mallik
Assembly Test Technology Development, Intel Corporation, Chandler, Arizona, USA
ravi.v.mahajan@intel.com

TSV-less Interposer

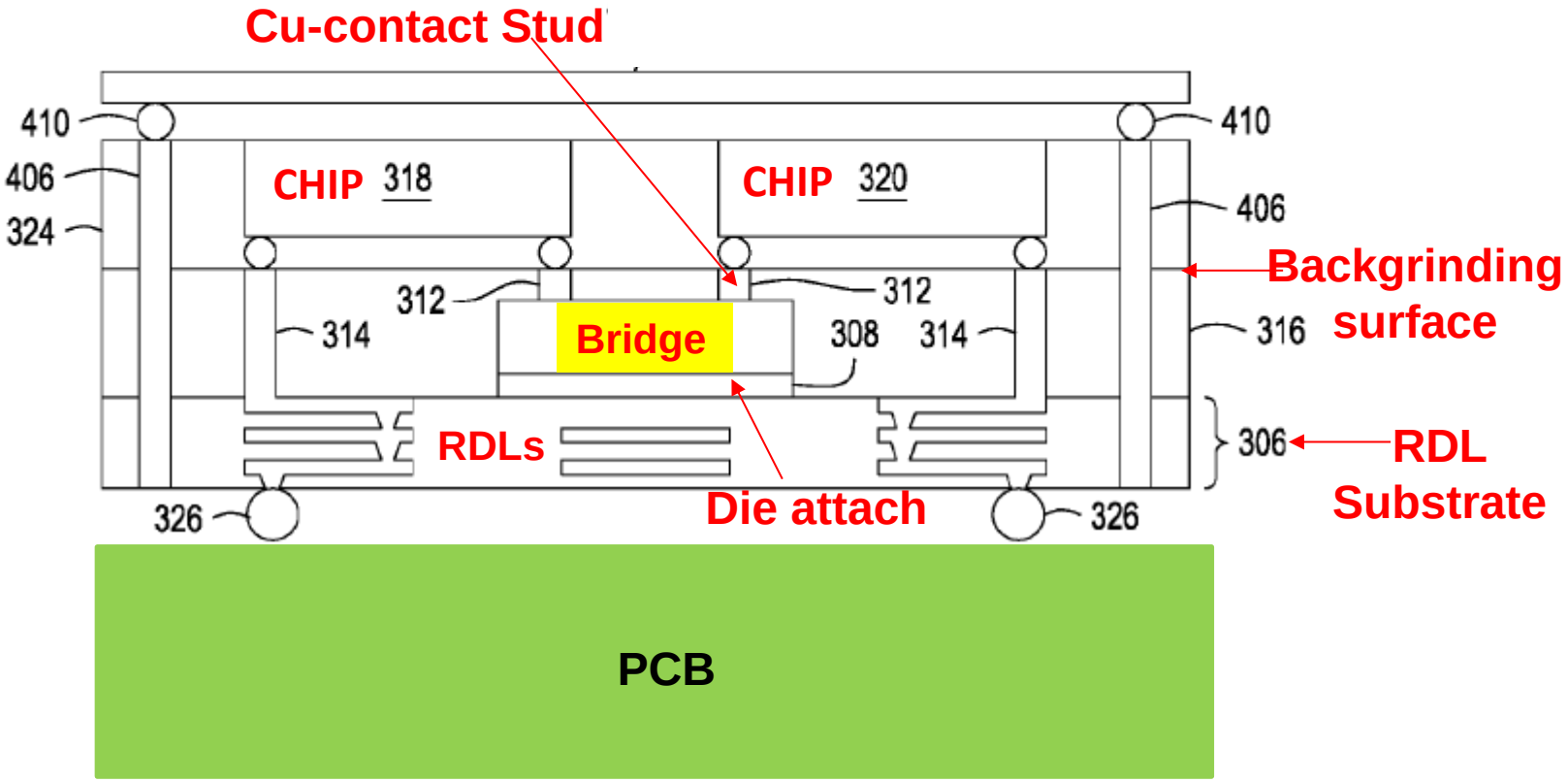


Intel's FPGA (Agilex) with EMIB





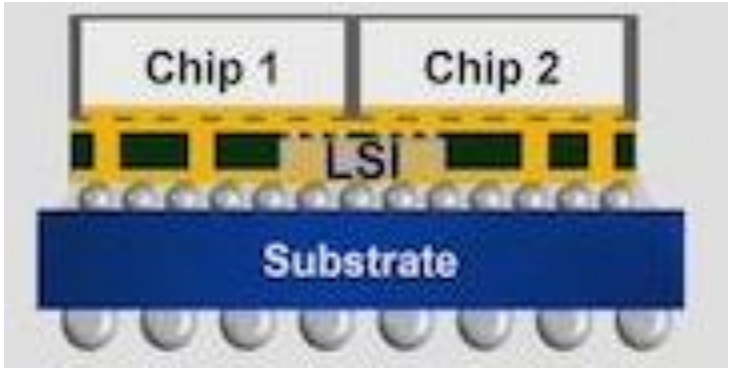
Fan-Out IC Integration with Bridge (Applied Materials)



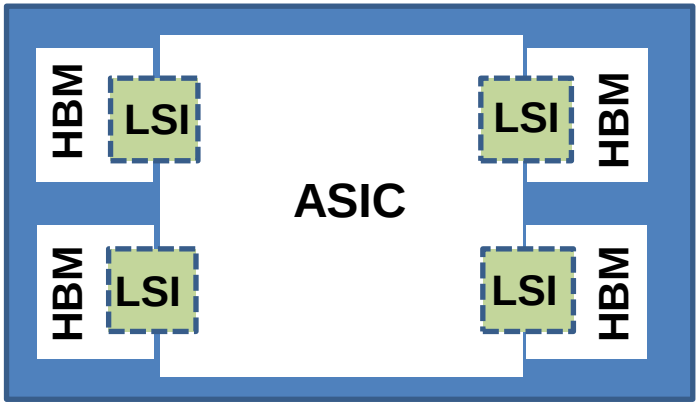
May 12, 2020 US 10,651,126 B2

TSMC's LSI (Local Silicon Interconnect)

CoWoS_LSI



InFO_LSI



TSMC Annual Technology Symposium, August 25, 2020

Classification of Heterogeneous Integrations

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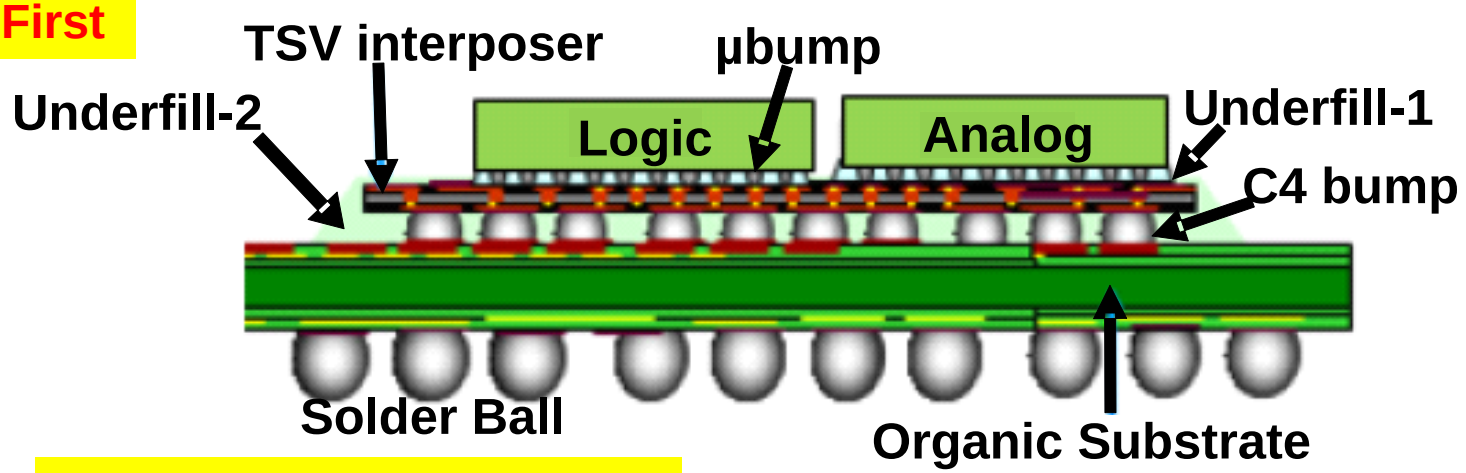
- Heterogeneous Integrations on TSV-less Interposer (Bridges)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

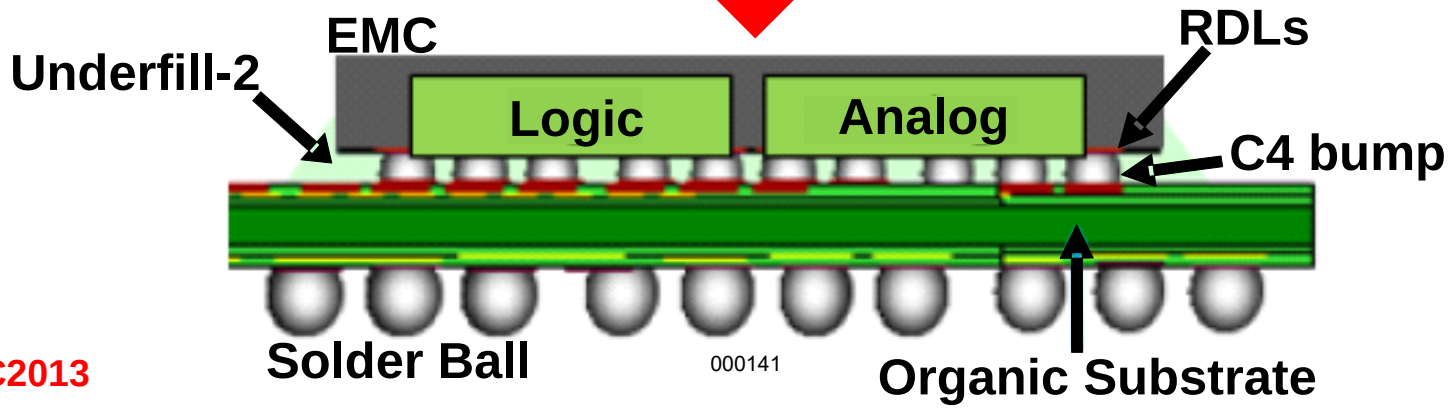
Fanout Flipchip eWLB (embedded Wafer Level Ball Grid Array) Technology as 2.5D Packaging Solutions

Seung Wook Yoon, Patrick Tang, Roger Emigh, Yaojian Lin, Pandi C. Marimuthu, and Raj Pendse
STATSChipPAC Ltd., 5 Yishun Street 23, Singapore 768442

Chip-First



- The µbump, underfill-1, and TSV-interposer are eliminated.
- The RDLs are made by fan-out technology.



Wafer Warpage Experiments and Simulation for Fan-out Chip on Substrate (FOCoS)

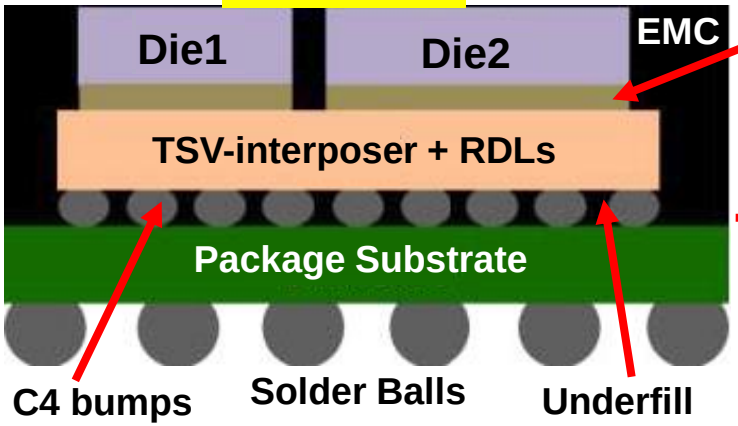
Yuan-Ting Lin, Wei-Hong Lai, Chin-Li Kao, Jian-Wen Lou, Ping-Feng Yang, Chi-Yu Wang, and Chueh-An Hseih*

Advanced Semiconductor Engineering (ASE), Inc.

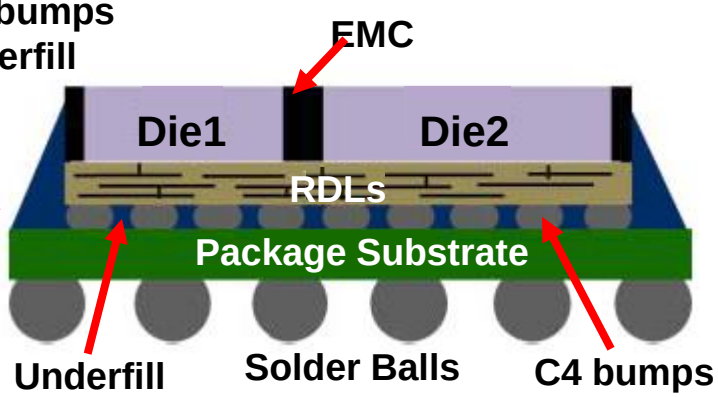
e-mail: Adren_Hsieh@aseglobal.com

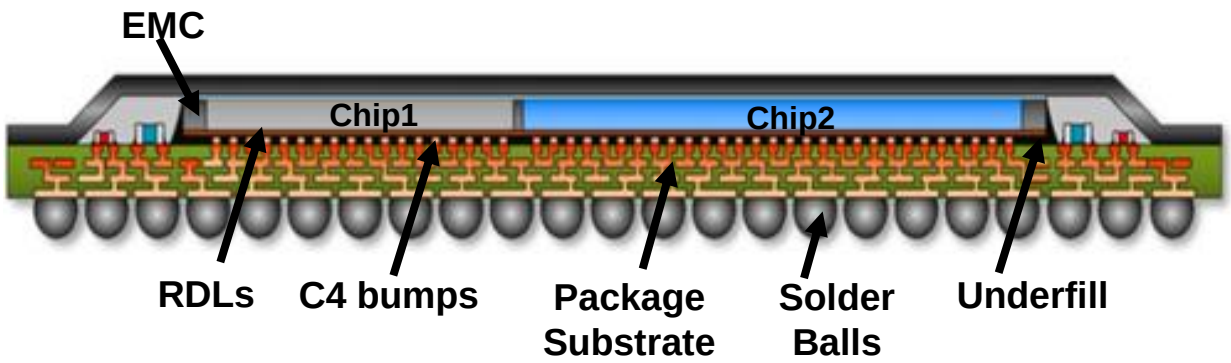
Chip-First

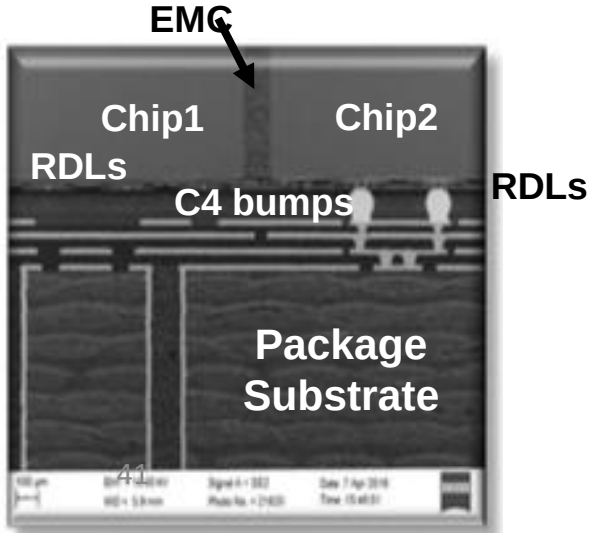
CoWoS



ASE's FOCoS



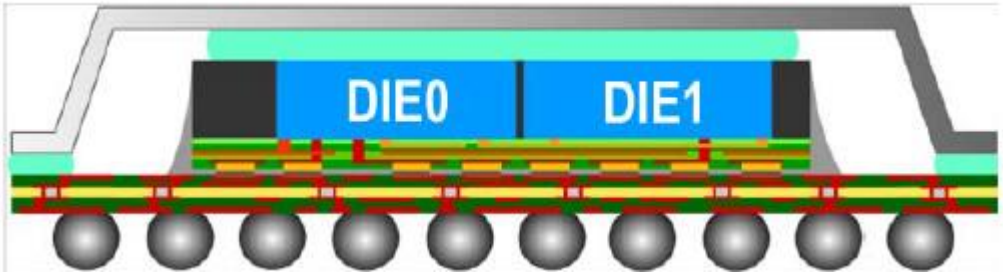


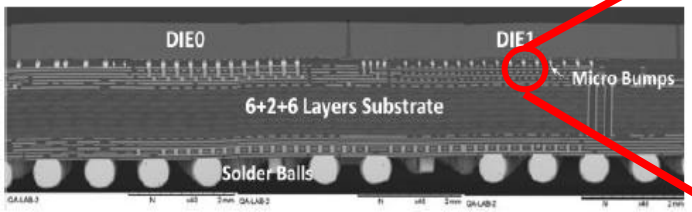


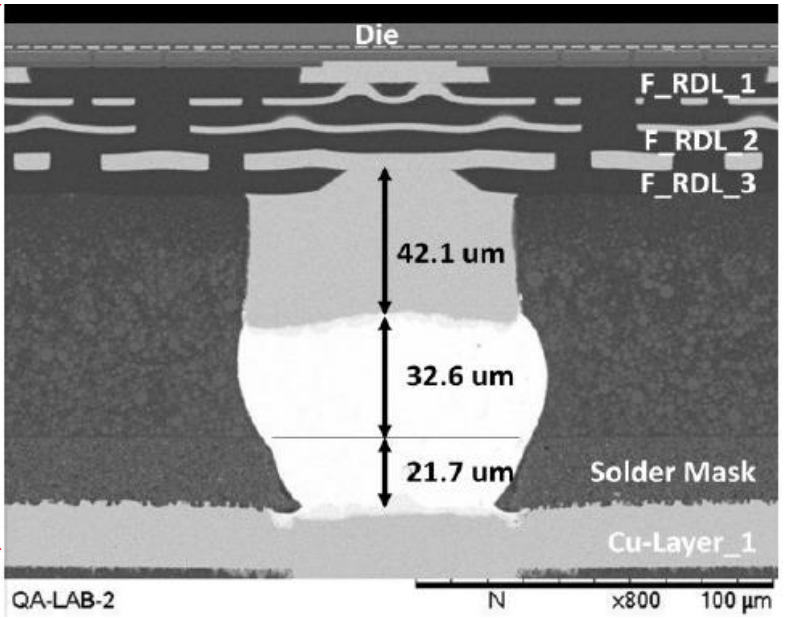
A Novel System in Package with Fan-out WLP for high speed SERDES application

Nan-Cheng Chen, Tung-Hsien Hsieh, Jimmy Jinn, Po-Hao Chang, Fandy Huang, JW Xiao, Alan Chou, Benson Lin
Mediatek Inc Hsin-Chu City, Taiwan

Chip-First

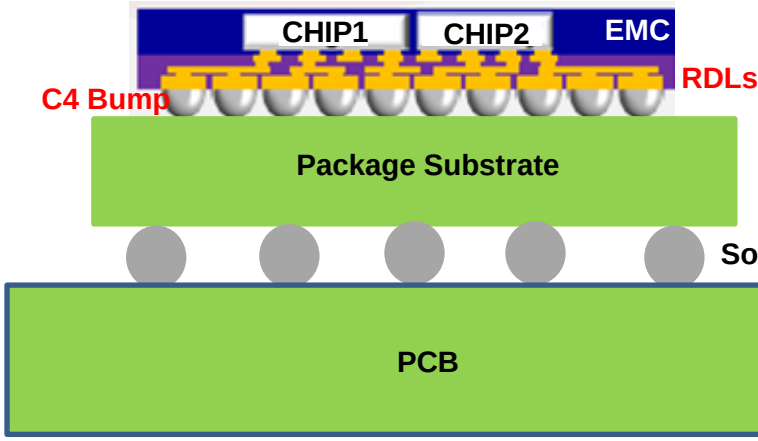




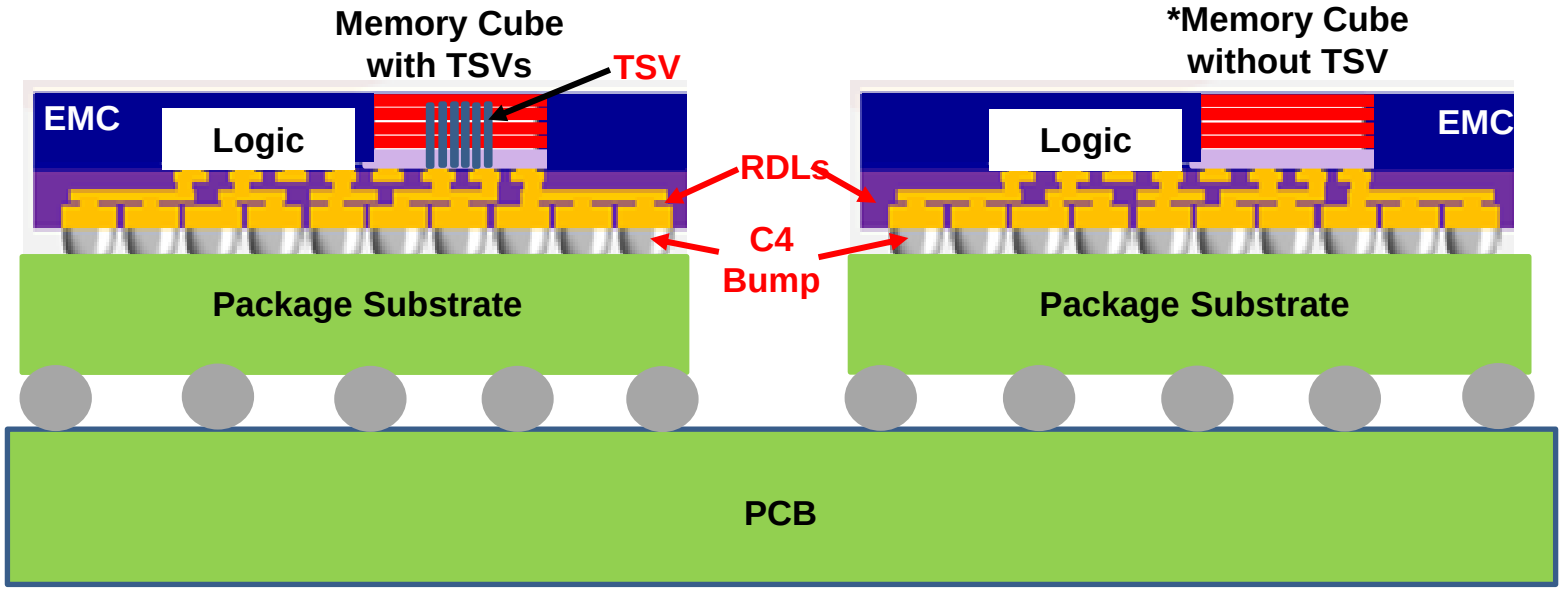


TSMC's InFO_oS and InFO_MS for Heterogeneous Integrations

InFO Chip-First



InFO_oS (Integrated Fan-Out on Substrate)



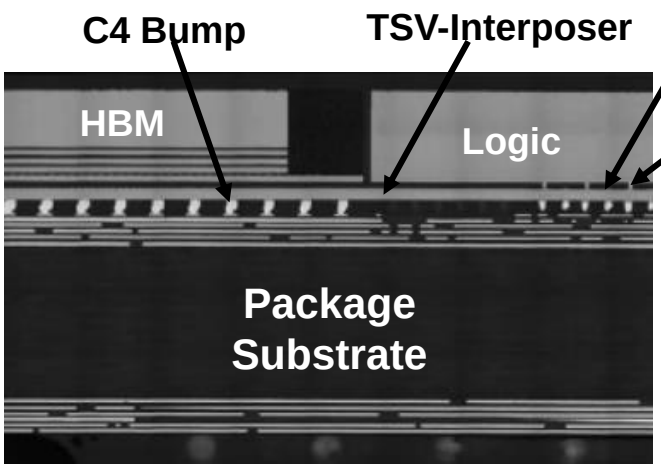
InFO_MS (Integrated Fan-Out with Memory on Substrate)

Low Cost Si-less RDL Interposer Package for High Performance Computing Applications

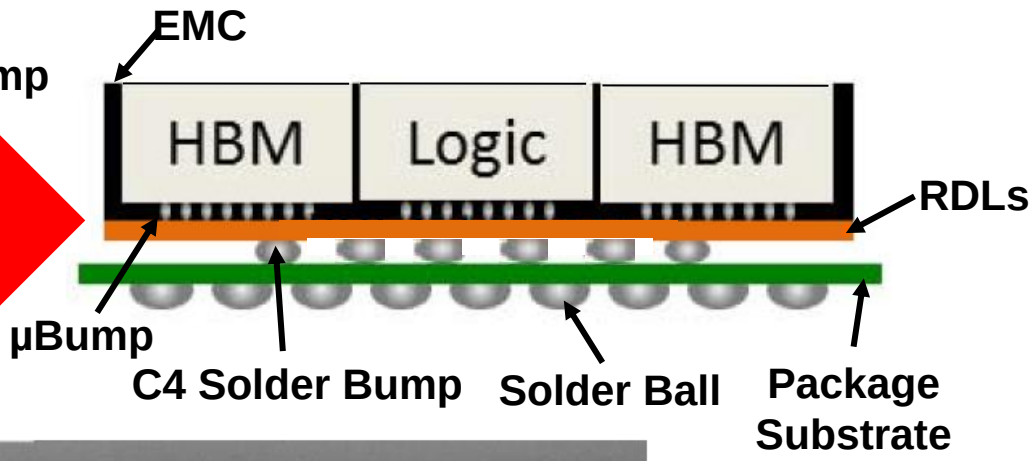
Kyoung-Lim Suk*, Seok Hyun Lee, Jong Youn Kim, Seok Won Lee, Hak Jin Kim, Su Chang Lee,
Pyung Wan Kim, Dae-Woo Kim, and Dan (Kyung Suk) Oh
Package Development Team, Samsung Electronics Co., Ltd.
Gyeonggi-do, Republic of Korea
*klim.suk@samsung.com

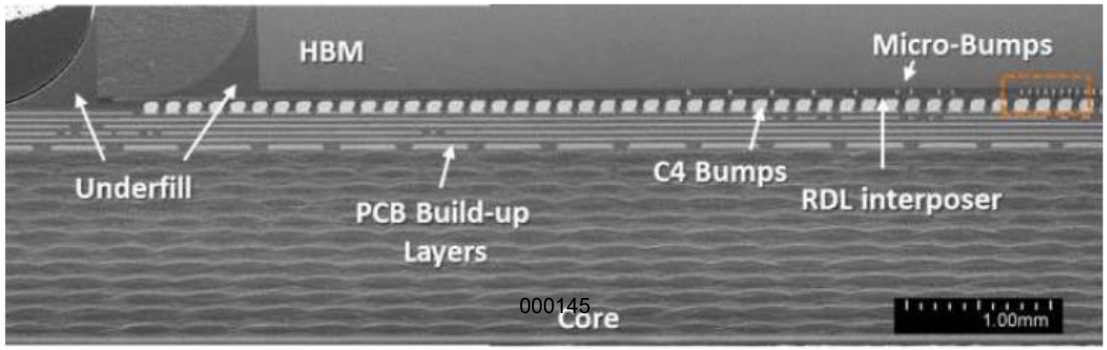
Chip-Last

CoWoS



Si-less RDL-Interposer

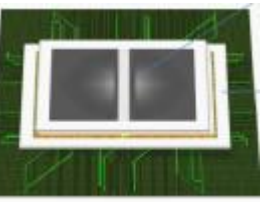




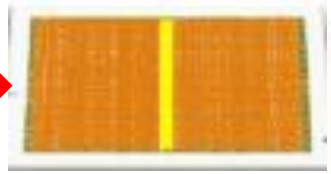
Ultra High Density IO Fan-Out Design Optimization with Signal Integrity and Power Integrity

Keng Tuan Chang, Chih-Yi Huang, Hung-Chun Kuo, Ming-Fong Jhong, Tsun-Lung Hsieh, Mi-Chun Hung, Chen-Chao Wang
Integrated Design, Corporation Design Division, Corporate Research and Development, Advanced Semiconductor Engineering (ASE), Inc.,
No. 26, Chin 3rd Road Nantze Export Processing Kaohsiung 811, Taiwan
Email: gordon_chang@aseglobal.com

Chip-Last

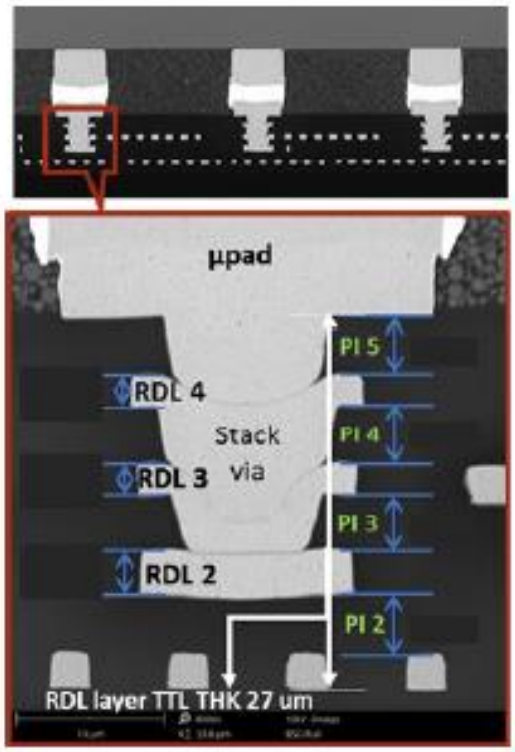


CoWoS

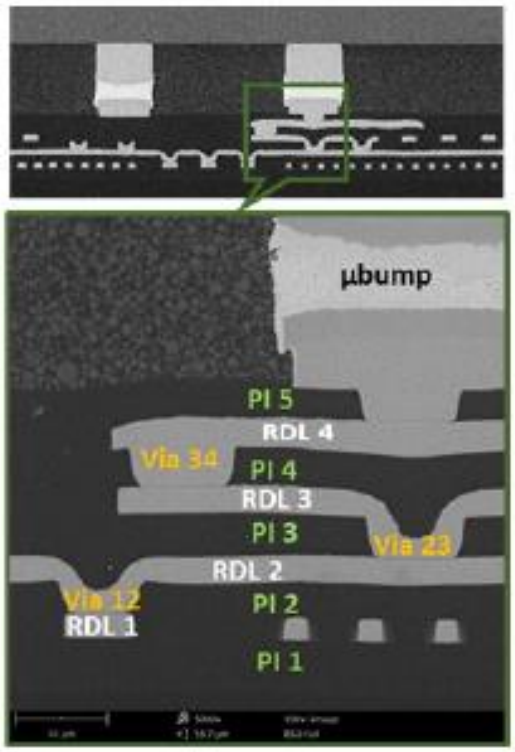


FOCoS

Stacked Vias



Non-stacked Vias



Cross sections of FOCoS

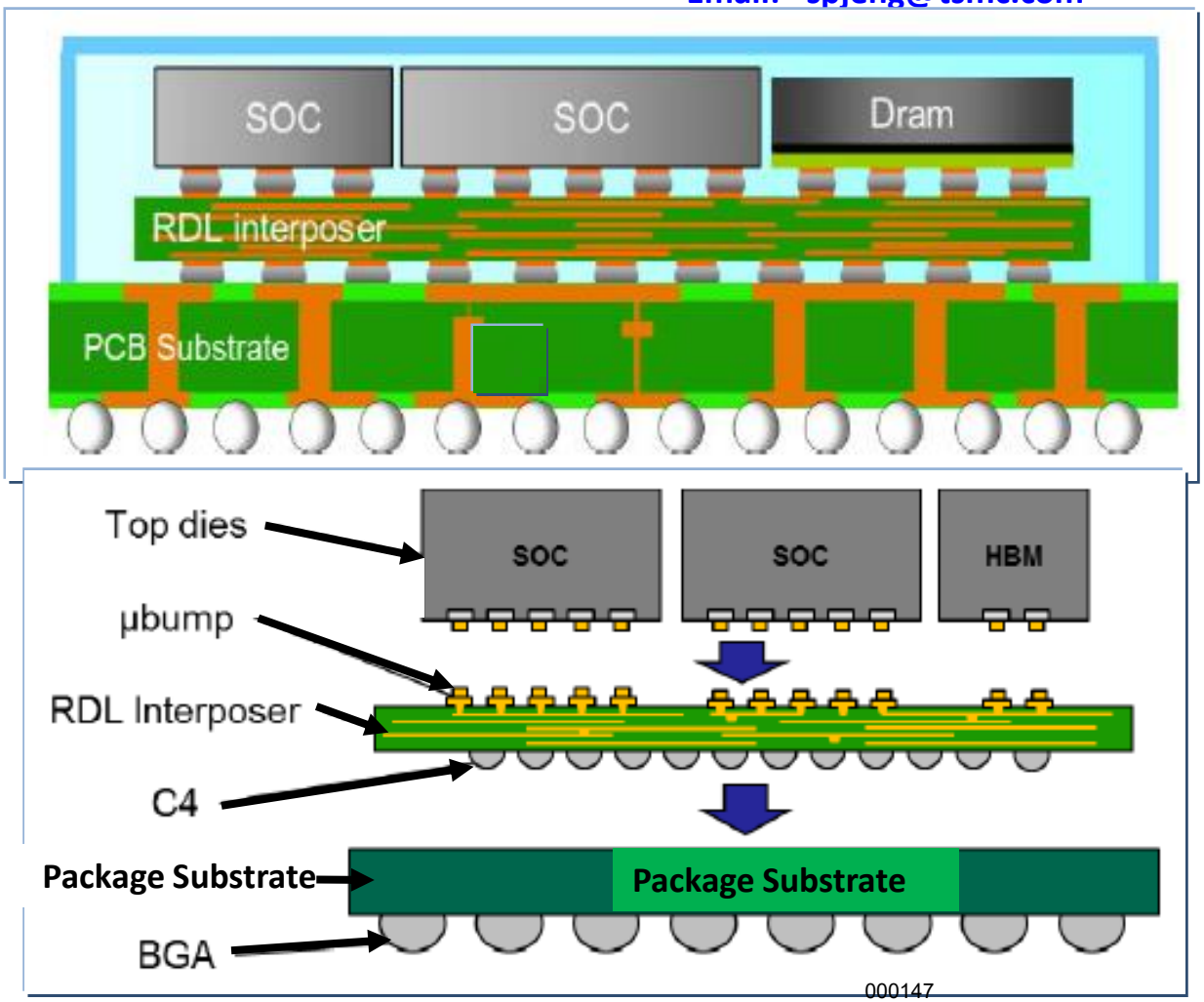
Heterogeneous Integration with Multilayer RDL Interposer

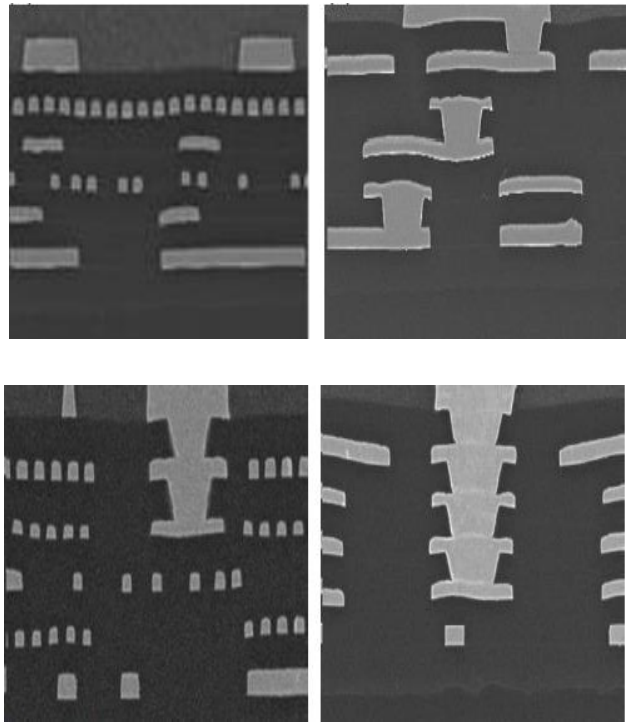
Yi-Hang Lin, M.C.Yew, M.S. Liu ,S.M. Chen, T.M. Lai, P.N. Kavle, C.H. Lin, T.J. Fang, C.S. Chen, C.T. Yu, K.C. Lee, C.K. Hsu, P.Y. Lin, F.C Hsu and Shin-Puu Jeng*

TSMC, No.6, Creation Rd. II, Hsinchu Science Park, Hsinchu, Taiwan (R.O.C.) 30077

Email: *spjeng@tsmc.com

Chip-Last

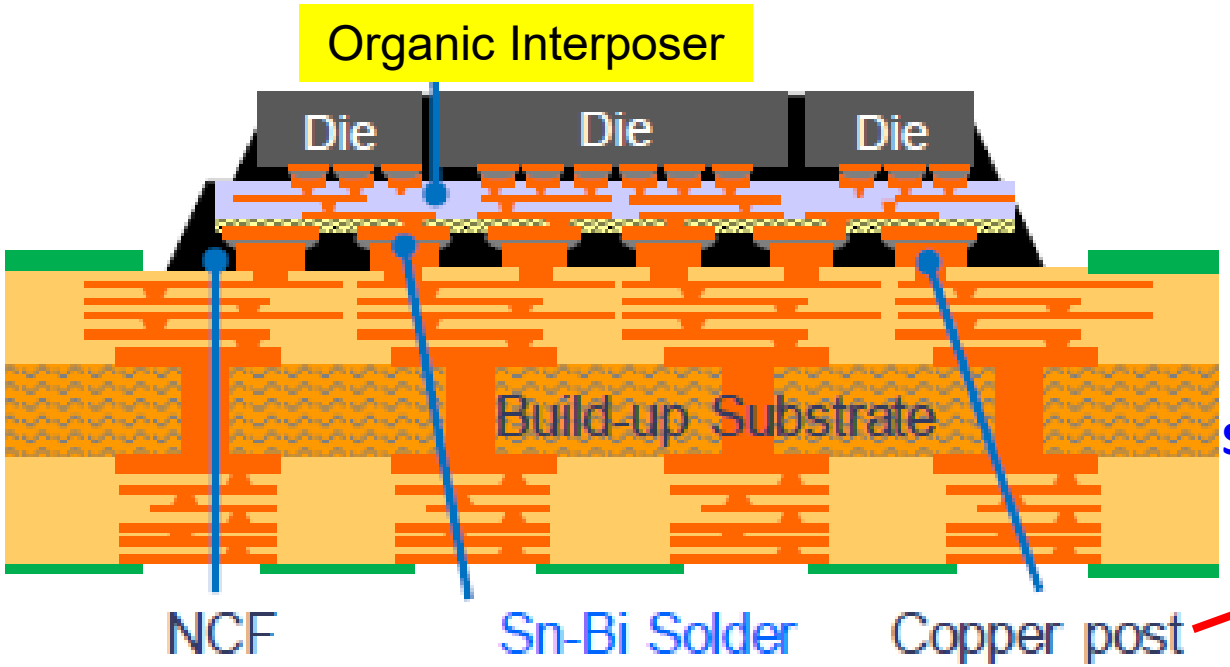


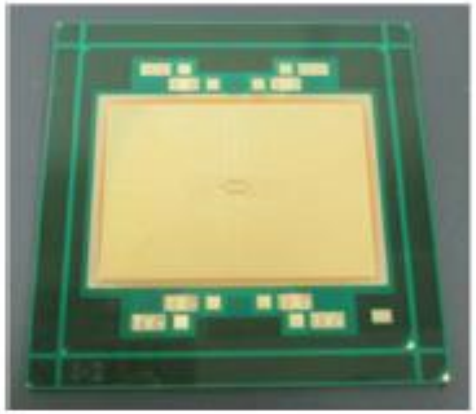


Electro-migration evaluation between organic interposer and build-up substrate on 2.3D organic package

Kei Murayama, Shota Miki, Hiromi Sugahara, Kiyoshi Oi,
Process Development Dept. R & D Div.
Shinko Electric Industries Co., LTD.
Nagano-shi, Japan
kei_murayama@shino.co.jp

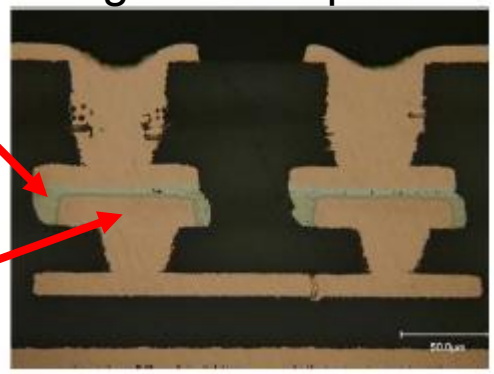
Chip-Last





Organic Interposer

SnBi

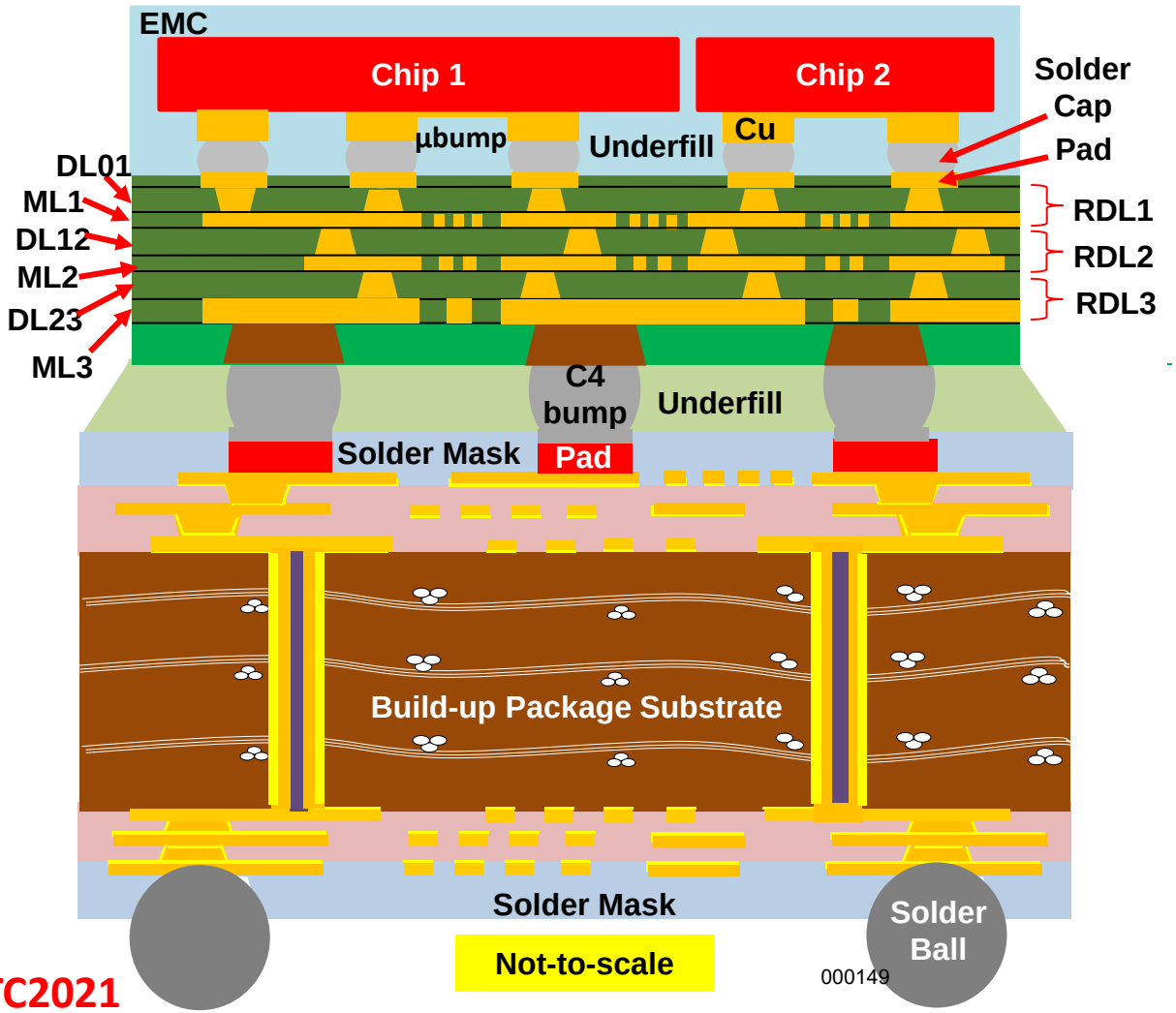


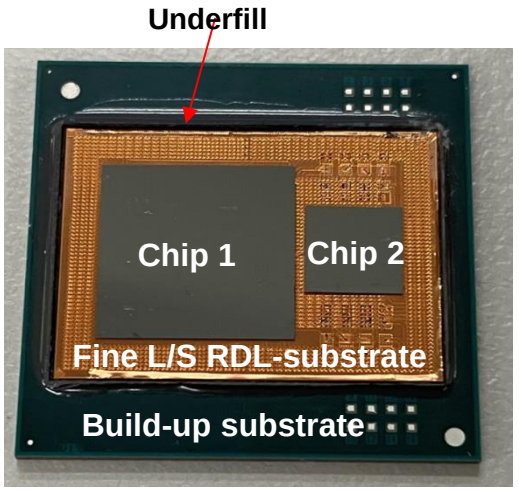
Build-up Substrate

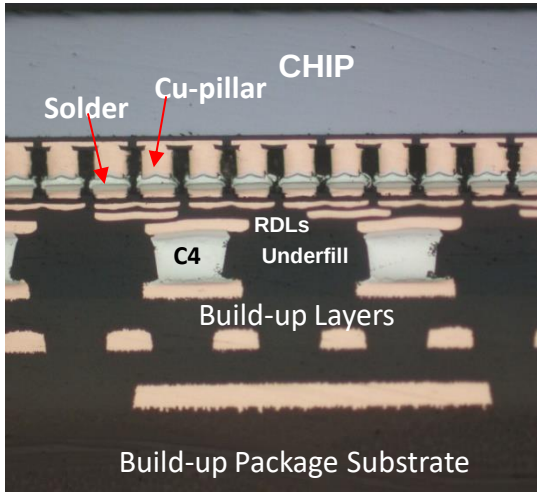
Fan-Out (RDL-First) Panel-Level Hybrid Substrate for Heterogeneous Integration

John H Lau, Gary Chang-Fu Chen, Jones Yu-Cheng Huang, Ricky Tsun-Sheng Chou, Channing Cheng-Lin Yang, Hsing-Ning Liu, and Tzvy-Jang Tseng
Unimicron Technology Corporation,
Taoyuan City, Taiwan
John_Lau@unimicron.com

Chip-Last







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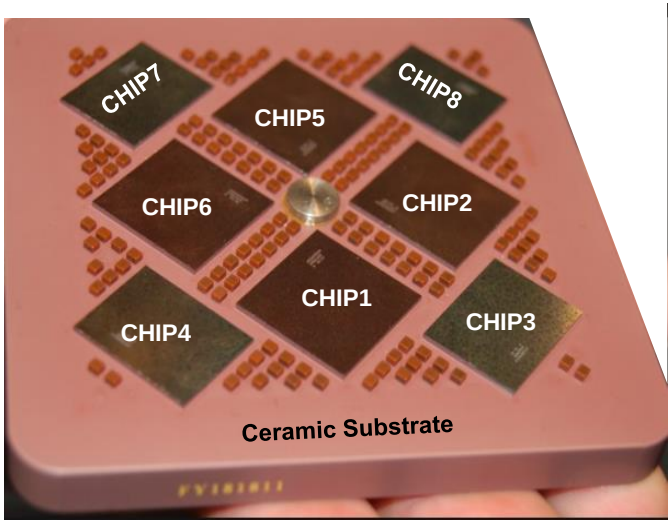
Classification of Heterogeneous Integrations

- Heterogeneous Integrations on Organic Substrates
- Heterogeneous Integrations of Silicon Substrates (TSV Interposers)
- Heterogeneous Integrations on TSV-less Interposer (Bridges)
- Heterogeneous Integrations on Fan-Out RDL-Substrates
- Heterogeneous Integrations on Ceramic Substrates

MCM (Multichip Module) on Ceramic Substrate



MCM on Ceramic Substrate

IBM 9121 TCM
(Thermal Conduction Module)

- TCM weighs 2.2Kg
- Contains up to 121 chips about 8-10mm square
- Each chip has a spring-loaded Cu piston to remove heat
- Up to 10W dissipation per chip
- Up to 600W dissipation per TCM
  Ceramic substrate has:
  - 63 layers
  - Up to 400m of wirings
  - Up to 2 million vias
- 5Kg air-cooled heatsink to remove heat from TCM

Trends and Roadmaps

TRENDS

- In order to promote the heterogeneous integrations, standards are necessary! The Defense Advanced Research Projects Agency (DARPA) program called Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS) is heading into the right direction:- to make modular computers out of chiplets. Intel's AIB (advanced interface bus).

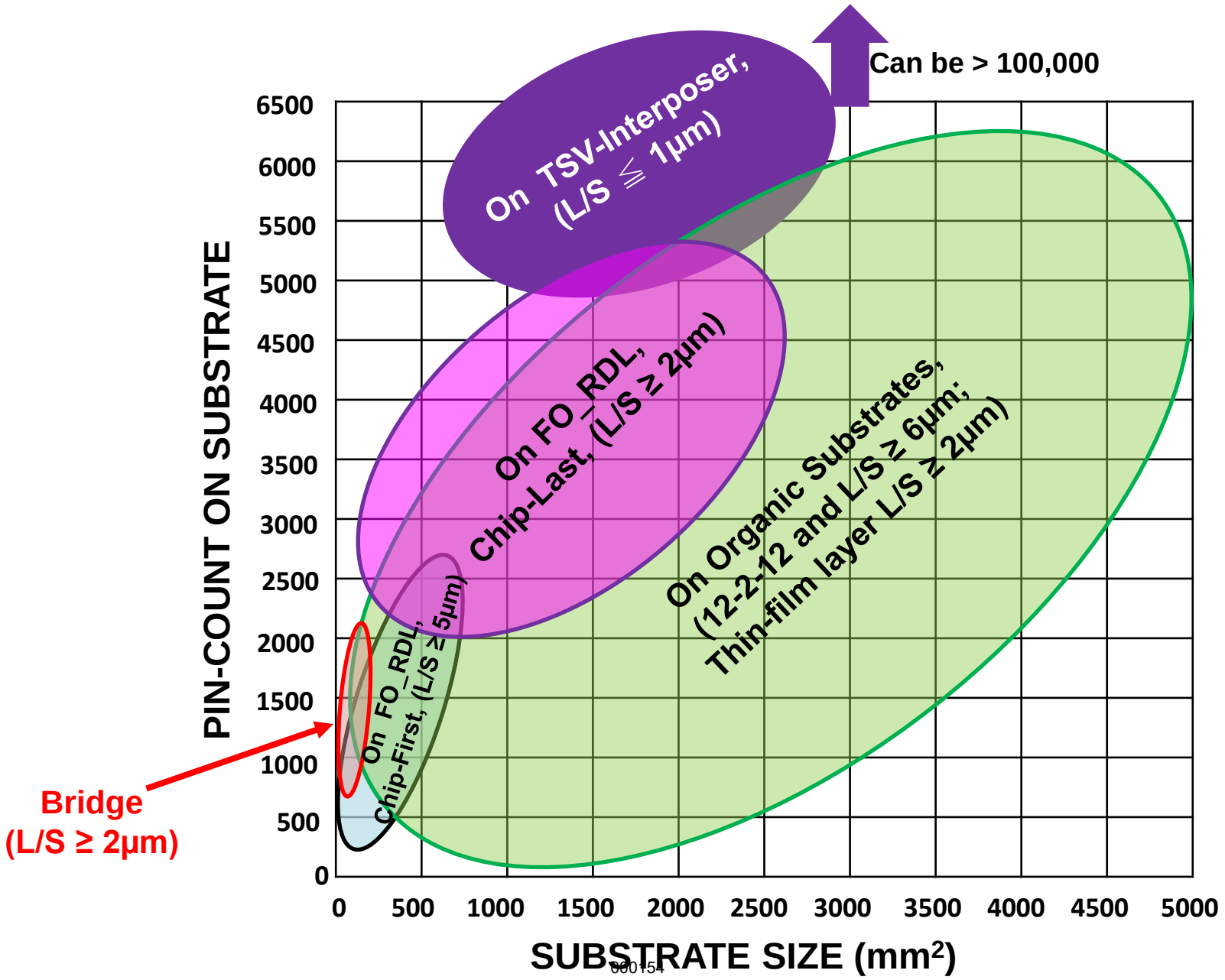
- EDA (electronic design automation) tools for automating system partitioning and design are desperately needed for complex heterogeneous integration systems.

- 75% of the heterogeneous integrations will be on organic substrates. (Actually most are SiPs). The assembly processes are mainly SMT and flip chip.

- 25% of the heterogeneous integrations will be on other substrates such as silicon (TSV-interposers), silicon (TSV-less interposers), fan-out RDLs, and ceramic.

- How to select different types of heterogeneous integrations? It depends on the applications. The most important indicator (selection criterion) is the metal line width and spacing of the RDLs for the substrates being used for the heterogeneous integrations.

Heterogeneous Integration Substrate Roadmaps



Thank You Very Much for Your Attention!