Heterogeneous Integration: Opportunities and Challenges

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President and Founder

- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY

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What's Driving Adoption Heterogeneous Integration?

- **As the industry moves to the next silicon nodes (≤7nm, etc.) on package integration is needed to achieve the economic advantages that were previously met with silicon scaling**
  - Design some components in the most advanced semiconductor node
  - Use this chip in combination with others in a package that provides the desired function in a more cost effective manner
  - Die functions that can be fabricated in older nodes and lower cost can be combined in a single package
  - IP reuse reduces cost
- **Heterogeneous integration provides a solution that can be in many formats!**
  - Silicon interposers (2.5D), TSMC CoWoS process
  - Alternatives such as embedded bridge including Intel's EMIB
  - Fan-out on Substrate
  - "chiplets" where substrate interconnect provides in package communication between different functions
  - 3D structures with TSVs or direct bond interconnect

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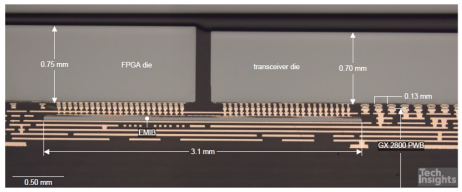
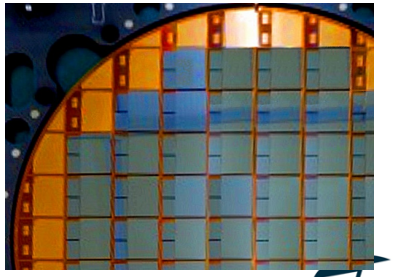
Many Different HI Options for HPC

- **Silicon Interposers**
  - Xilinx (many FPGA products) started in 2012, AMD shipped in 2015 (GPU + HBM), NVIDIA (GPU + HBM), Google, Baidu, Broadcom, many others in production!
- **Fan Out on Substrate**
  - Chip first (in production since 2016 at ASE) and chip last solutions (many designs)
  - In production for network switch at TSMC with InFO-R (since 2018)
  - Amkor Substrate-SWIFT®, SPIL Fan-Out Embedded Bridge, TFME
- **Embedded bridge Intel, IBM, SPIL, TSMC, and others**
  - Intel's EMIB silicon bridge in an laminate substrate, embedded by substrate supplier (Intel Stratix 10 for AI accelerator)
  - Amkor, ASE, IBM, SPIL, TSMC offerings
- **RDL Interposers InFO-SoIS (System on Integrated Substrate), Samsung R-Cube™, PTI, Unimicron, and others**
  - Extend to finer feature (2µm L/S) switch to fab-like process

Source: NVIDIA.



Source: Intel by TechInsights.



Source: ASE.

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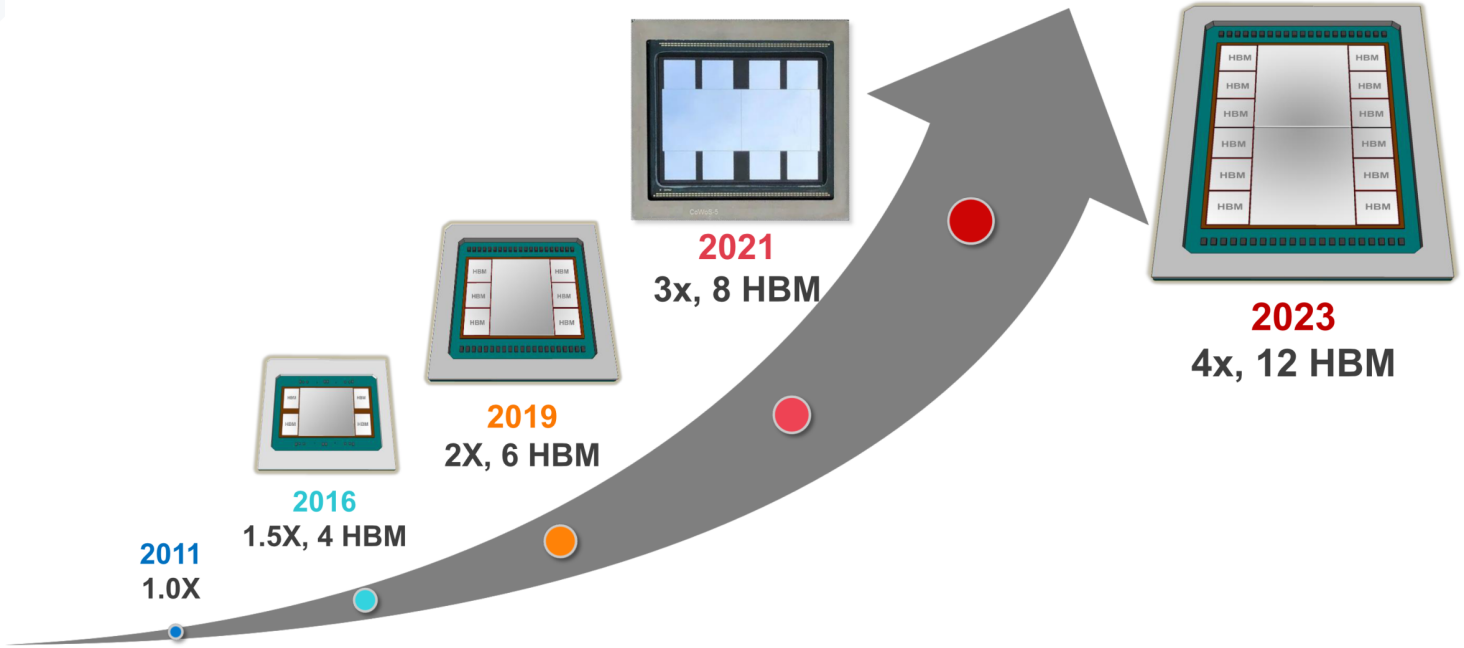
TSMC's CoWoS-S for High-Performance Computing



Source: TSMC.

- **Increasing size of interposer and multiple HBMs drives the size of the laminate substrate that forms the package**
  - Body sizes of 65 mm x 65 mm, 75 mm x 75 mm, increasing to 100mm x 100mm body size
  - Applications include AI accelerators, FPGAs, network switch, GPUs

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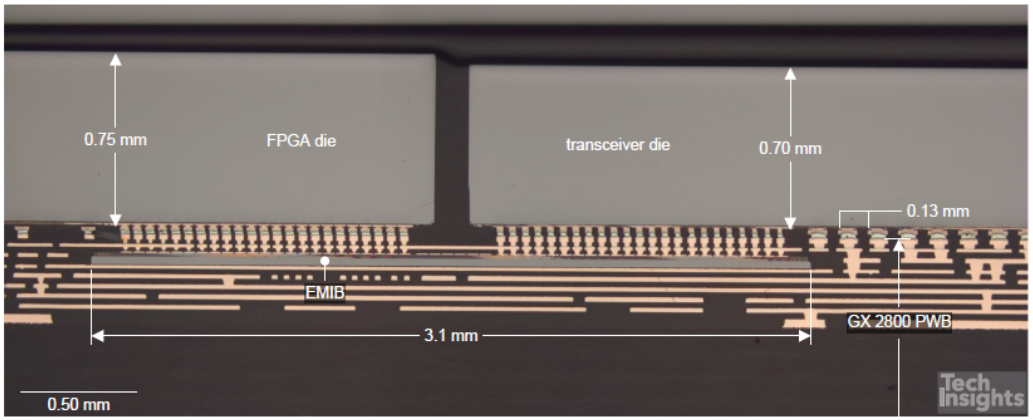
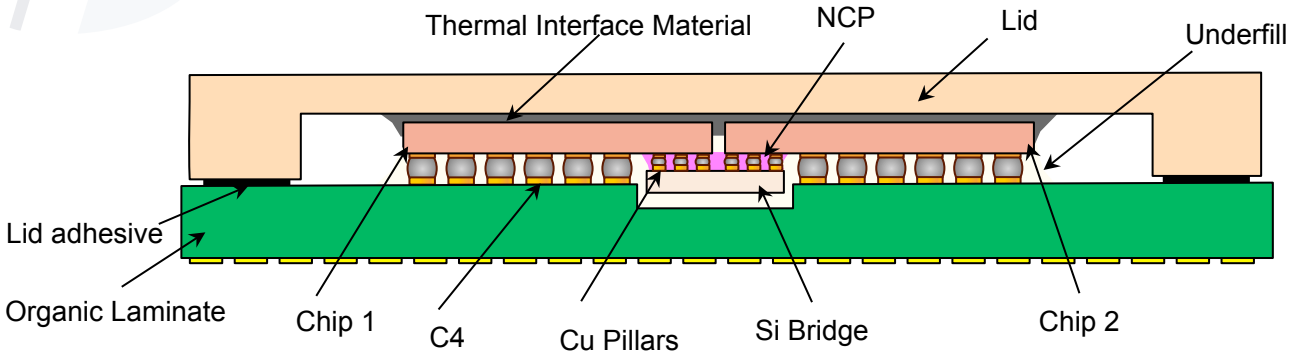
Intel's EMIB Uses Si Bridge for Chip-to-Chip Communication

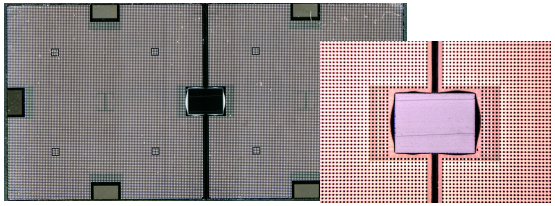


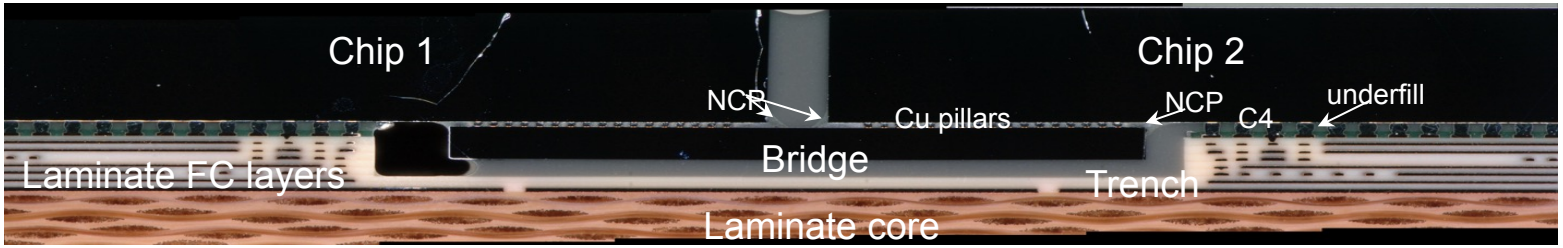
Source: TechInsights.

- **Embedded Multi-die Interconnect Bridge (EMIB)**
  - A small silicon bridge chip is embedded into the package (no TSVs)
- **EMIB allows the die I/O or bumps to be placed as close as possible to the edge of the die because fewer I/O or bumps are required**
  - Micro bumps on chips, communication between chips through interposer
  - Provides a high-density localized interconnect between the FPGA and the transceiver die

IBM Direct Bonded Heterogeneous Integration (DBHi) Si Bridge







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Source: IBM.

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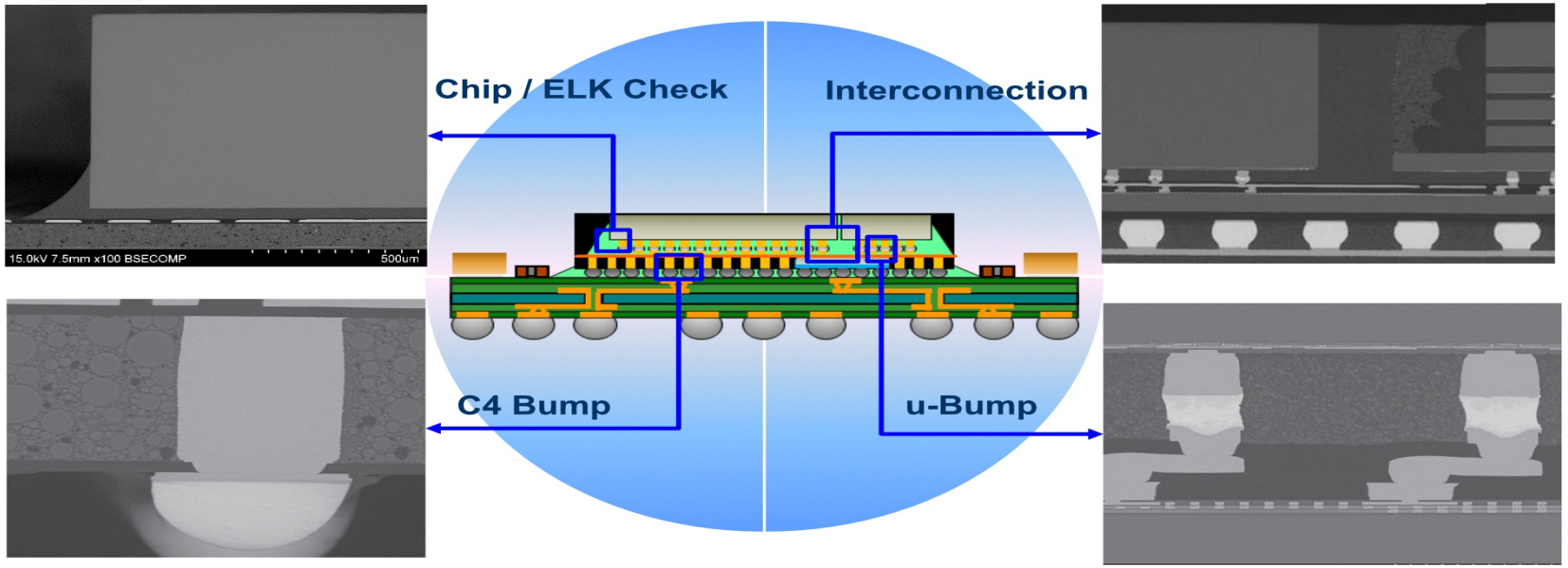
SPIL FO-EB Technology



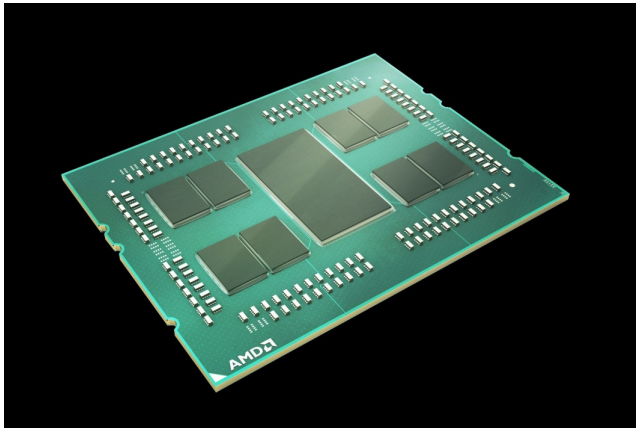
Source: SPIL.

- **SPIL has qualified a fan-out embedded bridge (FO-EB) RDL test vehicle**
  - Microbumps used to connect each die to RDL
  - C4 bumps connect to next level
- **FO-EB targeted for CPU + HBM, GPU, and network router**

Chiplets: Key Enabler for Next 10-20 Years

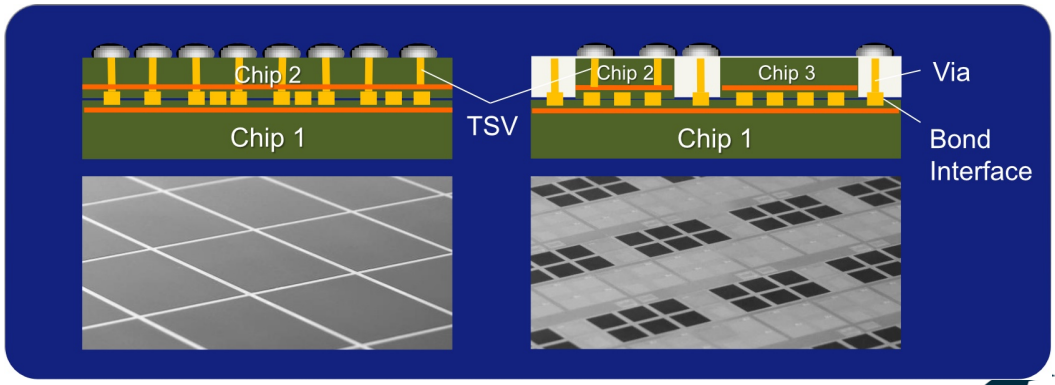
- **Chiplet demand driven by:**
  - Need for a more cost-effective solution given the economic challenging of continued silicon scaling
  - Desire to reuse IP
  - Improved electrical performance
  - Better power efficiency
  - Faster time-to-market

AMD's chiplet design on organic substrate



Source: Wired.com.

TSMC's SoIC



Source: TSMC.

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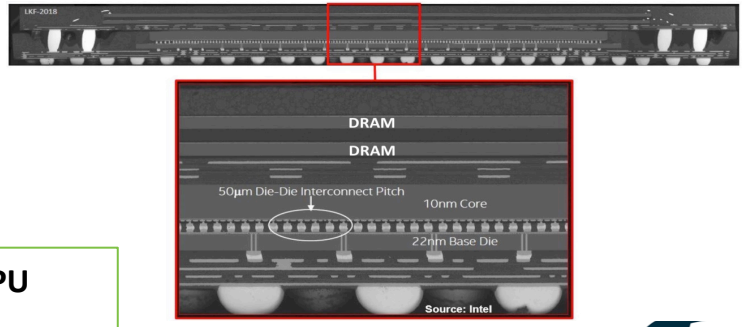
Intel Foveros Technology

- **Intel's Foveros technology die are stacked on an active interposer**
  - Active interposer (base chip) can include power management features, voltage regulators, DC/DC converters
- **Benefits include**
  - Reduced voltage drop
  - Power efficiency
  - More immediate power delivery to the CPU cores
  - Elimination of passives on substrate
  - System-wide communication across multiple chiplets/dice vs. the limited die-to-die communication capability enabled by passive Si interposers
- **Used in the Samsung Galaxy Note S (Mobile PC)**
  - Longer lasting battery
  - No fan
  - Very thin package, allows thin product

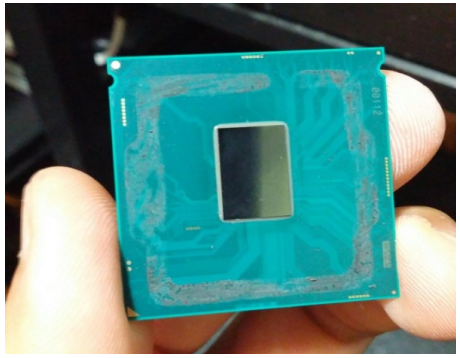


Source: Intel.

Intel's Lakefield CPU
- 10nm CPU
- 22nm Active Si Interposer

HPC Substrate Trends

- **HPC options use laminate substrates**
  - Silicon interposers
  - Fan-out on Substrate
  - Embedded die
- **Increased I/O counts driving up layer counts**
  - >20 layers
- **Larger die sizes and multiple die mounted on substrates driving need for larger substrates**
  - Up to 100 mm x 100 mm
- **More I/O increases wiring density requirements**
  - Need to support tight bump pitch of 40-55 µm, including bump pitch on high bandwidth memory (HBM)
  - Need ~2µm L/S and small via pad or via with no pad
- **Need improved signal integrity and power efficiency**
  - Requires reduced line lengths for wiring



Source: Anandtech.com

Source: TechSearch International, MediaTek.

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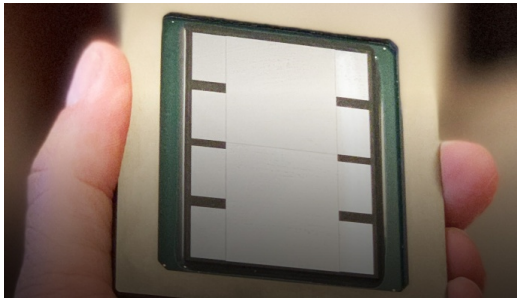
Build-up Substrate: Increased Demand

- **Unit growth volumes for build-up substrates for FC-BGA show <3% CAGR 2020 to 2024**
  - Datacenter and cloud computing expansion
  - AI accelerator expansion
  - Laptops continue to show growth
- **Big problem is increase in size and layer count**
  - Increased layer counts (18-20 build-up layers)
  - Larger body sizes (100 mm x 100 mm)
- **Networking switch products, largest projected body sizes**
  - Increasing in size 77.5mm x 77.5mm, 85mm x 85mm, 100mm x 100mm body size
  - Increased build-up layers

Source: Datacenterknowledge.com.



Source: TSMC.

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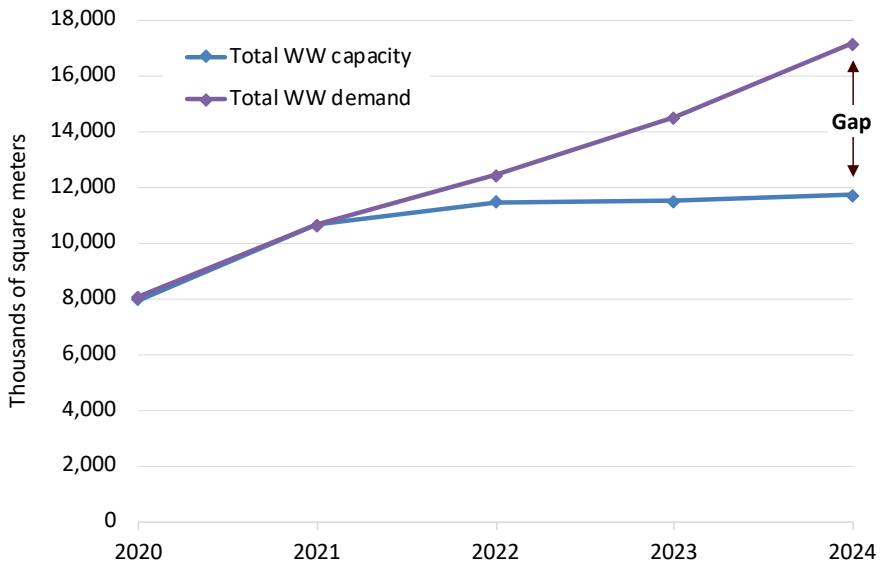
Worldwide Substrate Supply vs. Demand for Flip Chip BGA

- **Unit volume growth is not the problem**
- **The gap will continue to become wider because of the increase in body size and layer count**
- **Industry must find ways to decrease the gap**



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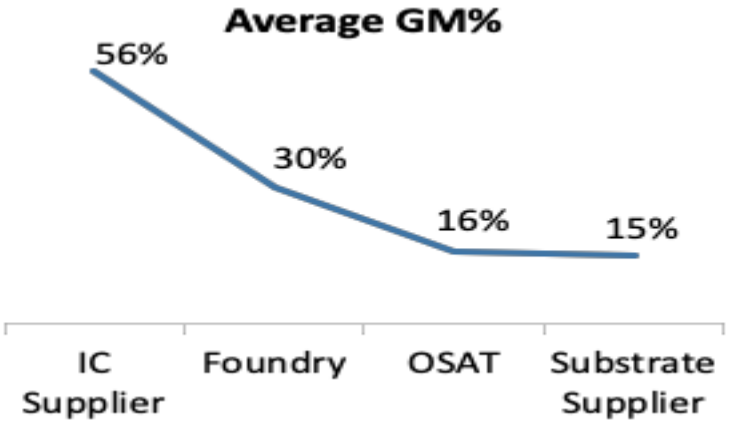
Substrate Capacity Constraint

- **Very little FC-BGA capacity is available**
  - In some cases, available capacity uses different material sets from the commonly used Ajinomoto build-up materials (or Sekisui material)
  - Qualification process for new suppliers and materials is long and expensive (can we make this shorter?)
  - Some laminate substrate equipment has long lead times of up to a year or more
- **Prices for IC package substrates are increasing, lead times stretched out**
- **Substrate suppliers are reluctant to increase capacity for fear of over capacity**
  - New production line with fab-like equipment for advanced substrates (~5µm L/S) is expensive (each line is ~$300 million or more)
  - Substrate makers have relatively low gross margin



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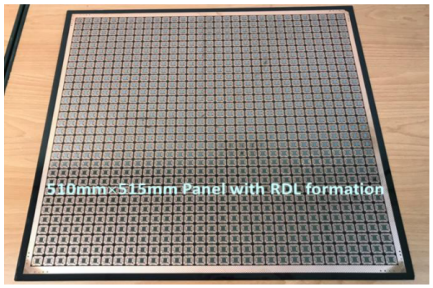
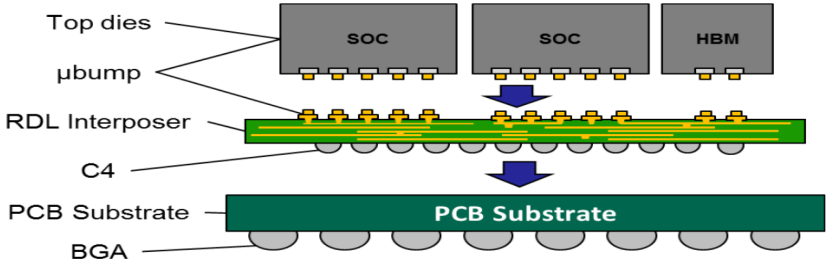
Alternatives to Reduce Build-up Layer Count

- **RDL interposer can reduce the number of build-up layers**
  - RDL has fine features of 2µm L/S that can be used for routing
  - With higher density routing in the RDL, build-up substrate can have fewer layers and higher yield
- **RDL interposer activities**
  - Amkor Technology
  - Deca
  - PTI
  - Samsung
  - TSMC
  - Unimicron

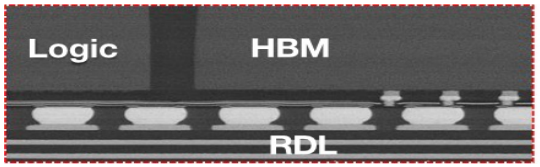


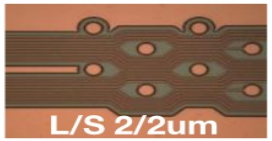
Source: Unimicron.



TSMC's InFO System on Integrated Substrate (SoIS)

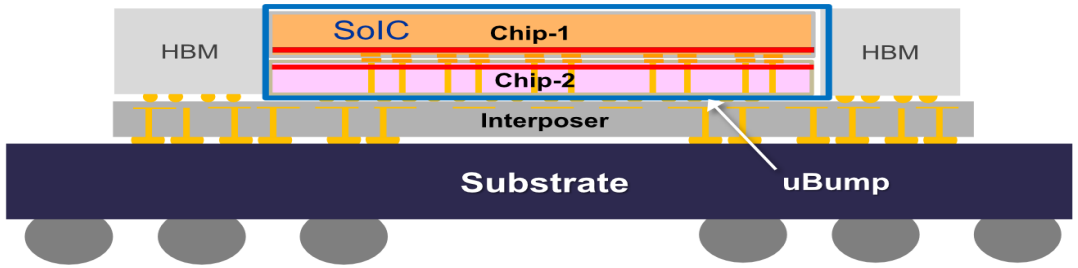
Source: TSMC.





Source: Samsung.

TSMC's SoIC on Si Interposer + HBM



Source: TSMC.

- **Logic + HBM on Si interposer can include 3D logic such as SoIC**
  - With SoIC potential for few build-up layers in the laminate substrate
- **With SoIC there is virtually no distance between integrated chips, and a very small bond-pad pitch of 9 µm provides good scalability**
  - Potential for finer bond pitch interconnect
- **Bumpless bonding process provides improvements in performance, power, resistance, and capacitance**
  - Inductance and thermal resistance are lower
  - Improved power efficiency

Summary

- **A new era in heterogeneous integration including 3D and chiplets is emerging**
  - Provide advantages to optimize system power, performance, area, and cost
  - It is possible to continue scaling, but cost advantages are achieved with advanced packaging innovations
- **Many potential heterogeneous solutions (partition the die)**
  - Split die to reduce die size and improve yield at wafer level
  - Heterogeneous integration (interposers, FO-on-substrate or other multi-die solutions such as “chiplets,” and some variation of 3D stacking)
  - Introduction of 3D chip stacking with bumpless bonding
- **Heterogeneous integration challenges: Need a robust ecosystem**
  - Design of new architectures requires EDA tools and modeling capability, co-design
  - Adequate substrate capacity
  - Thermal solutions, especially for 3D
  - Test strategies

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Thank you!

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