Chip Package Bumping on Wafer-level for RDL First Fan-out Wafers

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Self-introduction

Dr. Anshuma Pathak is ‘Process Development Manager’ of the Wafer level Packaging unit at PacTech in Nauen, Germany. She received her PhD degree from Institute of Nanoelectronics, TU Munich in an interdisciplinary field of electrical engineering, material science and nanotechnology, focusing on organic electronics in 2015. She has worked as a research assistant at Institute of Semiconductor Technology at TU Braunschweig before starting her PhD. She has been in the field of semiconductor industry for over 10 years and is involved in device fabrications and characterizations over these years.

Overview

- Introduction
- Process flow: Fan-Out wafer fabrication
- RDL design
- Molding Process
- Solder bumping process
- Reflow optimization: Laser scanning reflow
- Handling challenges: mold material; warpage issue, mechanical & thermal stress
- Solder bumps quality check

Introduction

- Fan-out wafer-level packaging (FOWLP) is one of the most attractive advanced packaging trends in microelectronics: it allows an improved form factor with reduced package volume & thickness
- FOWLP also enables better thermal packaging performance with a shorter heat dissipation path
- FOWLP combines multiple chips from heterogeneous processes into a compact package, thereby reducing the footprint.
- KGDs are embedded in an EMC and an RDL establishes the connections within the package without any need of TSVs or a laminate package substrate.
- RDL 1st approach: RDL layers are built-up on a carrier wafer and KGDs are attached to the RDL followed by molding & solder bumping
- Wafer handling challenges appear after molding that leads to warpage of the molded wafer due to CTE mismatch between Si and mold compound
- solder bumping process of RDL 1st FOWLP wafers are evaluated at wafer-level and handling challenges are explained

Process flow

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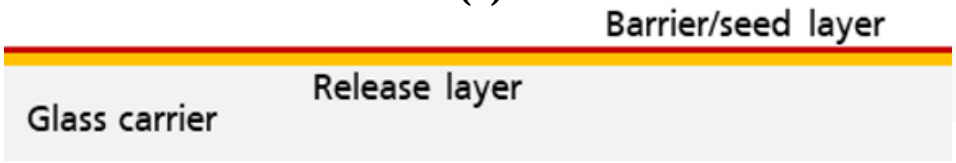

- Application of release layer on temporary glass carrier
- Deposition of barrier/ seed/ protection layer

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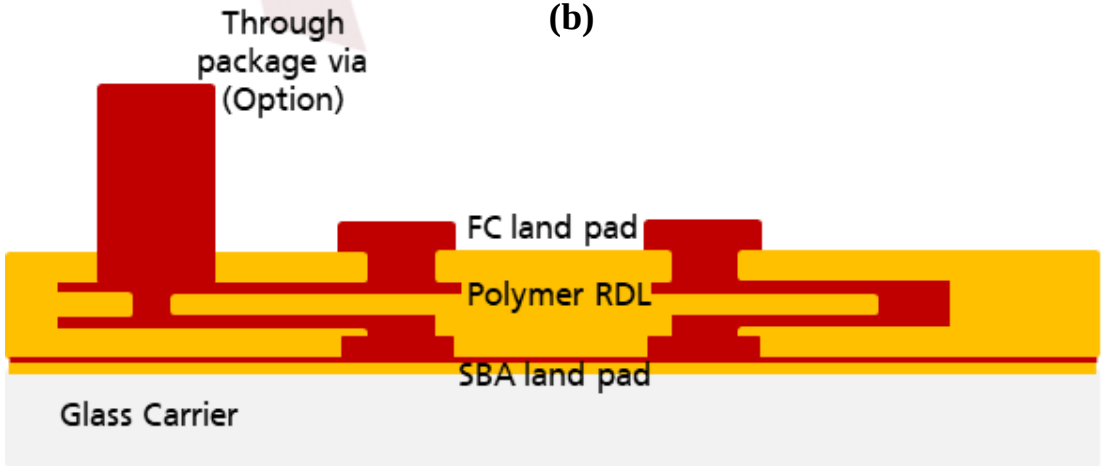

Sequential build-up of a multilayer polymer RDL including:

- Land pads for solder ball attach (SBA)
- Multi-layer copper redistribution layer for fan-out and component to component wiring
- Land pads for flip chip assembly as well as IPD assembly

Through package via (TPV) for top to bottom interconnects

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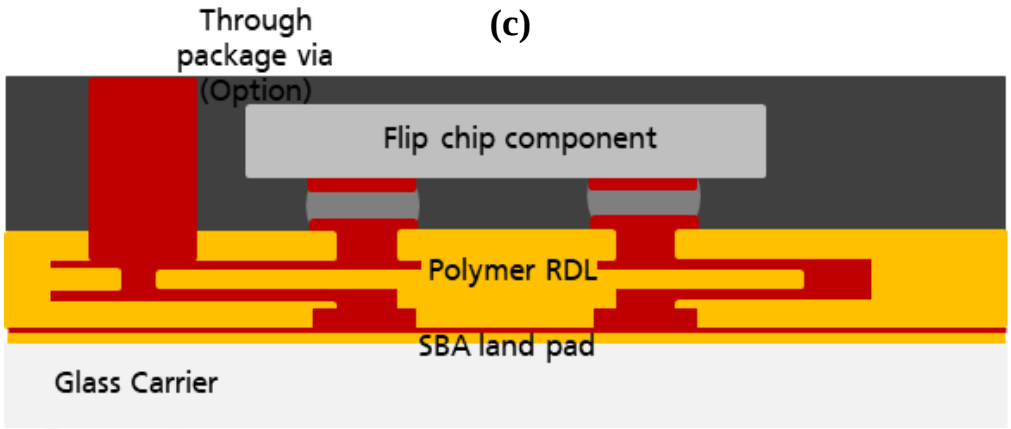
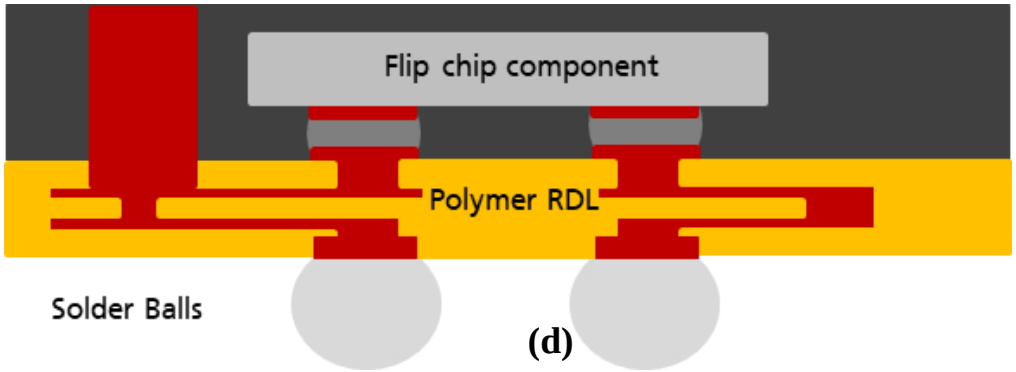


- Die to wafer assembly of flip chip components and mass solder reflow
- Wafer mold by injection molding including mold underfill
- TPV open by modified molding process and/or mechanical back grinding



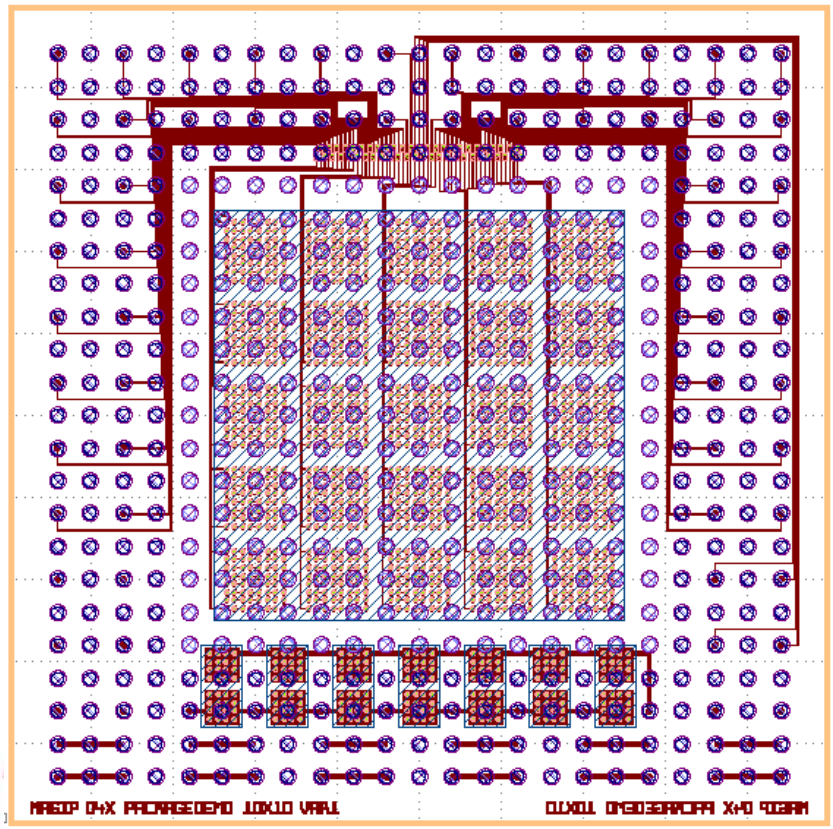
(d)

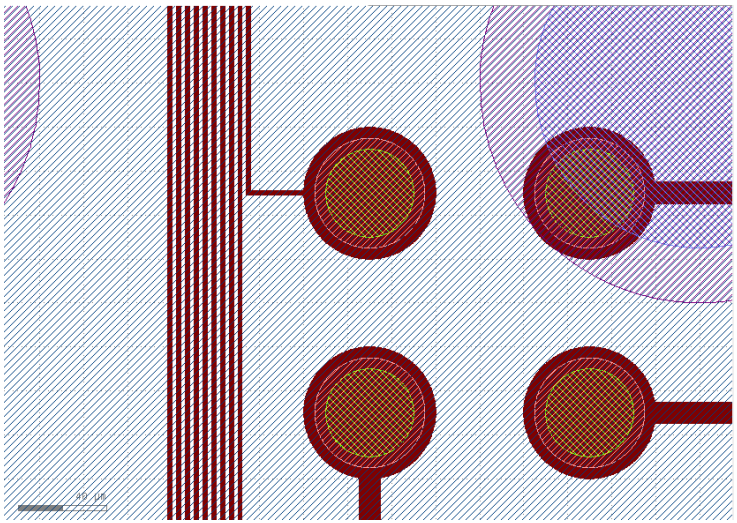
- Laser release of temporary glass carrier and post laser release removal of release layer residues; Wet etch of temporary barrier/ seed/ protection layer
- Cleaning of SBA land pads, application and reflow of solder balls

RDL design

- Generic daisy chain design with dense RDL area, FC µ-pillar, test pads;
- Details of 2µm line/space RDL inside the die area.

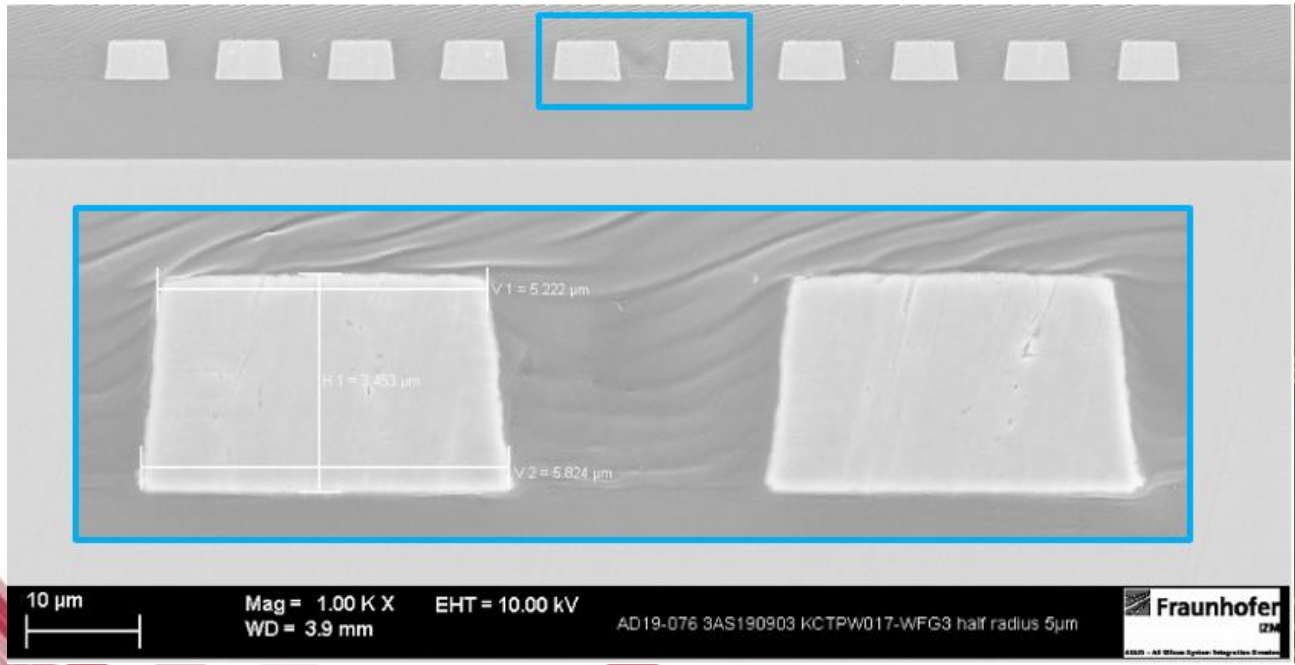
Wafer size: 300mm
Wafer thickness: ~200µm
Warpage: ~1mm

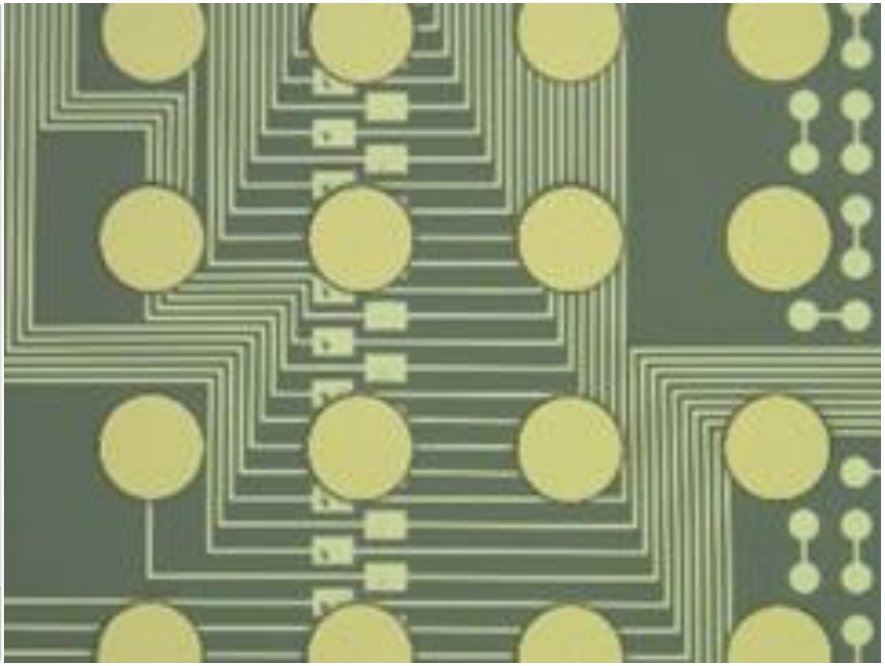




RDL design

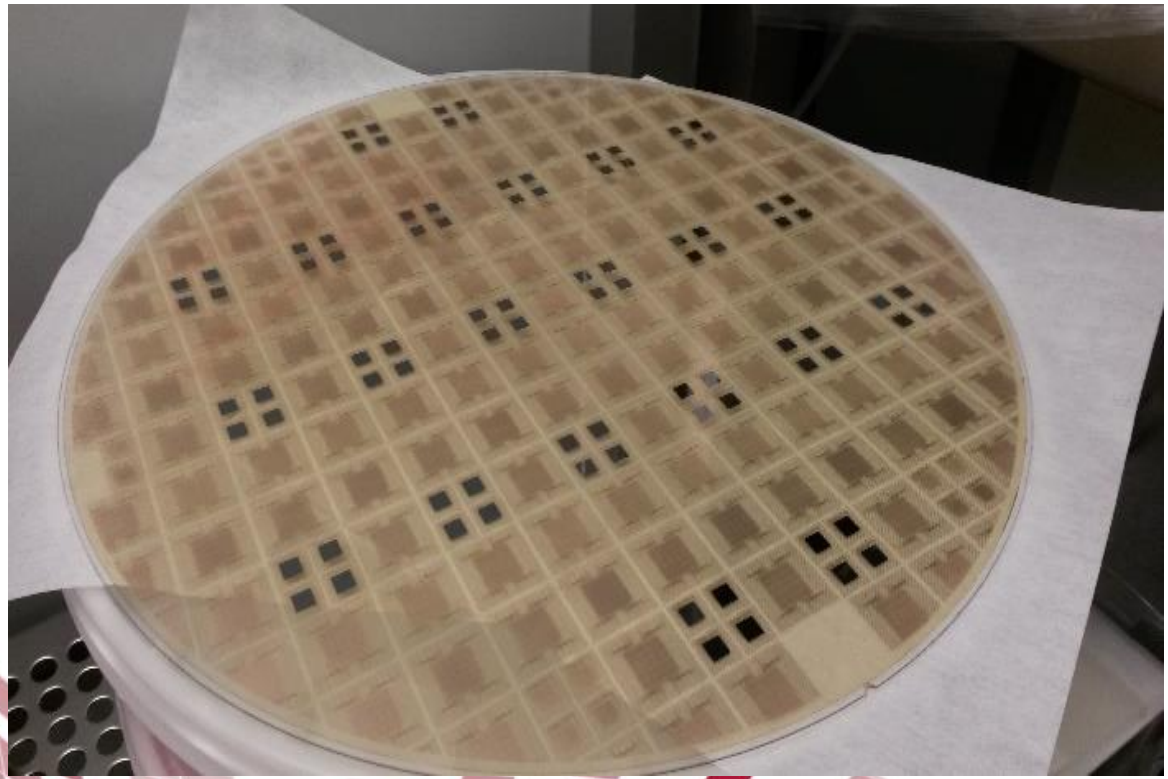
- RDL cross-section through high density copper-RDL, 5µm line/space, 3µm thick;
- Top view of multi-layer RDL showing SBA-land pads, test pads, RDL and FC-land pads.

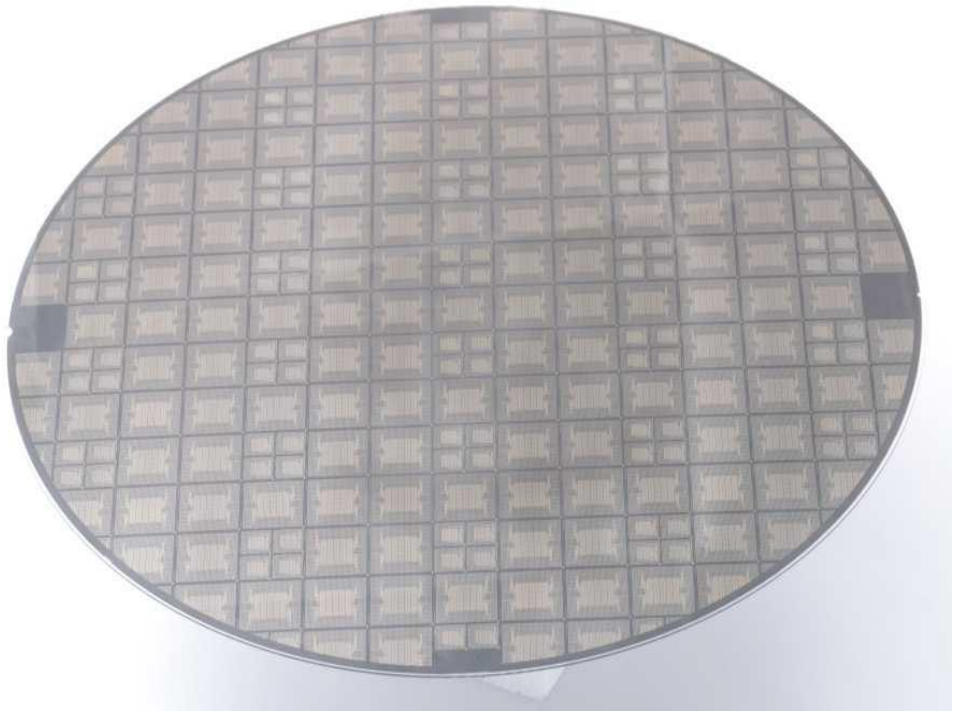




RDL design

- RDL 1st test wafers after DC chips assembly;
- Wafer after molding process

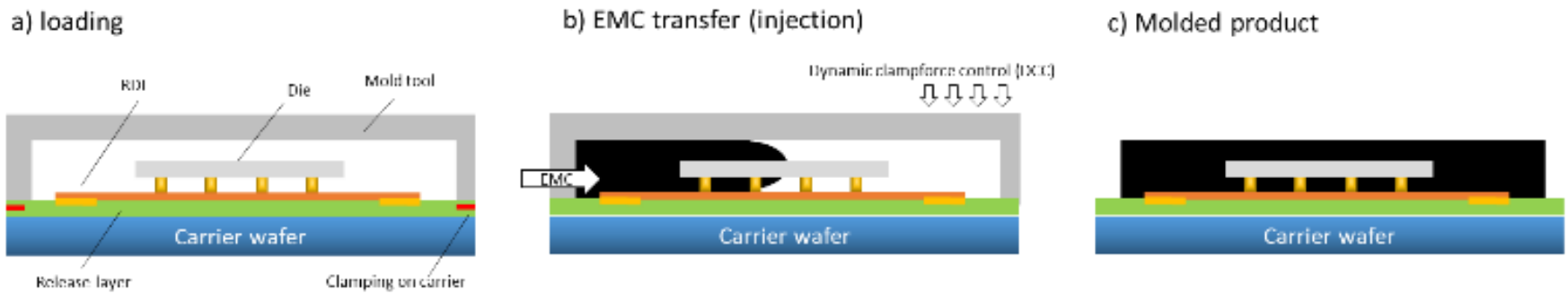




Molding Process

Process flow of the RDL-1st FO-WLP transfer molding process

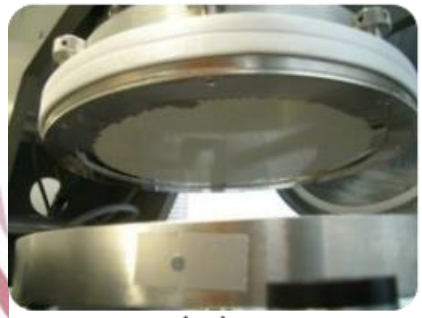
- EMC is transferred inside a cavity after the mold tool is closed; specific advantages in cost reduction for this approach
- Before molding a plasma activation using ArH_2 plasma (300 w) is performed
- 50 µm thick PET foil is fixated to the inner surfaces of the mold to protect it from the injected EMC.
- Pressure between sample and mold is kept constant preventing any damage to the wafer.
- Injection speed is controlled to smoothly fill the mold with a transfer speed starting at 5mm/s, slowing down to 2 mm/s and lower.
- Temperature(175°C) and pressure (7 MPa) kept constant for the time needed for pre-curing of the EMC (7 min).
- After curing, the molding press opens and the molded wafer is removed.
- Post mold cured for 4hrs at 175°C.



Solder bumping process

Wafer level solder ball placement by using a stencil:

- vacuum picking of solder balls from reservoir
- removal of excess balls & optical inspection
- Wafers are printed with flux material
- placement of solder balls on the wafer
- schematic showing the ball placement



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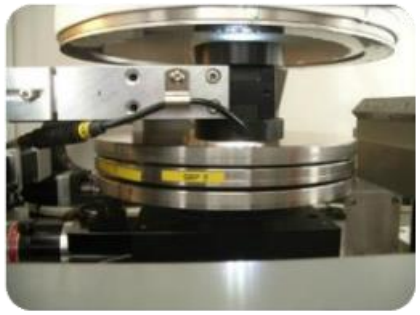

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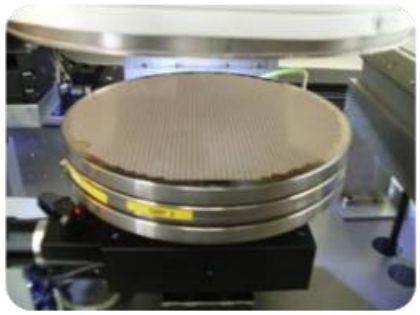

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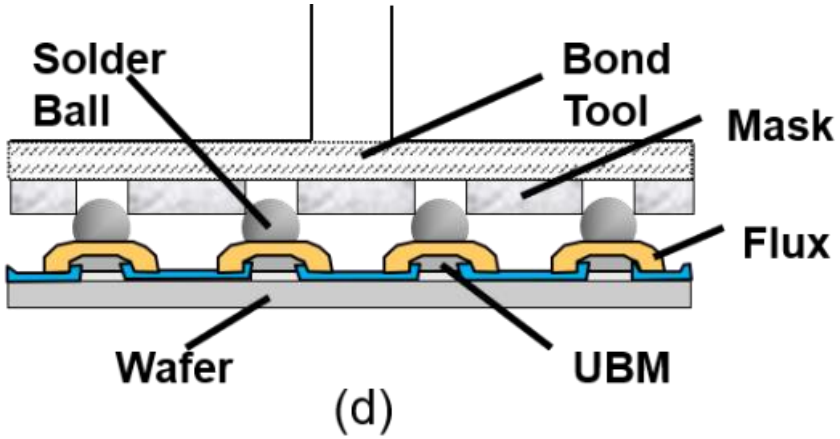

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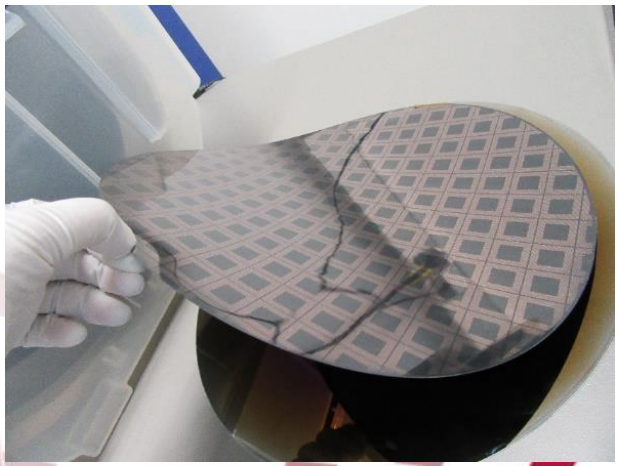
Solder bumping process

- Handling w/o carrier is complicated due to the “paper-like” nature of the wafers.
- Image of the wafer surface after ball placement process using flux printing but before reflow.
- Solder Ball placement on these molded wafers look quite promising.



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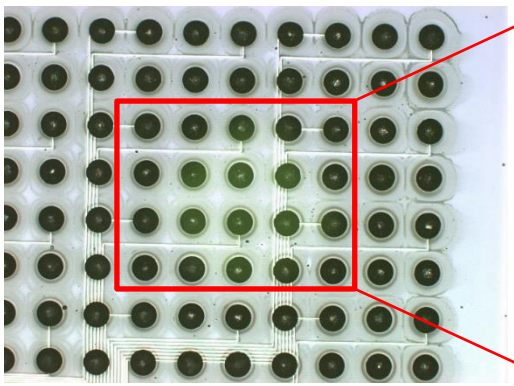

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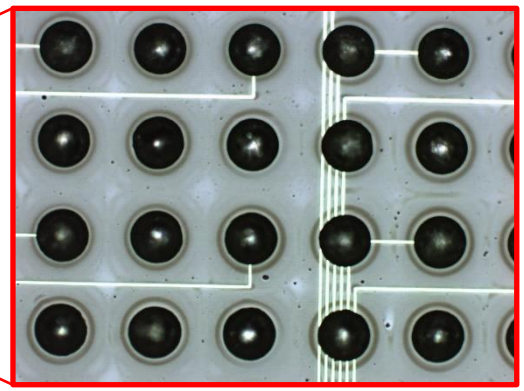

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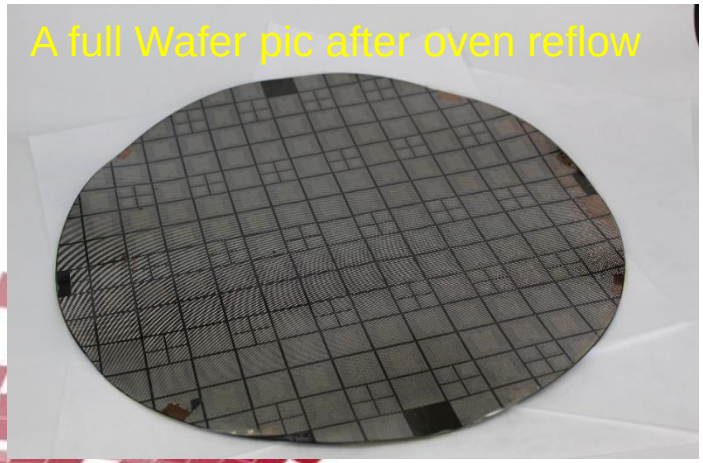
Reflow optimization

- Performing a reflow on molded wafers is challenging due to thermal & mechanical stress @ high temp.
- Mechanical stress and deformation of the molded wafer is observed due to the EMC shrinkage at high temp. and CTE mismatch between Si chip and mold compound
- Solder reflow to a peak temperature of ~250°C is critical due to their thermal fragility
- Low melting temperature solder alloys like In-Sn or In-Bi → limits many operations on the device
- Reflow inside an oven shows discoloration of mold material and a very high wafer warpage observed → high risk of wafer breakage
- Laser reflow helps to overcome this problem → localized reflow on the pads by laser scanning



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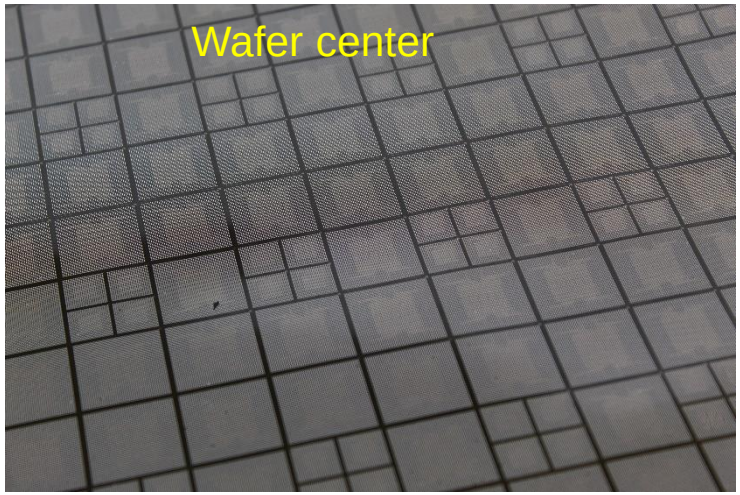
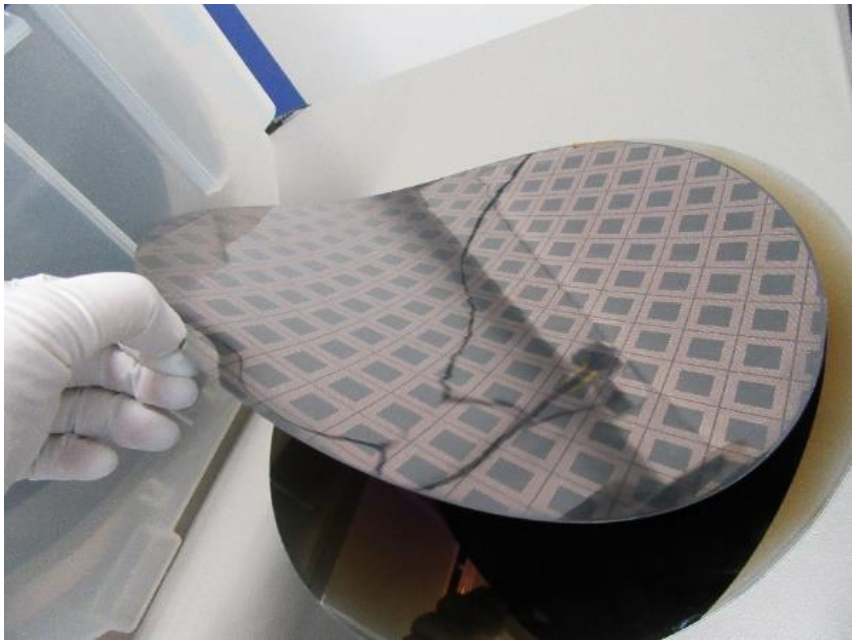


Laser scanning reflow

- Laser reflow helps to overcome problem of wafer warpage & breakage
- Involves localized reflow on the pads by laser scanning
- PacTech`s LaPlace tool system is used for this purpose
- A laser pulse of 500ms is used
- Measured temperature at this pulse is 250°C.

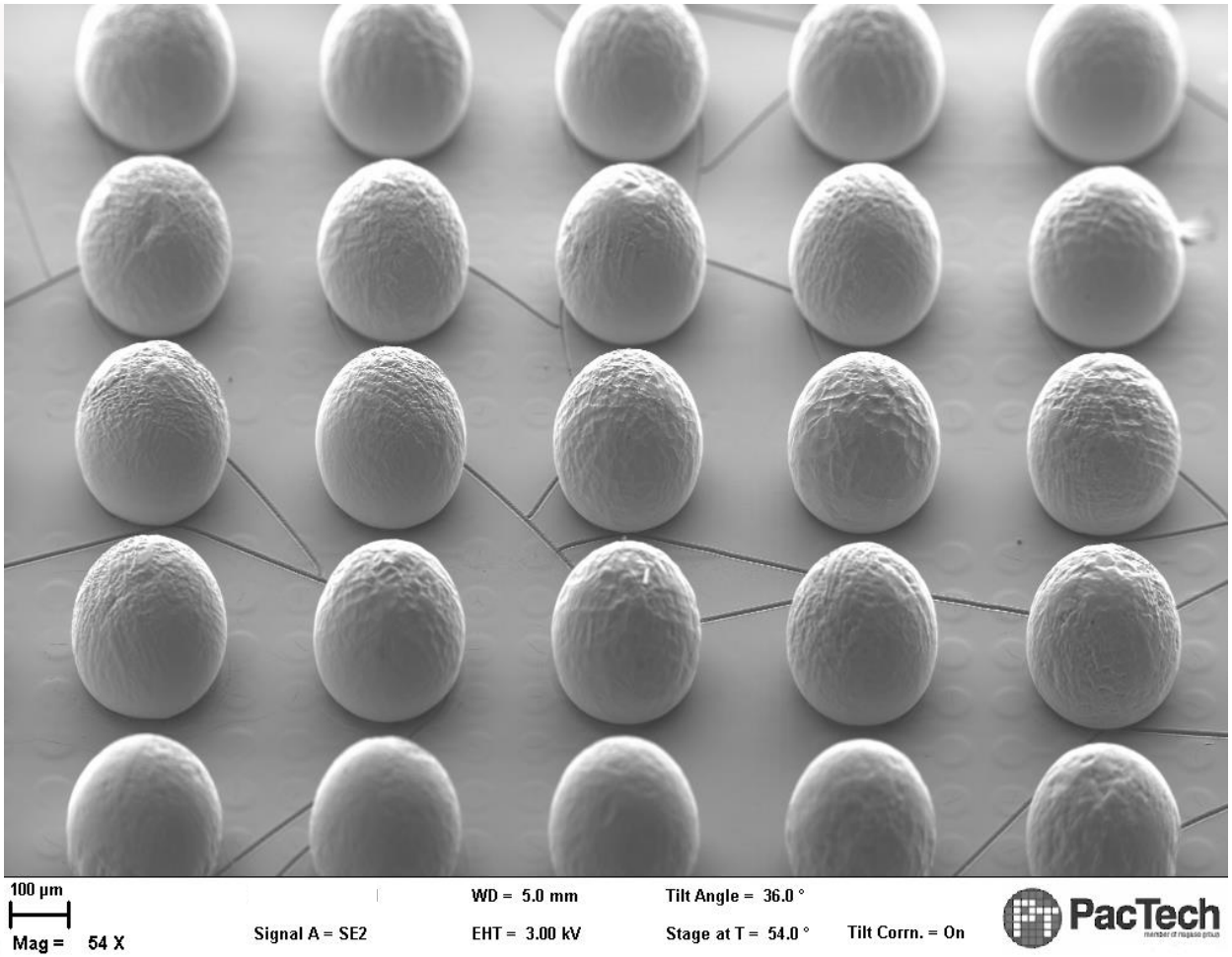
Handling challenges

- Challenges in handling: Picture of the wafer after removing from the backside tape. Handling w/o carrier is complicated due to the “paper-like” nature of the wafers.
- Transport plate used for moving through different stations
- Wafers are warped; warpage ~1mm
- Problems during reflow:
  - EMC shrinkage: deformation of mold material
  - mechanical & thermal stress at high temp.



Bumps quality check

- SEM image of wafer surface after solder bumping process
- Shear test: average shear force value ~150g for 200µm pads.
- Mechanical test done with a jaw passed



Conclusions

- Process flow for proving RDL-1st FOWLP concept is established
- High density Cu RDL with 5µm line/space is used
- A transfer molding process to produce the RDL 1st molded wafers
- Solder bumping process of RDL-1st FOWLP wafers is evaluated at wafer-level
- Handling challenges during these evaluations are explained
- A good solder placement process could be observed; but a following oven reflow process was quite challenging
- A laser scanned reflow on localized pads helped to overcome the constraints

PacTech
member of nagase group

Thank you !!