Electronic Packaging Lab
Department of Materials Science and Engineering, NCKU

17TH INTERNATIONAL CONFERENCE ON • APRIL 12-15, 2021
DEVICE PACKAGING
A GLOBAL VIRTUAL EVENT • WWW.DEVICEPACKAGING.ORG

Electromigration Study of a Novel Cu Stack-via Interconnect for Advanced High-density Fan-out Packaging

Kuan-Ju Shao[1], Min-Yan Tsai[2], Chien-Lung Liang[1], Chin-Li Kao [2], Gao-Tian Lin [3], and Kwang-Lung Lin[1]

1. Department of Materials Science and Engineering, National Cheng Kung University, No. 1, University Road, Tainan 70101, Taiwan.
2. Advanced Semiconductor Engineering (ASE) Group, No. 26, Chin 3rd Road, Kaohsiung 81170, Taiwan.
3. VIACPU Technologies, No. 525, Zhongzheng Road, New Taipei City 23148, Taiwan.

ASE GROUP

NATIONAL CHENG KUNG UNIVERSITY 1931

About the Presenter

- Kuan-Ju Shao, National Cheng Kung University
  - National Cheng Kung University (NCKU) undergraduate degree
  - National Cheng Kung University (NCKU) graduate student in Department of Materials Science and Engineering
  - Field of research : Pb-free solder joint, electromigration
- Acknowledgement :
  - Ministry of Science and Technology, Taiwan (MOST107-2221-E-006-014-My3)
  - Specimens provided by ASE group and VIACPU Technologies

Introduction

Cu via technology has been developed as interconnect for connecting the Cu redistribution lines (RDLs) . A novel Cu stack-via presented in this article can be applied to the advanced fan-out chip on substrate (FOCoS) packaging for the purpose of space-saving and high density packaging.

FOCoS packaging was proposed to meet the growing demands of small dimension and multifunctional electronics. With the advantages[2] of good electrical performance, lower cost, thinner package, and a high-end resolution to the high density (I/O number >1000), the FO packaging technology is expected to be applied on the products with high-density packaging requirements, such as artificial intelligence (AI) and 5G applications .

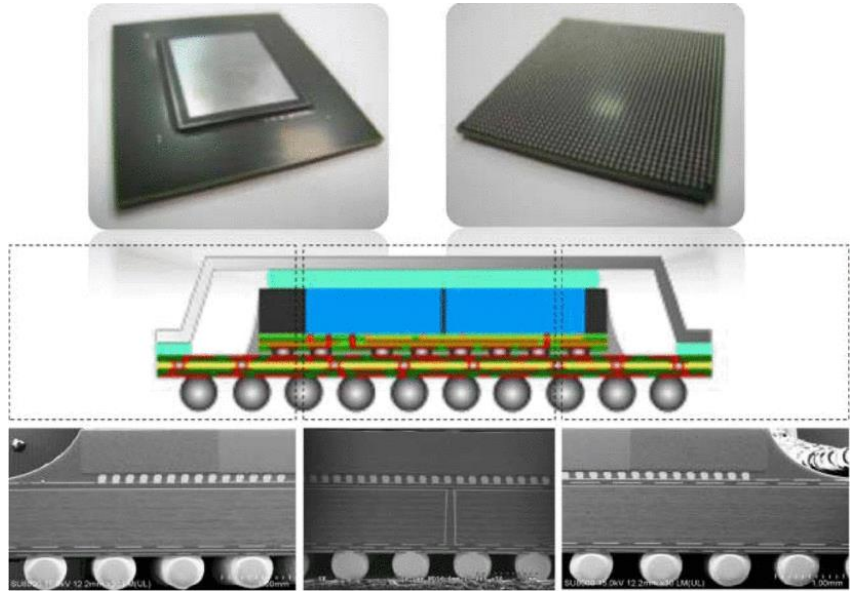


Figure 1 The real images and SEM cross section images of FOCoS package.[1]

[1] Y. Lin *et al., 2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, pp. 13-18 (2016)

[2] C. -L. Liang *et al.*, "*IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 9, pp. 1438-1445 (2020)

Introduction

Electromigration is known as a phenomenon to describe the mass transport driven by electron wind force with the presence of an electric field. However, the electromigration reliability studies on high-density packaging devices with the novel Cu stack–via interconnect are not extensive yet. Accordingly, in this work, the electromigration behavior was investigated in terms of electrical resistance change and microstructure evolutions to explore the failure mechanism.

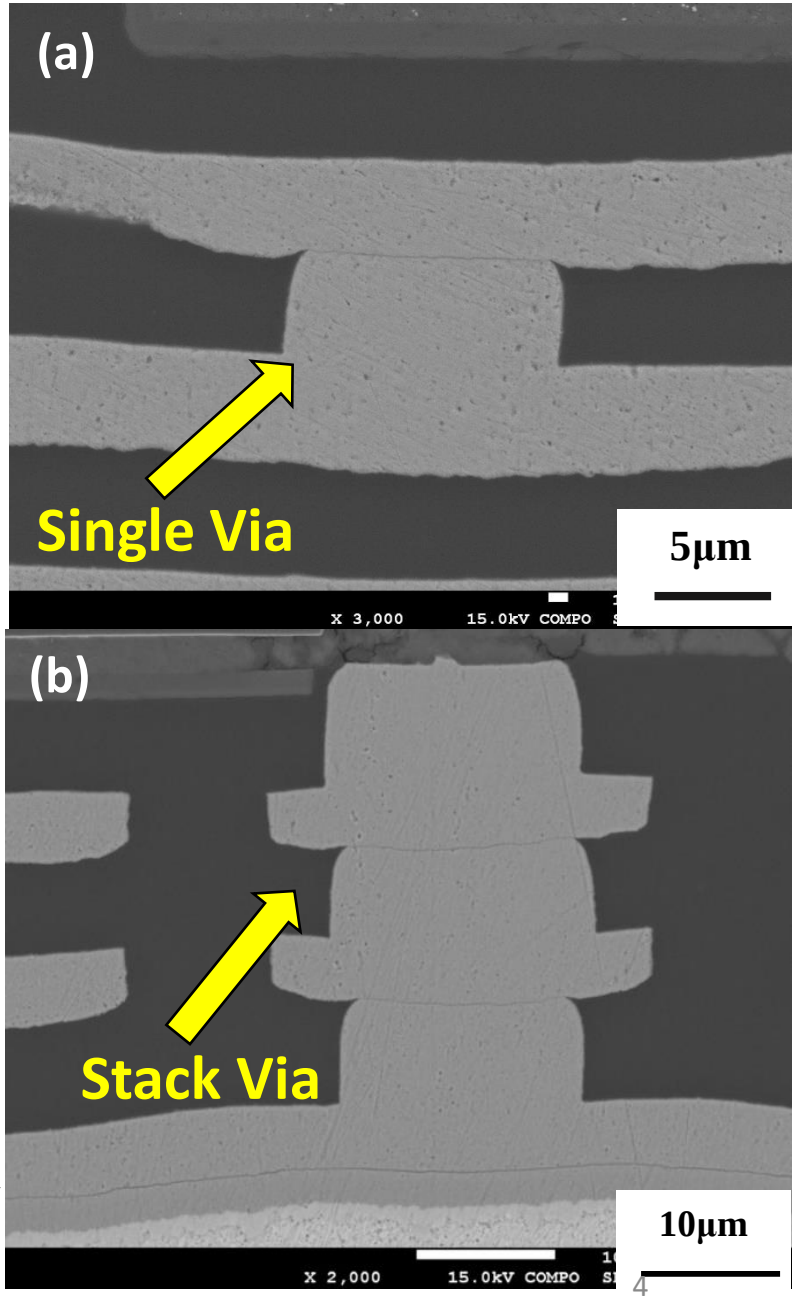


Figure 2 (a) SEM cross-sectional image of Cu single via
(b) SEM cross-sectional image of Cu stack-via

Experimental Procedure

EM experiment parameters :

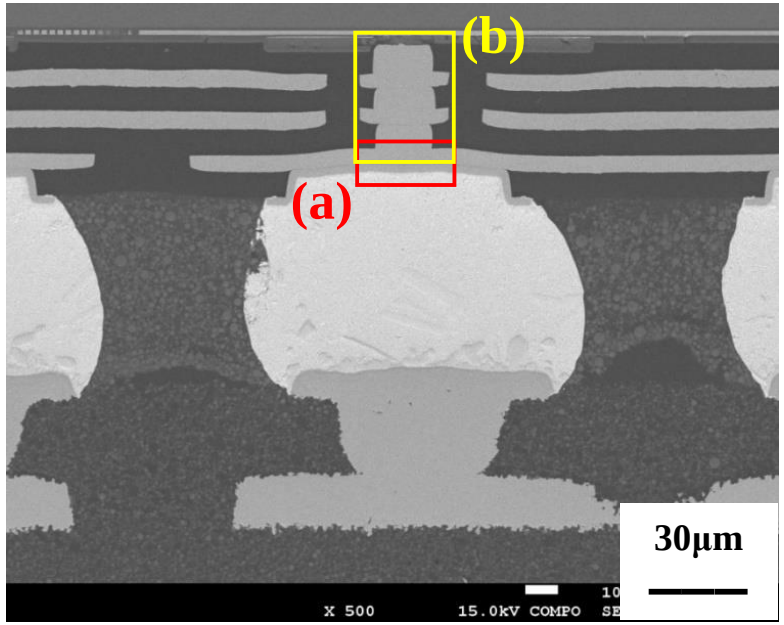
1. Current density：0.9 A, approximately 5.1×10^5 A/cm^2
2. Stressing time： 591.2, 855.7, and 1450.2 hours
3. Environment temperature ：180^{o}C
4. Electron flow direction

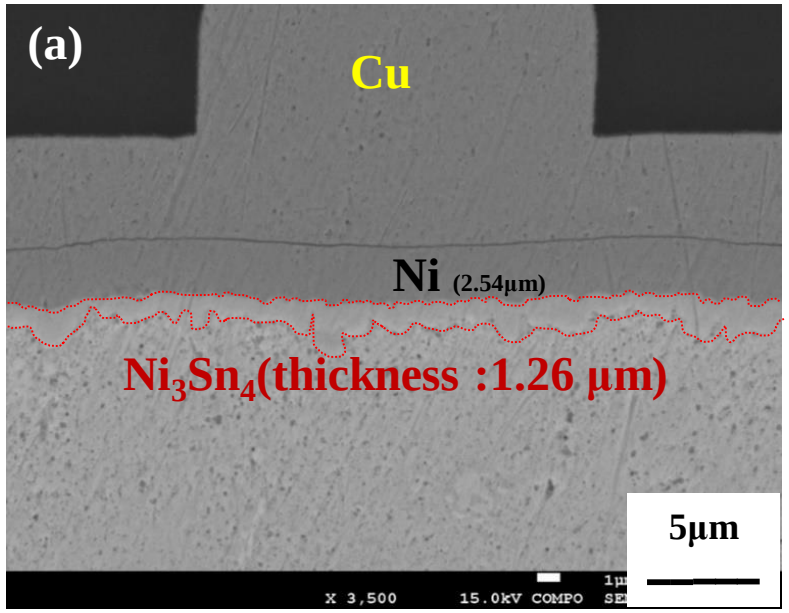
(a) e^- upward : cathodic interconnect (b) e^- downward : anodic interconnect

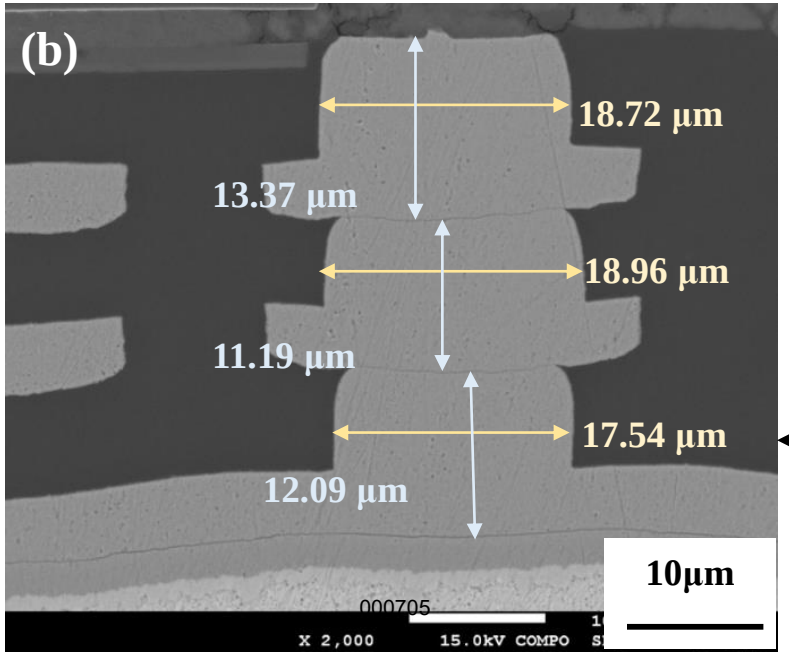
Outline

- **Results and Discussion**
  - **The microstructure of the stack-via/metallization**
  - **Cathodic interconnects**
  - **Anodic interconnects**
  - **Resistance variation for stack-via**

Results and Discussion







The IMCs formed at the interface were identified as Ni_3Sn_4 by EDS, also the thicknesses of IMC and the metallization layer were calculated as the figures show.

Specimen structure :
Si chip/Cu stack-via/Ni metallization/
Sn-Ag /Ni(P) metallization/Cu trace

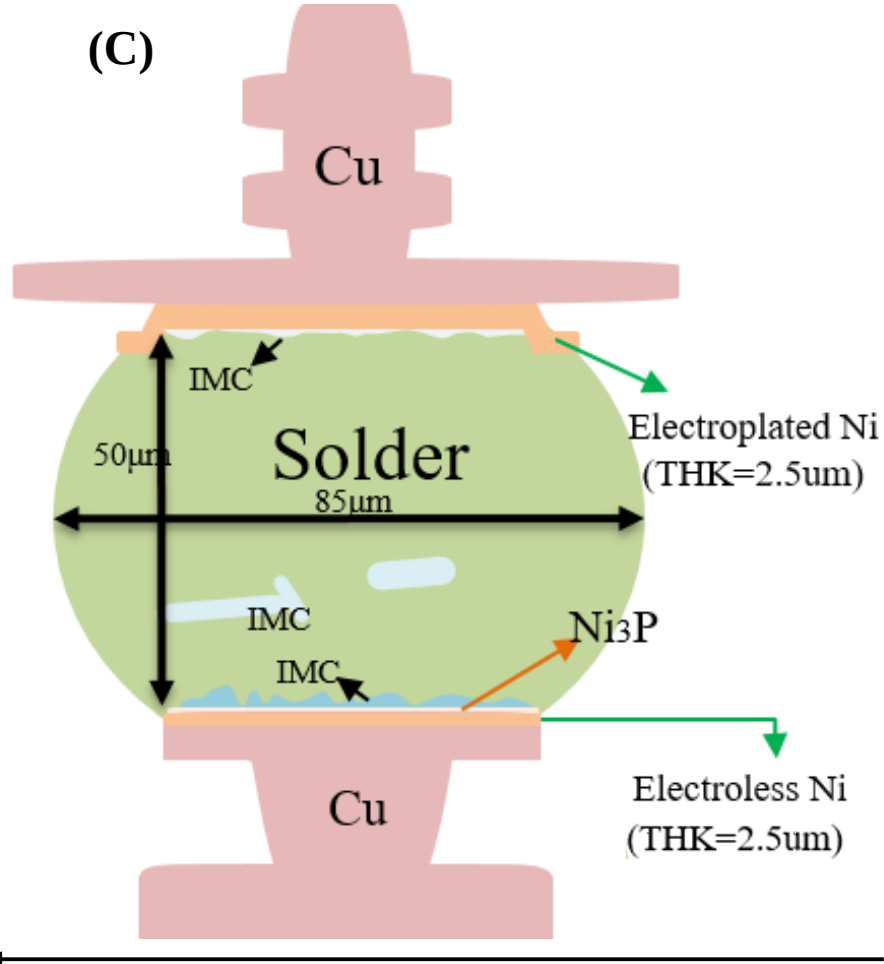
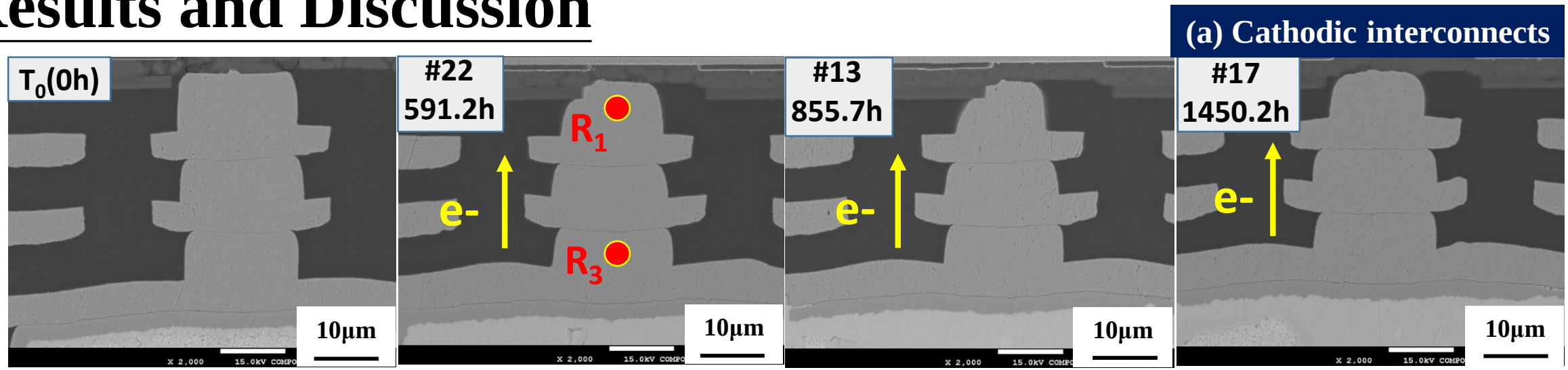


Figure 3
The microstructure of (A) metallization (B) stack-via (C) solder bump schematic picture

Outline

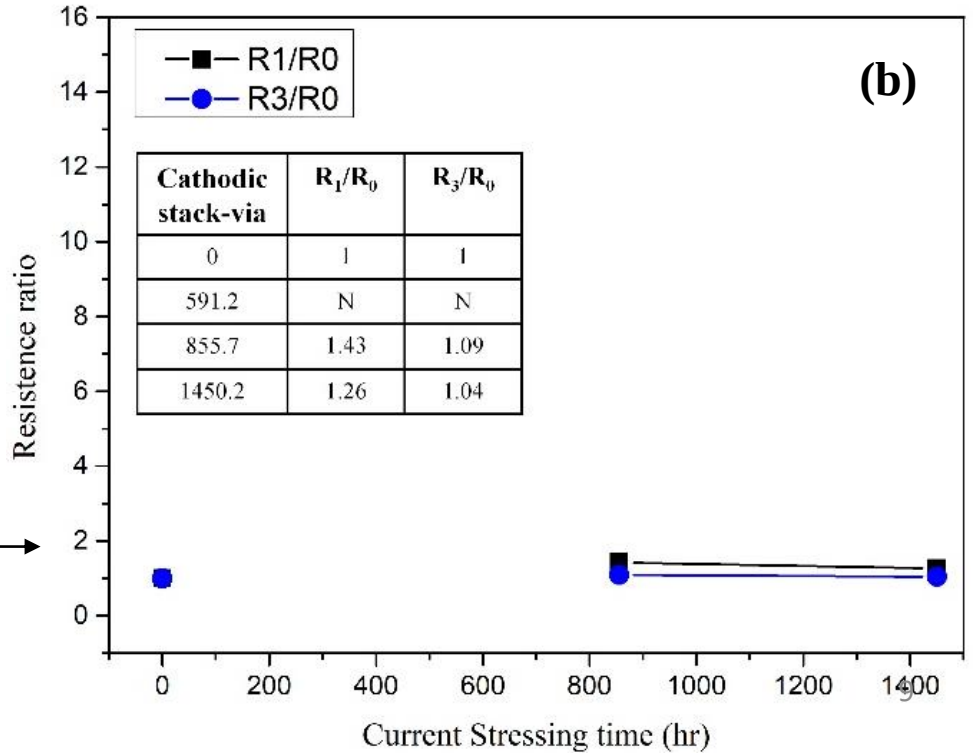
- **Results and Discussion**
  - The microstructure of the stack-via/metallization
  - **Cathodic interconnects**
  - Anodic interconnects
  - Resistance variation for stack-via

Results and Discussion



R_1 : The resistance of via1 R_3 : The resistance of via3
R_0 : The initial resistance of stack-via

For the Cu stack-via suffering upward electron flow, we found insignificant change in microstructure and resistance fluctuation when the current stressing time was up to 1450 hours.



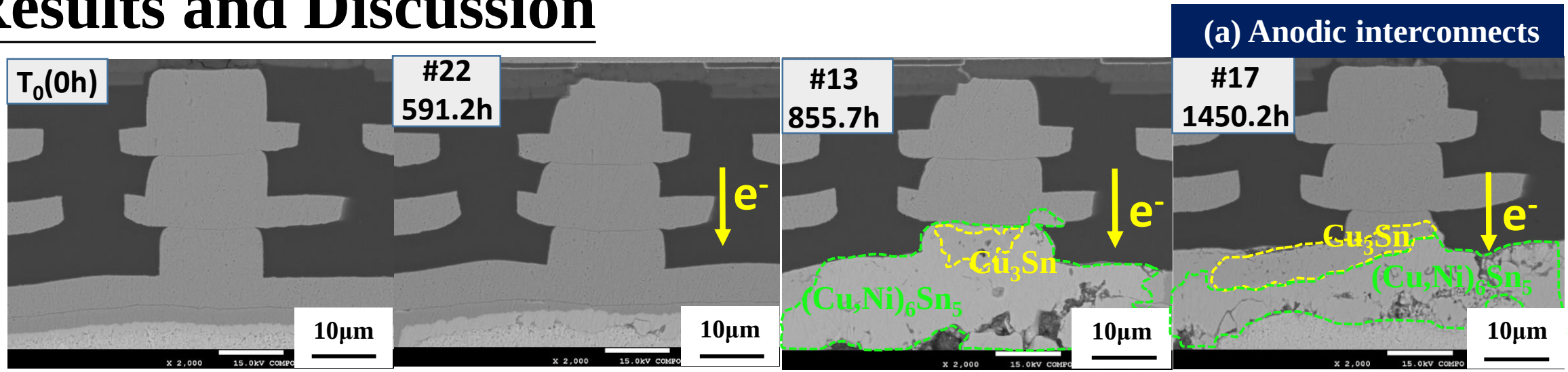
Cathodic stack-via	R_1/R_0	R_3/R_0
0	1	1
591.2	N	N
855.7	1.43	1.09
1450.2	1.26	1.04

Figure 4 (a) The microstructure of cathodic stack-via with different current stressing time with (b) the corresponding resistance measurement ratio R_1/R_0 and R_3/R_0

Outline

- **Results and Discussion**
  - The microstructure of the stack-via/metallization
  - Cathodic interconnects
  - **Anodic interconnects**
  - Resistance variation for stack-via

Results and Discussion



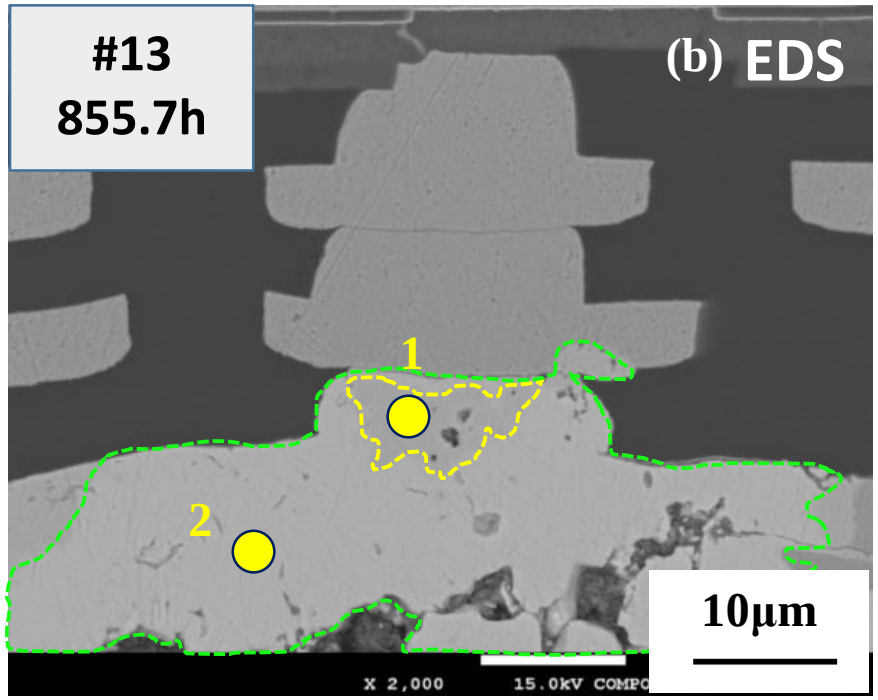
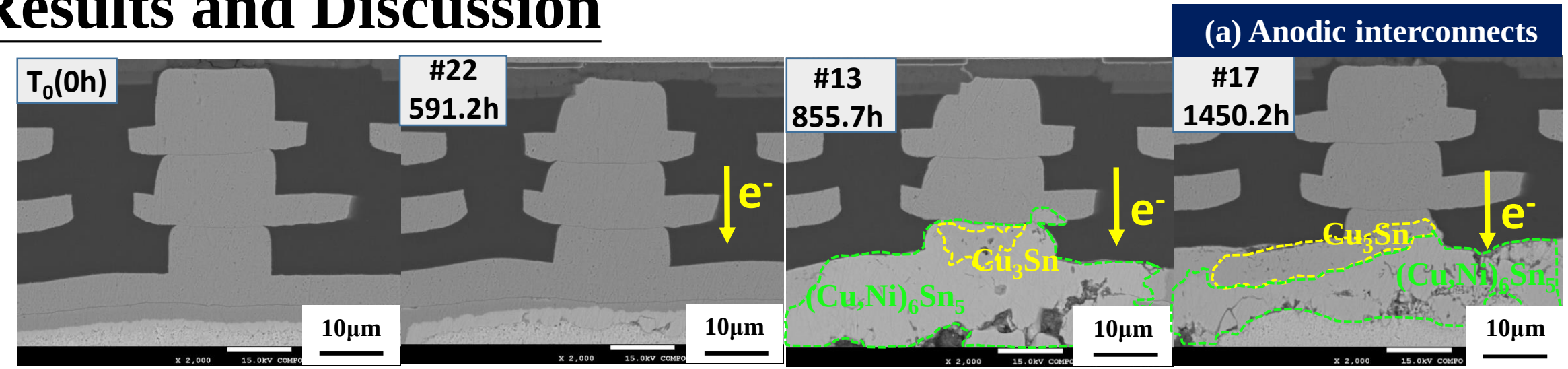


Table 1 The EDS composition analysis for IMCs

	Cu (at%)	Sn (at%)	Ni (at%)	Ag (at%)	IMC
1	73.60	23.89	2.00	0.51	**Cu_3Sn**
2	32.78	24.24	42.81	0.17	**$(Cu,Ni)_6Sn_5$**

Figure 5
(a) The microstructure of anodic stack-via with different current stressing time
(b) The microstructure of anodic stack-via under 855.7 hours current stressing

Results and Discussion



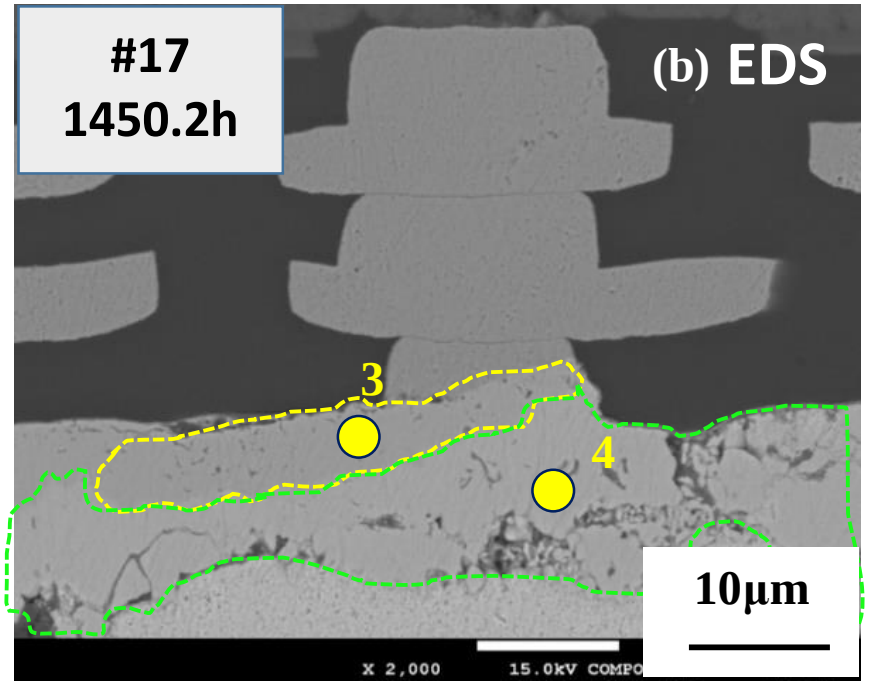
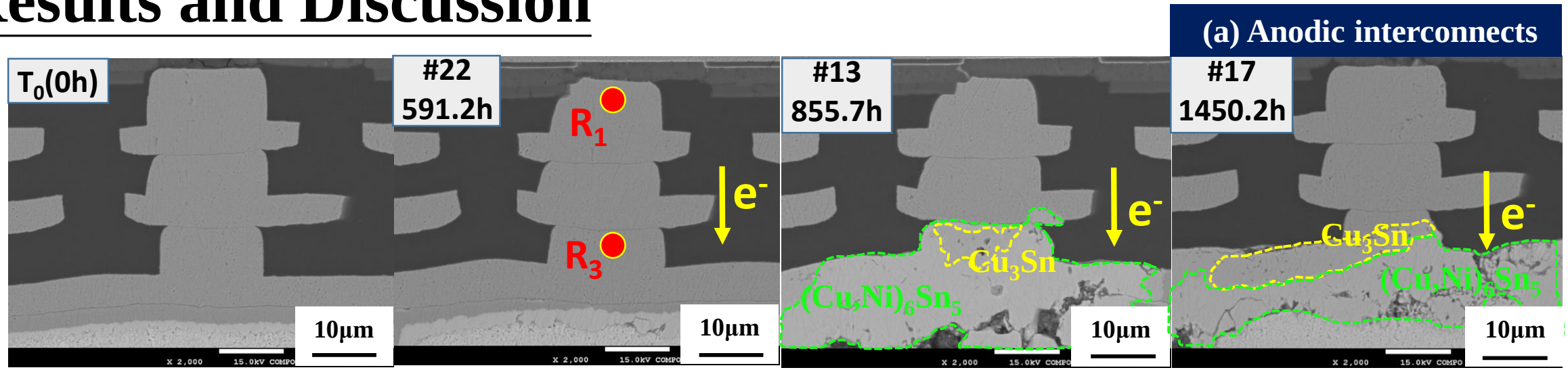


Table 2 The EDS composition analysis for IMCs

	Cu (at%)	Sn (at%)	Ni (at%)	Ag (at%)	IMC
3	74.07	23.33	2.30	0.31	**Cu_3Sn**
4	33.42	22.65	43.93	0	**$(Cu,Ni)_6Sn_5$**

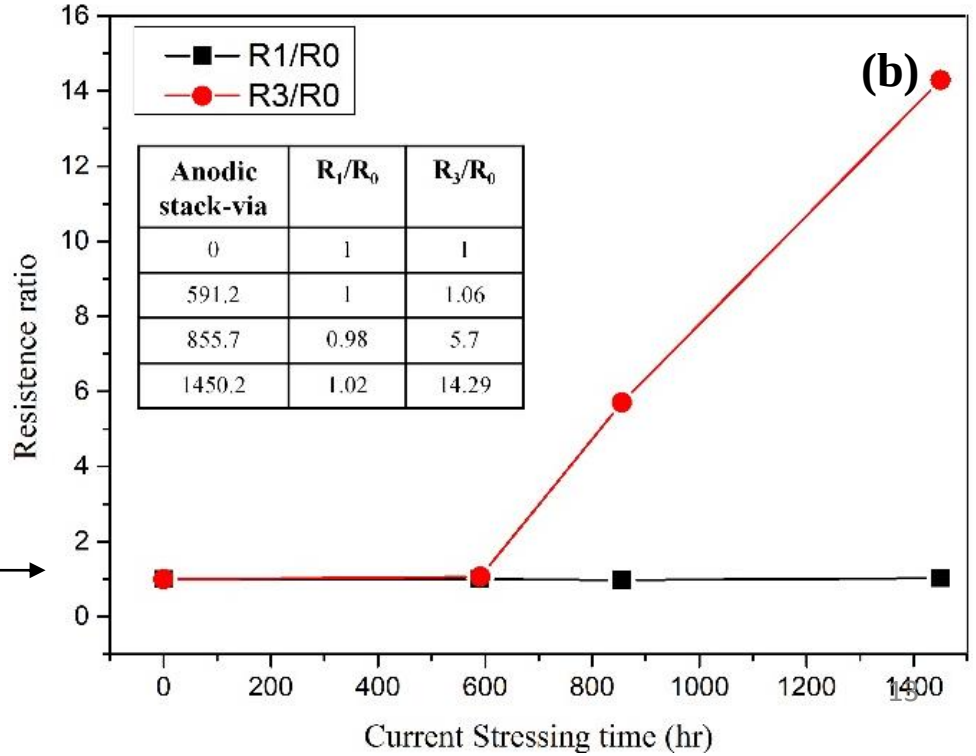
Figure 6
(a) The microstructure of anodic stack-via with different current stressing time
(b) The microstructure of anodic stack-via under 1450.2 hours current stressing

Results and Discussion



It was investigated that insignificant resistance fluctuation in R_1 via while the prominent resistance rise in R_3 via in the anodic interconnects.

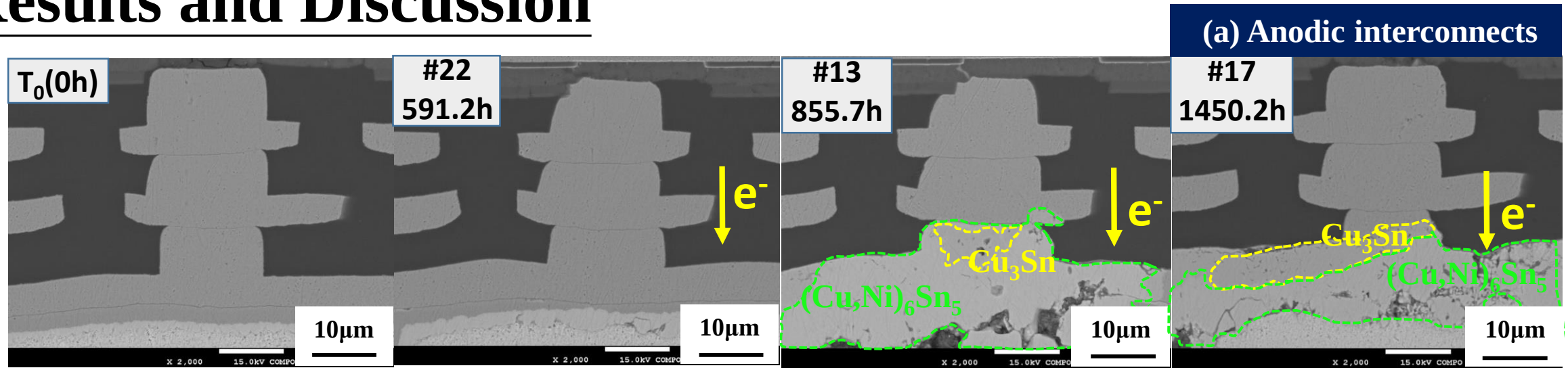
The dramatic resistance change can result from two possible factors.



Anodic stack-via	R_1/R_0	R_3/R_0
0	1	1
591.2	1	1.06
855.7	0.98	5.7
1450.2	1.02	14.29

Figure 7 (a) The microstructure of anodic stack-via with different current stressing time with (b) the corresponding resistance measurement ratio R_1/R_0 and R_3/R_0

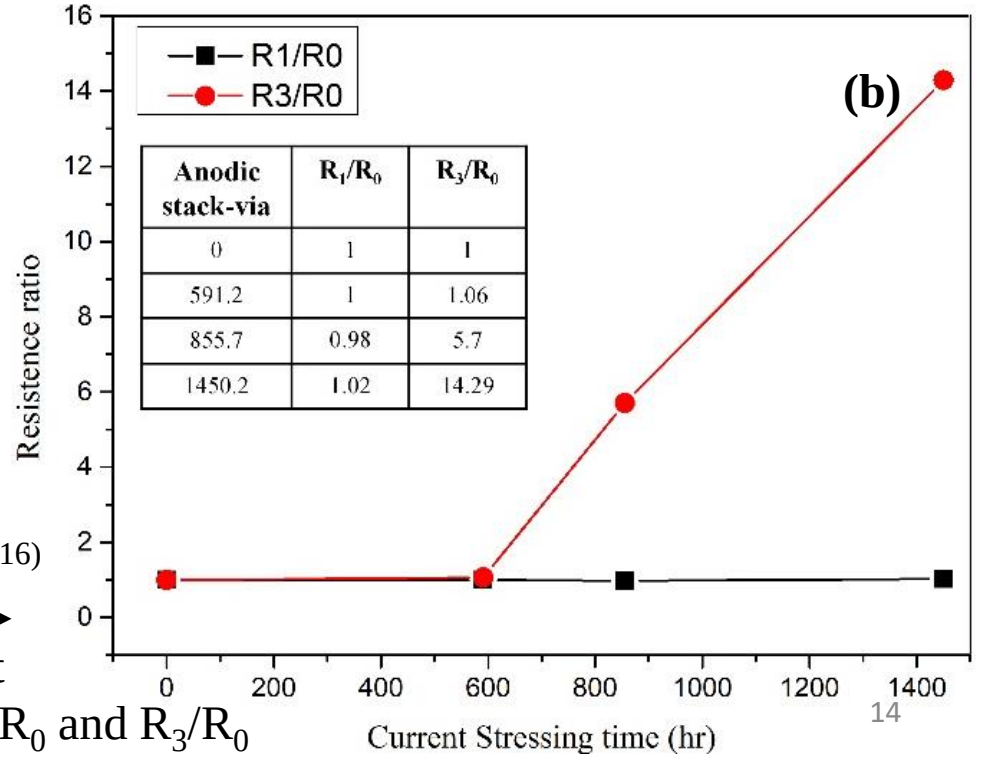
Results and Discussion



Two factors lead to the dramatic rise in resistance：

A. Voids/crack formation in IMCs

The voids formation was attributed to the volume shrinkage due to the phase transformation from Cu to Cu-Sn IMCs. (-4.49%[3] and -7.5%[4] for Cu_6Sn_5 and Cu_3Sn respectively.)

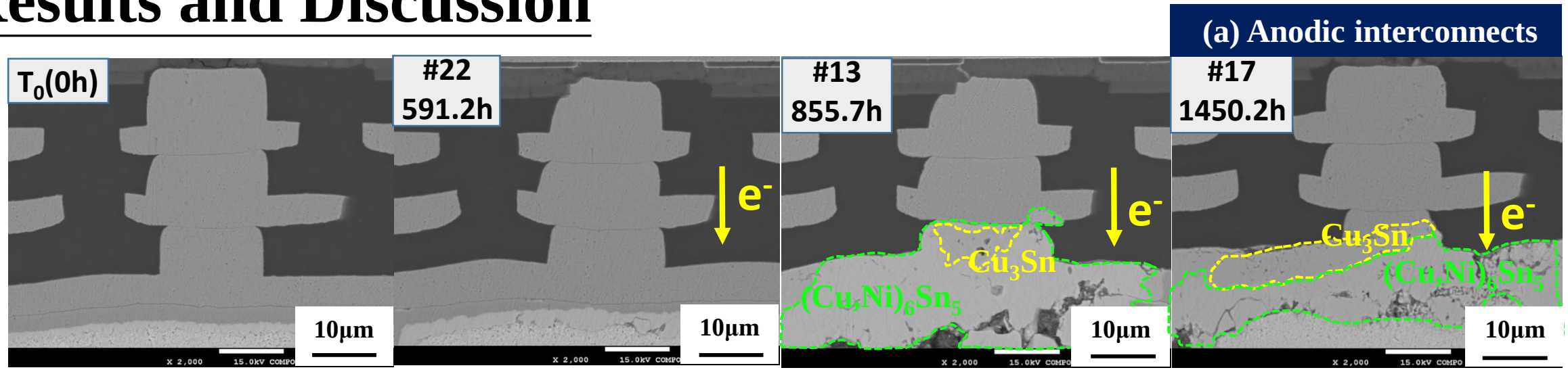


[3] Y. C. Chu *et al.*, *2016 International Conference on Electronics Packaging*, Hokkaido, Japan, pp. 252-255 (2016)

[4] C. C. Lin *et al.*, *Metall Mater Trans A 45*, pp. 2343–2346 (2014)

Figure 8 (a) The microstructure of anodic stack-via with different current stressing time with (b) the corresponding resistance measurement ratio R_1/R_0 and R_3/R_0

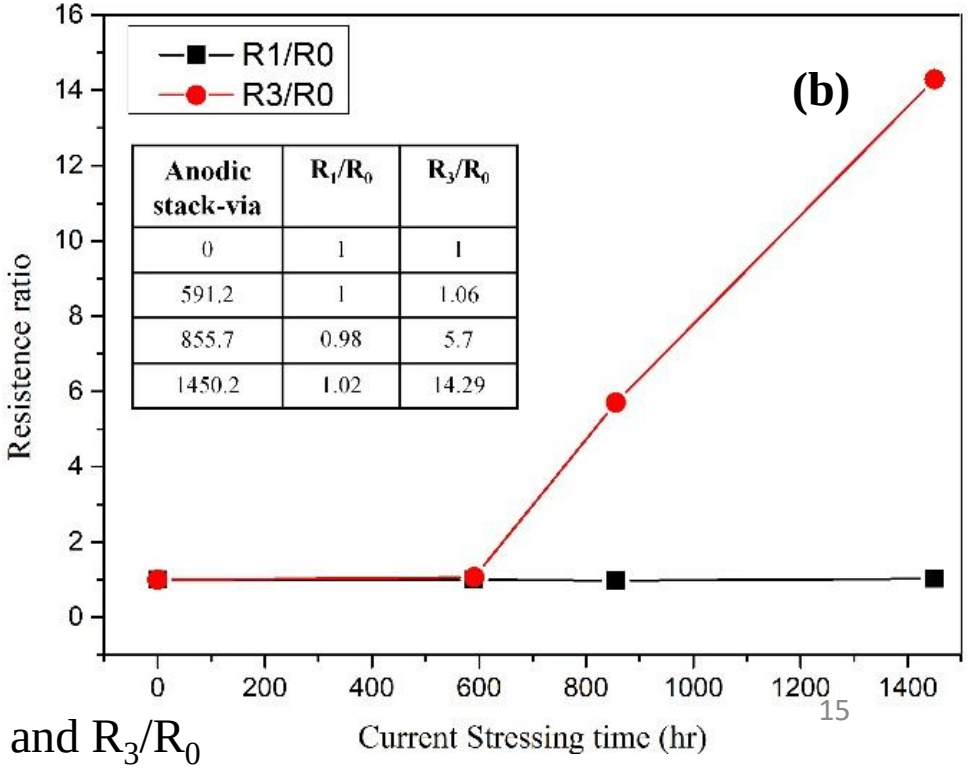
Results and Discussion



Two factors lead to the dramatic rise in resistance：

A. Voids/crack formation in IMCs

B. It was reported that the electrical resistivity of these intermetallic phases was approximately 5 to 10 times greater than that of the Cu phase[5].
(1.66, 17.5, and 8.9 μΩ-cm for Cu, Cu_6Sn_5, Cu_3Sn respectively)



Anodic stack-via	R_1/R_0	R_3/R_0
0	1	1
591.2	1	1.06
855.7	0.98	5.7
1450.2	1.02	14.29

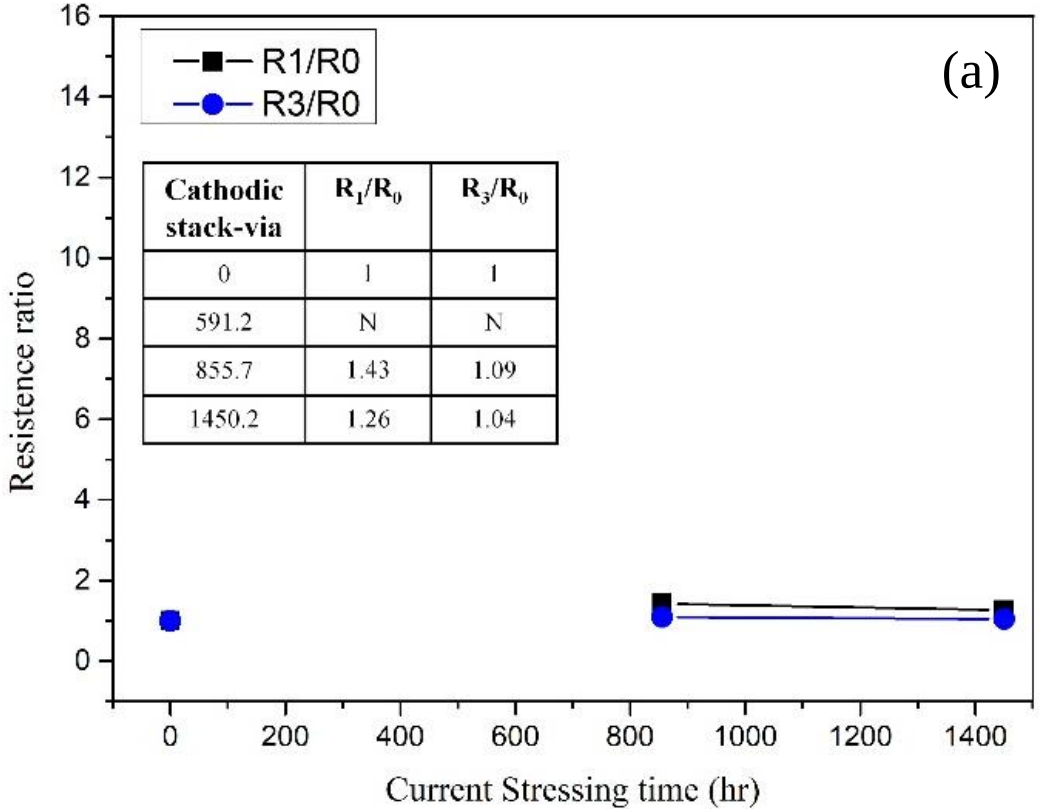
[5] C. L. Liang *et al.*, *Surf. Coat. Technol.*, vol. 319, pp. 55-60 (2017)

Figure 9 (a) The microstructure of anodic stack-via with different current stressing time with (b) the corresponding resistance measurement ratio R_1/R_0 and R_3/R_0

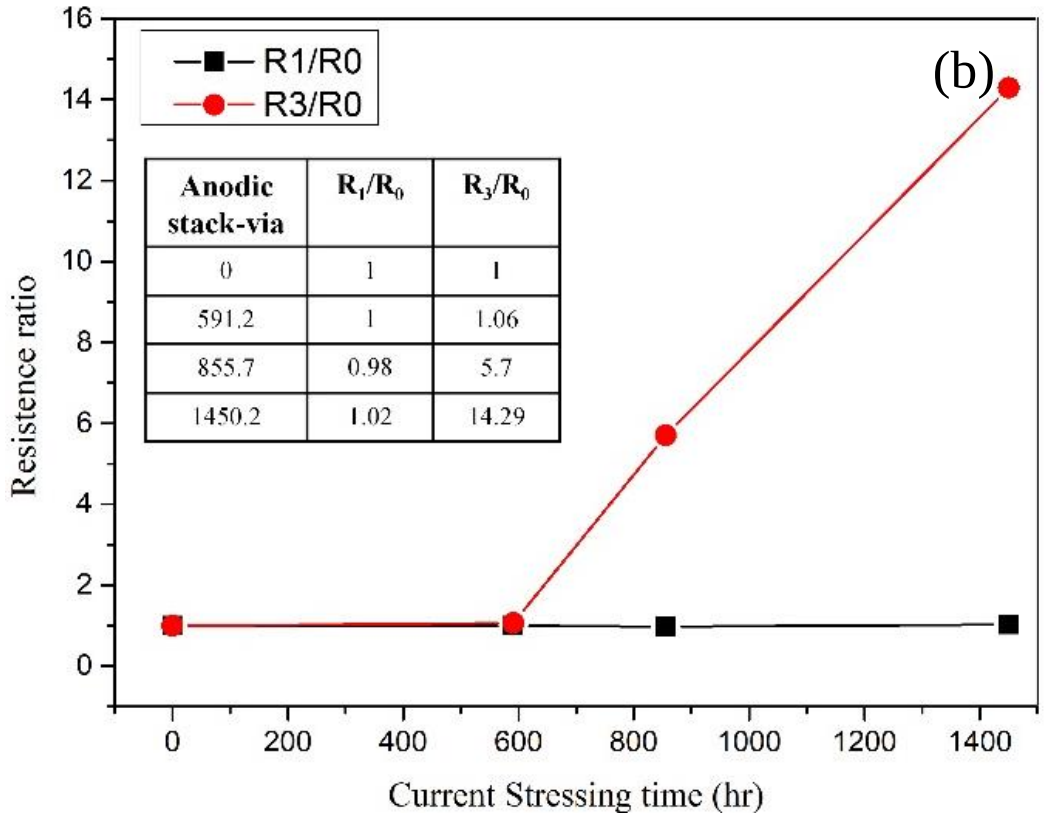
Outline

- **Results and Discussion**
  - The microstructure of the stack-via/metallization
  - Cathodic interconnects
  - Anodic interconnects
  - **Resistance variation for stack-via**

Results and Discussion



Cathodic stack-via	R_1/R_0	R_3/R_0
0	1	1
591.2	N	N
855.7	1.43	1.09
1450.2	1.26	1.04

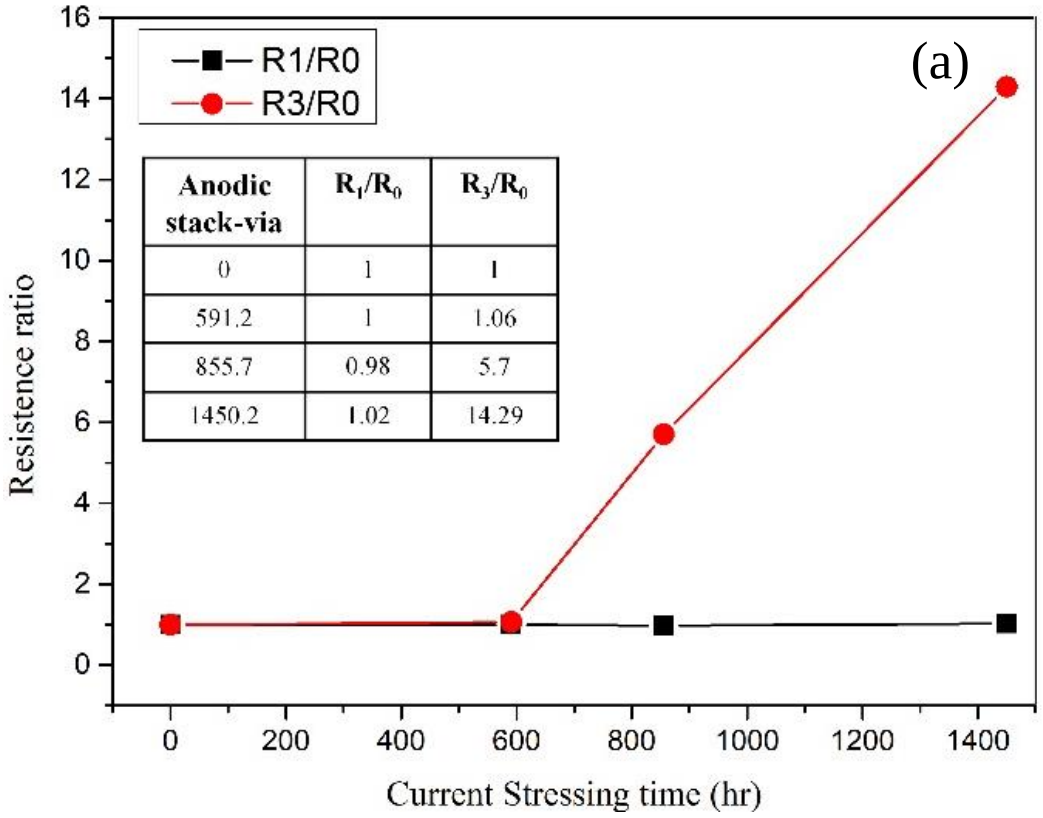


Anodic stack-via	R_1/R_0	R_3/R_0
0	1	1
591.2	1	1.06
855.7	0.98	5.7
1450.2	1.02	14.29

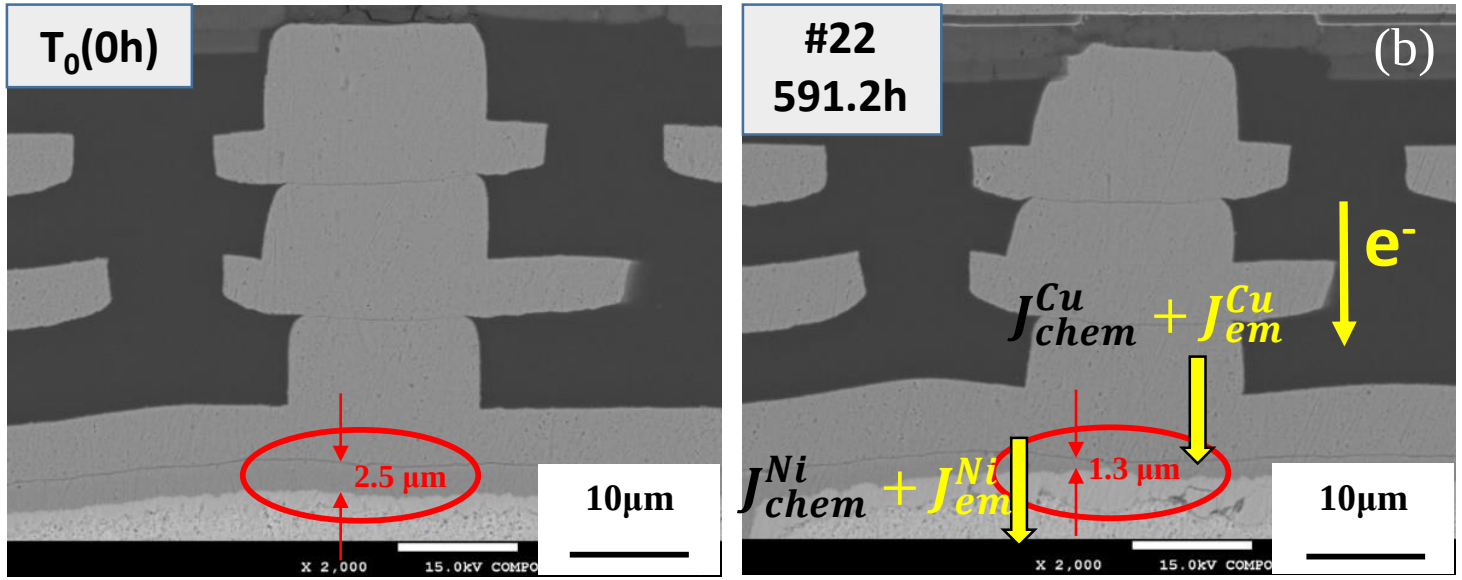
It's investigated that both the Cu stack-via and metallization have insignificant change in microstructure of cathodic interconnects, whose corresponding resistance showed a flat fluctuation. Due to the polarity effect, the consumption of Ni barrier layer in anodic interconnects was much more severe than that in cathodic interconnects, which contributed to the dramatic rise in resistance R_3.

Figure 10 The resistance measurement ratio R_1/R_0 and R_3/R_0 for (a) cathodic stack-via (b) anodic stack-via

Results and Discussion



Anodic stack-via	R_1/R_0	R_3/R_0
0	1	1
591.2	1	1.06
855.7	0.98	5.7
1450.2	1.02	14.29



J_{chem} : diffusion term due to the chemical potential gradient

J_{em} : diffusion term due to the electron momentum transfer effect

The chemical potential gradient and the electromigration driving force induced the diffusion of Ni atom from barrier layer to solder matrix, causing complete Ni metallization consumption and thereby triggering the Cu diffusion for the phase transformation.

Figure 11 (a) The resistance measurement ratio for anodic stack-via (b) the microstructure of anodic stack-via with flux sign

Conclusions

In summary, we studied the electromigration behavior of the novel Cu stack-via. For cathodic stack-via, there was no significant variation both in microstructure and resistance. However, the resistance ratio R_3/R_0 of anodic stack-via showed divergent, dramatic rise from 1.06 (591.2 h) to 14.29(1450.2 h).

In the corresponding microstructure of R_3 of anodic stack-via, it was found that via 3 is occupied by Cu-Sn IMCs growing with voids and crack production, which contributed to the dramatic resistance change.

The Cu-Sn IMCs would form on the via 3 after the Ni barrier layer was consumed completely. Accordingly, thickening of the Ni metallization was recommended for retarding the Cu diffusion and the effective inhibition of the Cu via phase transformation.

Thanks for your attention!

Contact Information

- Kuan-Ju Shao
- National Cheng Kung University (NCKU) undergraduate degree
- National Cheng Kung University (NCKU) graduate student
- Email : n56094067@ncku.edu.tw
- Field of research : Pb-free solder joint, electromigration