Setting the 600mm Large Panel Fan-Out Standard with M-Series™

Cliff Sandstrom – VP Technology Development at Deca
Tim Olson – CEO at Deca
Benedict San Jose – Material Scientist at Deca
Craig Bishop – CTO at Deca

iMAPS – April, 2021

My Bio

- VP of Technology for Deca Technologies
- Background includes front-end at Cypress Semiconductor before joining Deca in 2010
- Deca is currently an IP and Design company now as we sold our fab to nepes in 2020
- Education includes a Chemical Engineering and an MBA from University of Minnesota
- 30+ plus years of Semiconductor experience both in Asian and United States
- Contributions from

1. Tim Olson — CEO of Deca
2. Benedict San Jose — Materials Scientist of Deca
3. Craig Bishop — CTO of Deca

Setting the 600mm Standard with M-Series

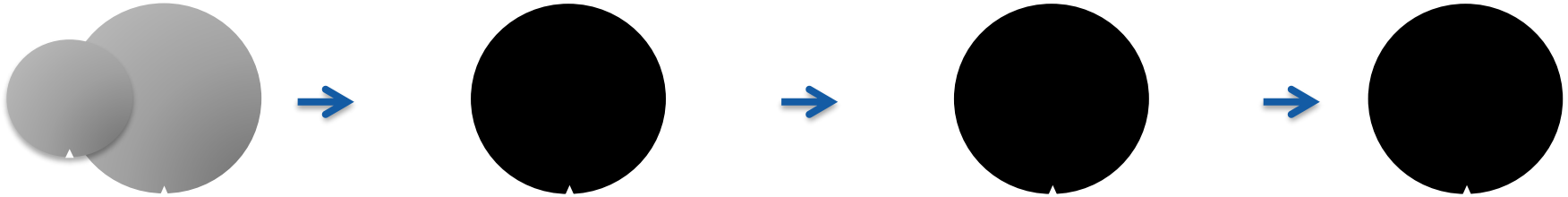
1. Background
2. Cost
3. Yield
4. Scaling
5. Conclusion

Background

- Inspired by SunPower's large area solar wafer processing including patterned polyimide, PVD seed metal, photoresist, thick Cu plating, strip and etch
- Deca proved large area methods borrowed from SunPower on 200mm & 300mm silicon wafer level chip scale packaging initially
- Key equipment, processes and materials were designed starting in 2009 to support large area build-up processing on the M-Series fan-out structure
- In 2013, Deca started piloting 600mm large panel fan-out
- Key considerations included:
    1. Ability to quarter panel into 300 x 300mm square segments after wafer fab processing for final test (allowing re-use of expensive capital assets running 300mm round wafers with handler kit upgrades)
    2. Although wafer fab processing occurs on a 600mm square format, the four 300mm square quadrants could be treated separately for key process characteristics including uniformity
    3. 300mm square segments were a straightforward extension of 300mm round processes
    4. 600mm was the largest square format which could be processed on key equipment including LDI lithography

Background

300mm round initial production format



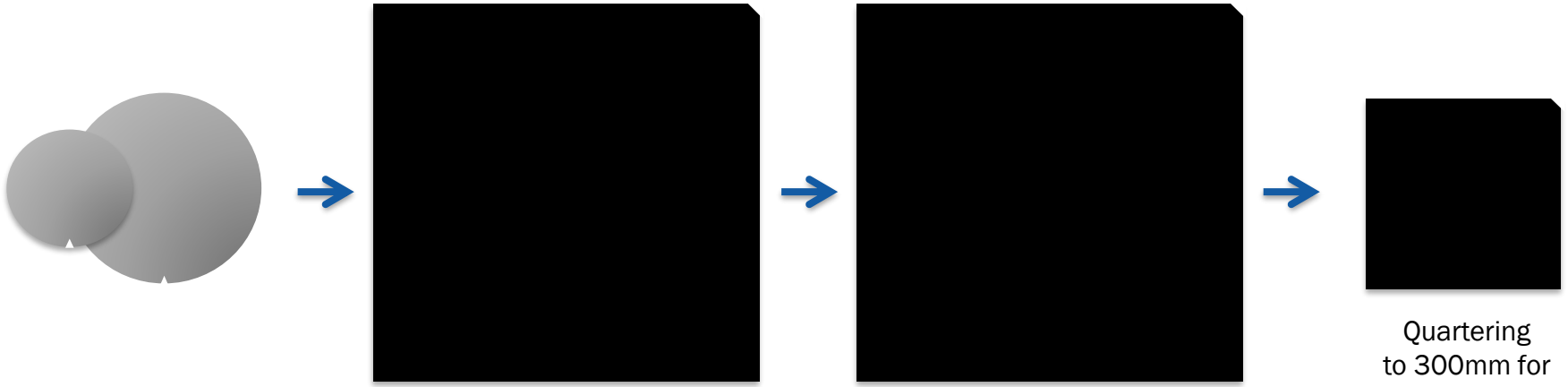
Customer Device Wafer
200 or 300mm

Panelization

Fan-Out

Final Test and BE2

600mm x 600mm large panel format



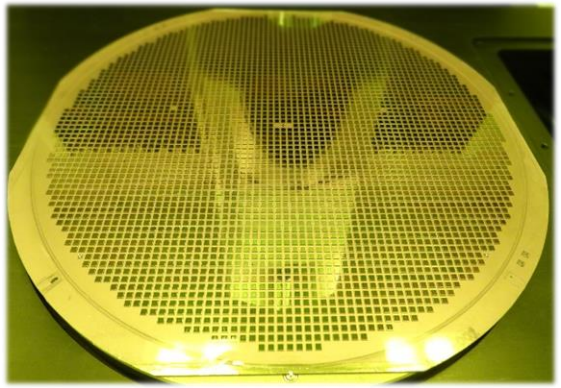
Panelization

Fan-Out

Quartering
to 300mm for
final test & BE2

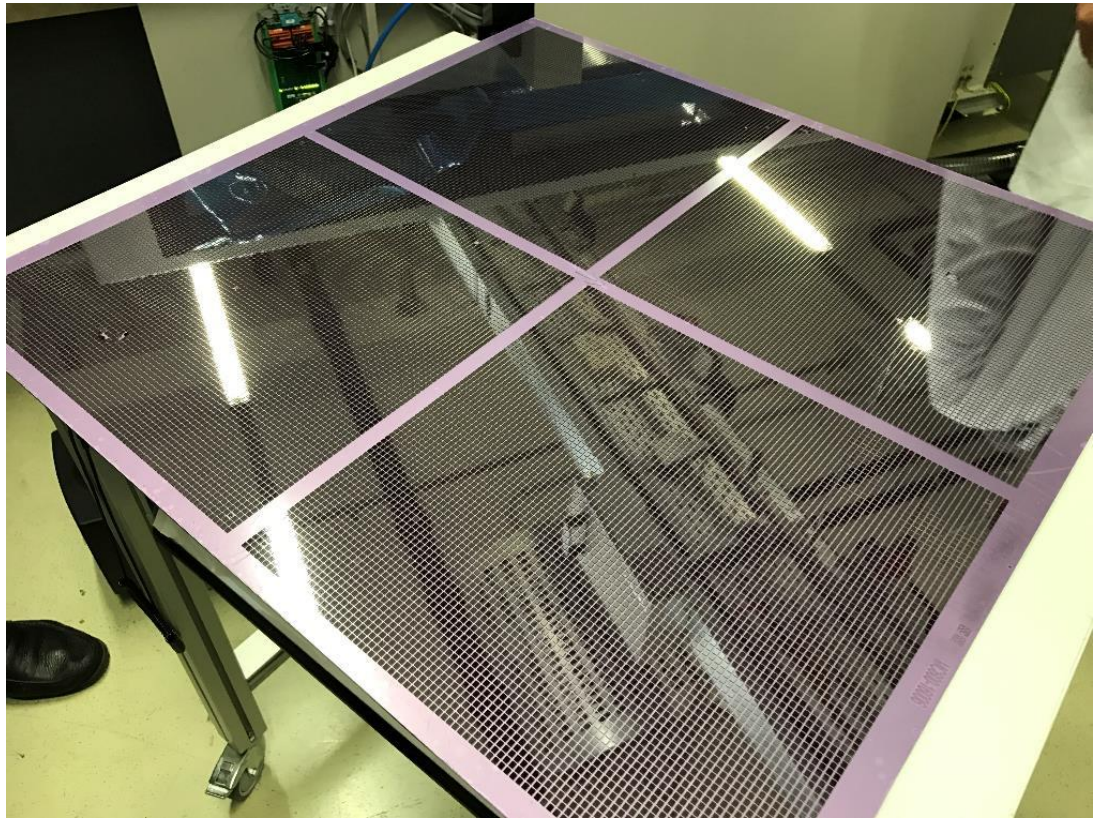
Background

M-Series™ – Post Chip Attach (on temporary carrier)



Courtesy of Deca

300mm round



Courtesy of Deca

600mm x 600mm

Background

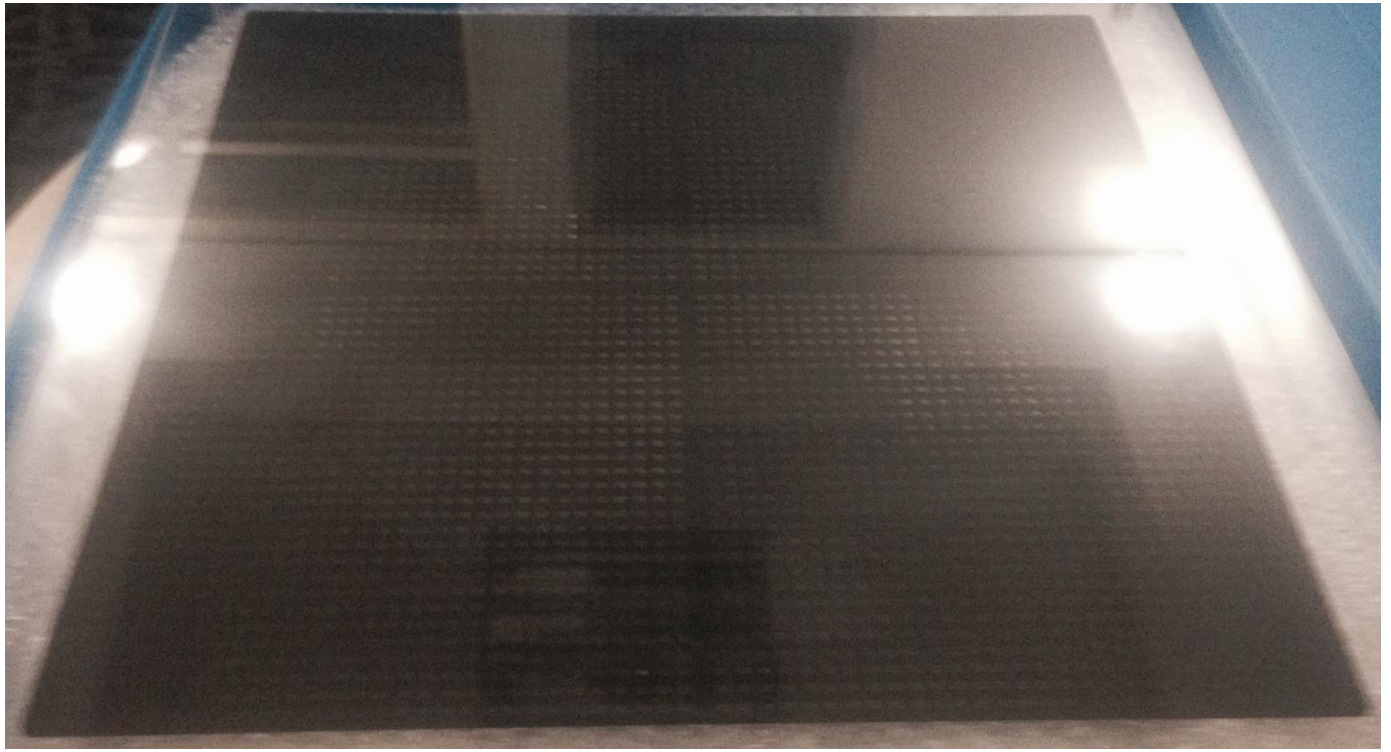
M-Series™ – Post Panelization

Initial production

Courtesy of Deca

300mm round

Large Panel Future Production



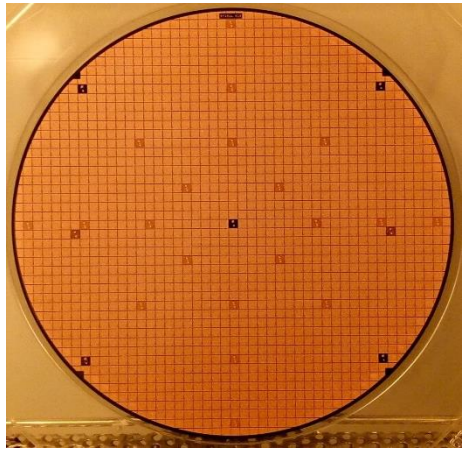
Courtesy of Deca

600mm x 600mm

Background

M-Series™ – Post RDL

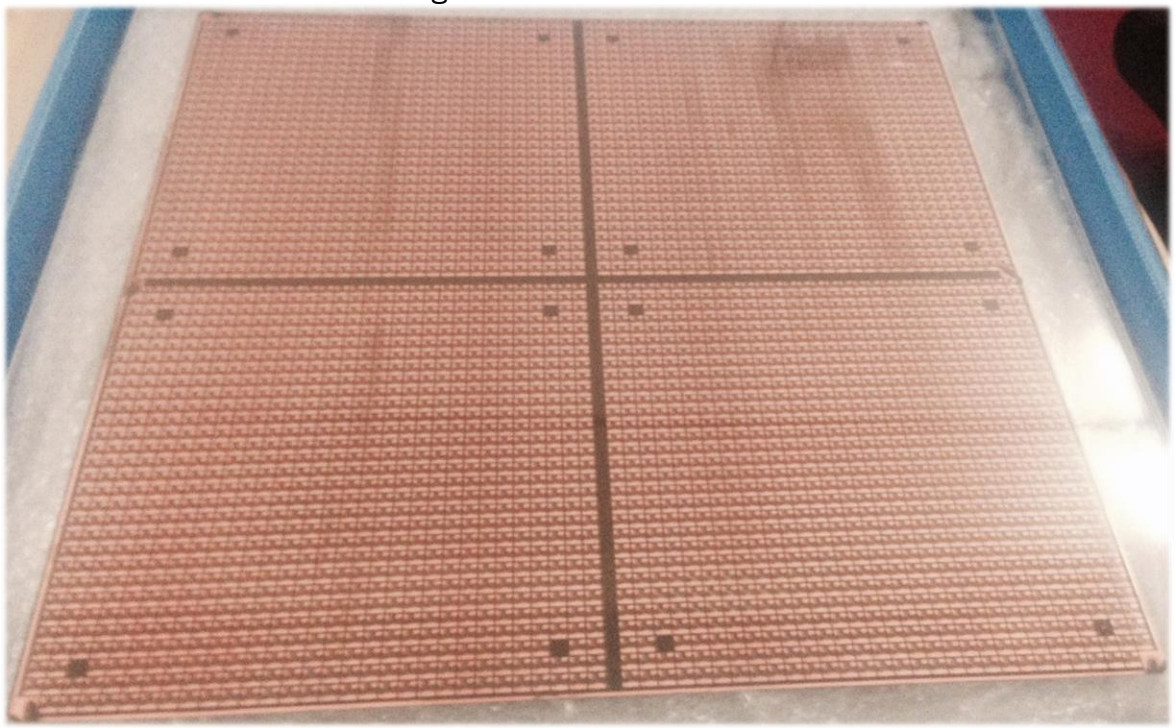
Initial production



Courtesy of Deca

300mm round

Large Panel Future Production

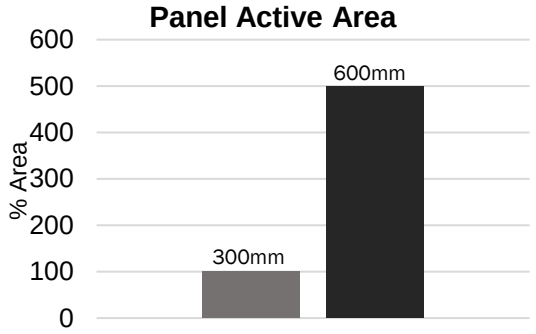


Courtesy of Deca

600mm x 600mm

600mm delivers

- *500% increase in usable area*
- *> 25% estimated cost reduction*



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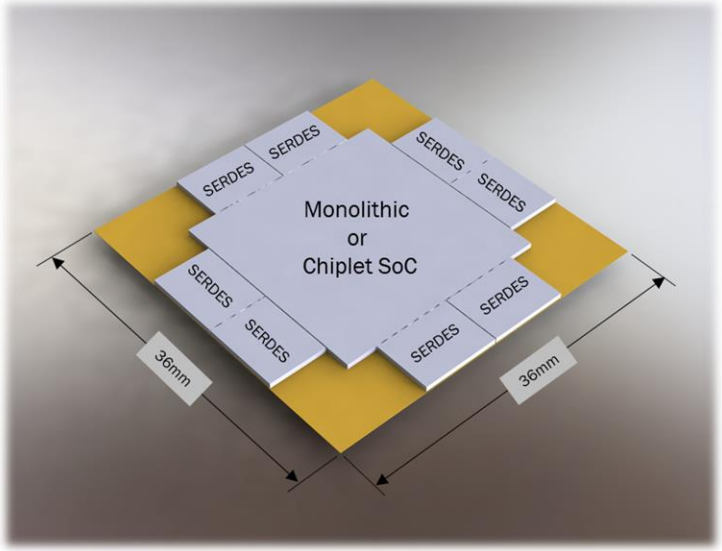
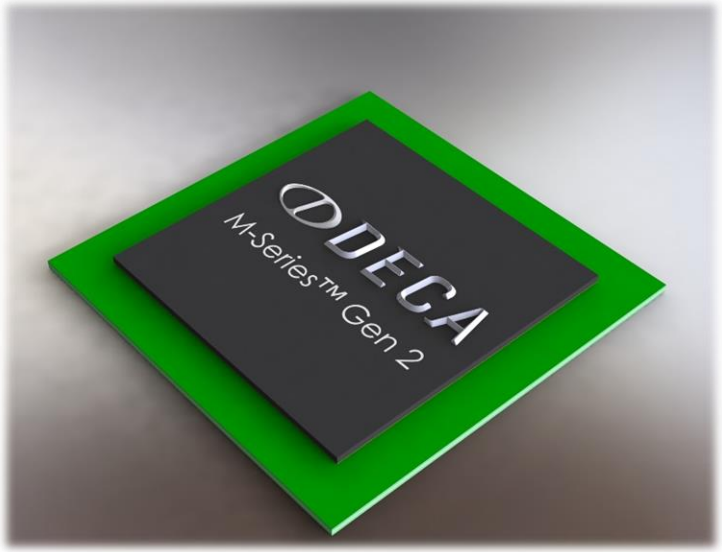
Background – Example Chiplet Device

- 9-die customer test vehicle device
- 36mm x 36mm package size
- 2µm line & space with 11,500 routes between chiplets



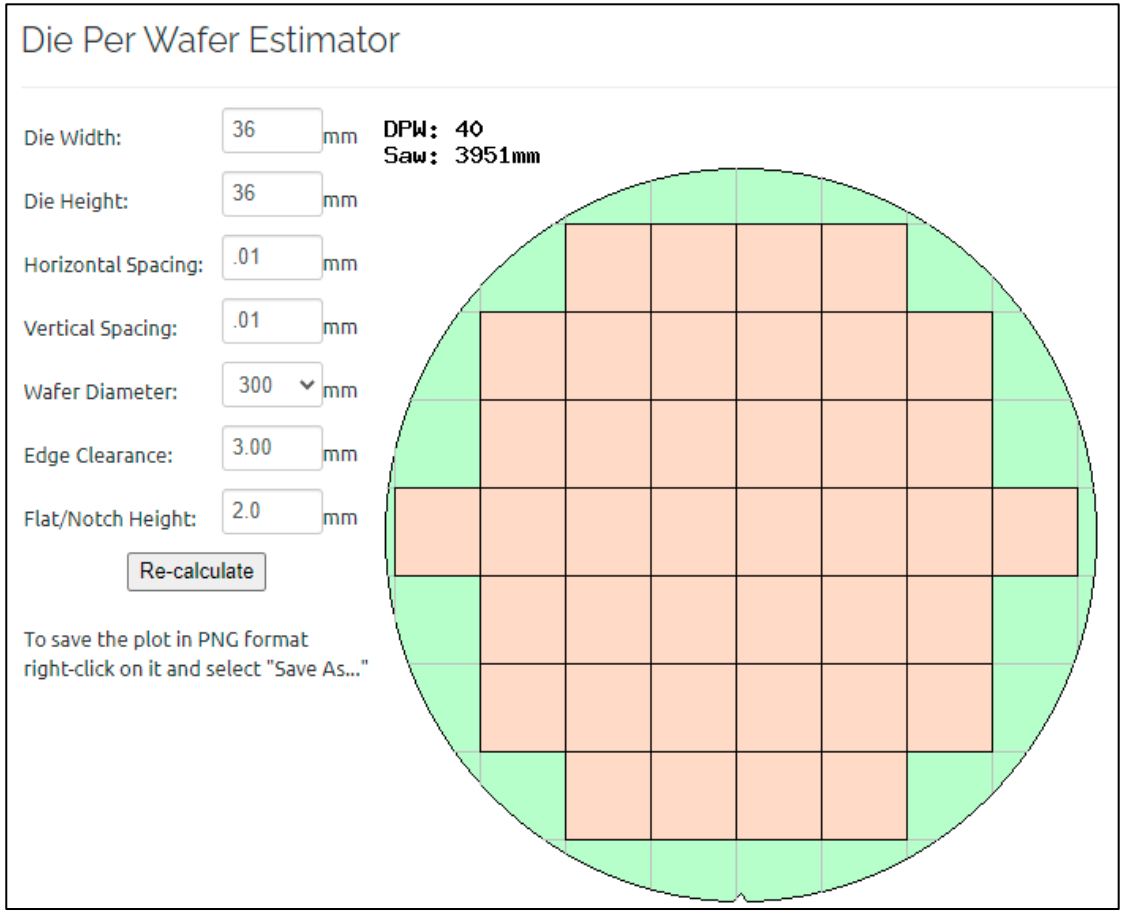
Chiplet-based fan-out device (9-die)

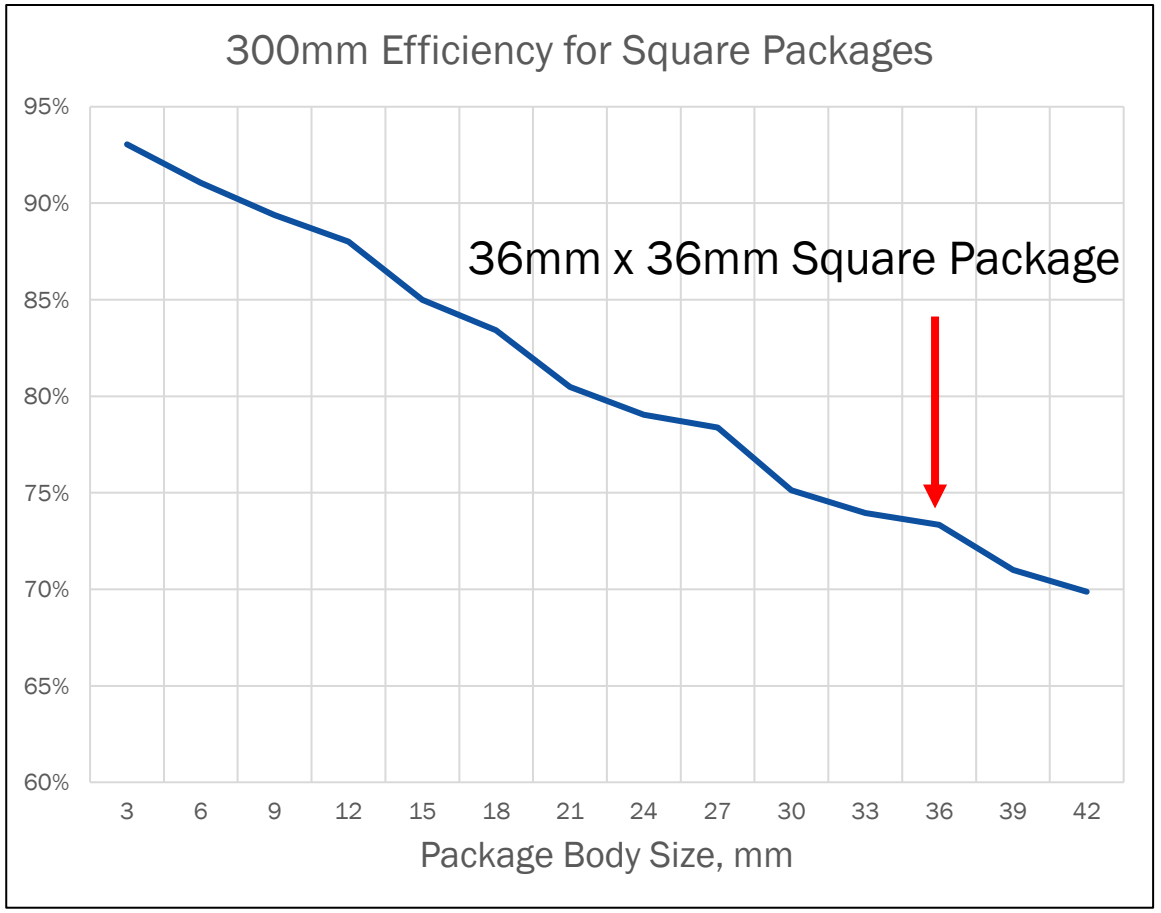
Molded 9-die structure
(with Cu pillar bumps)



Flip Chip mounted on
substrate

Background – Example Chiplet Device

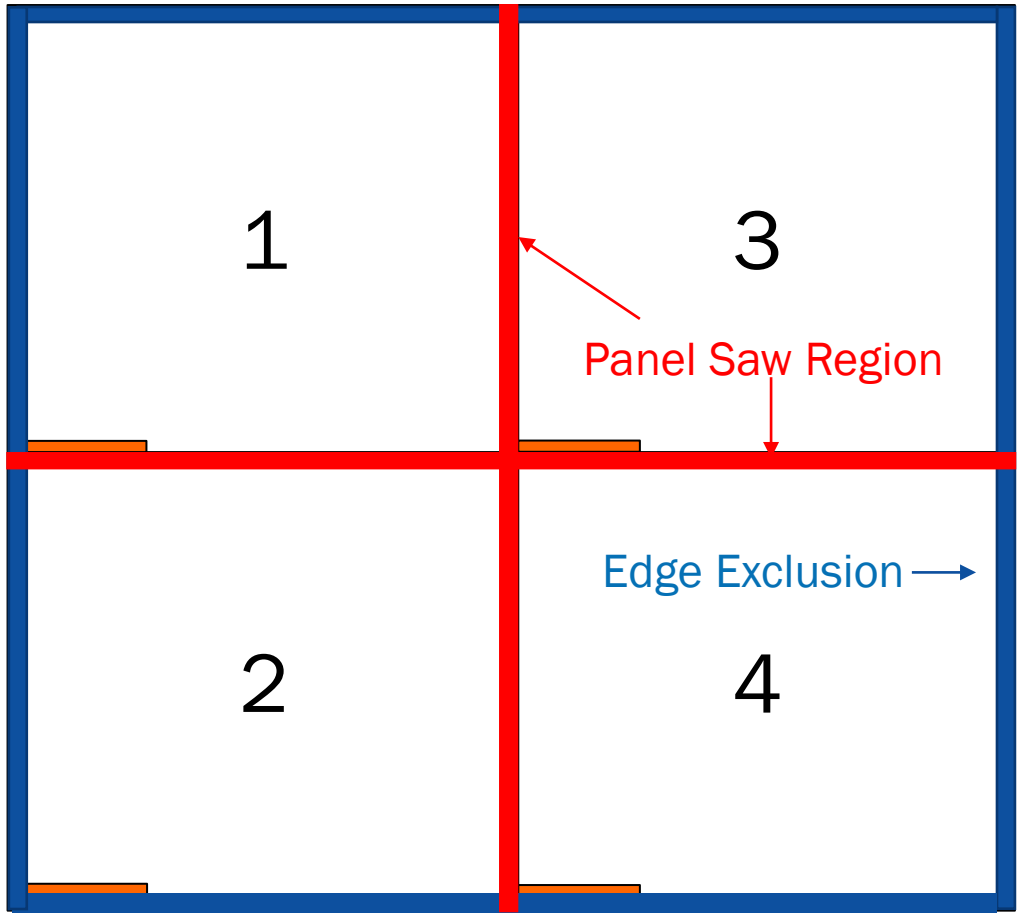


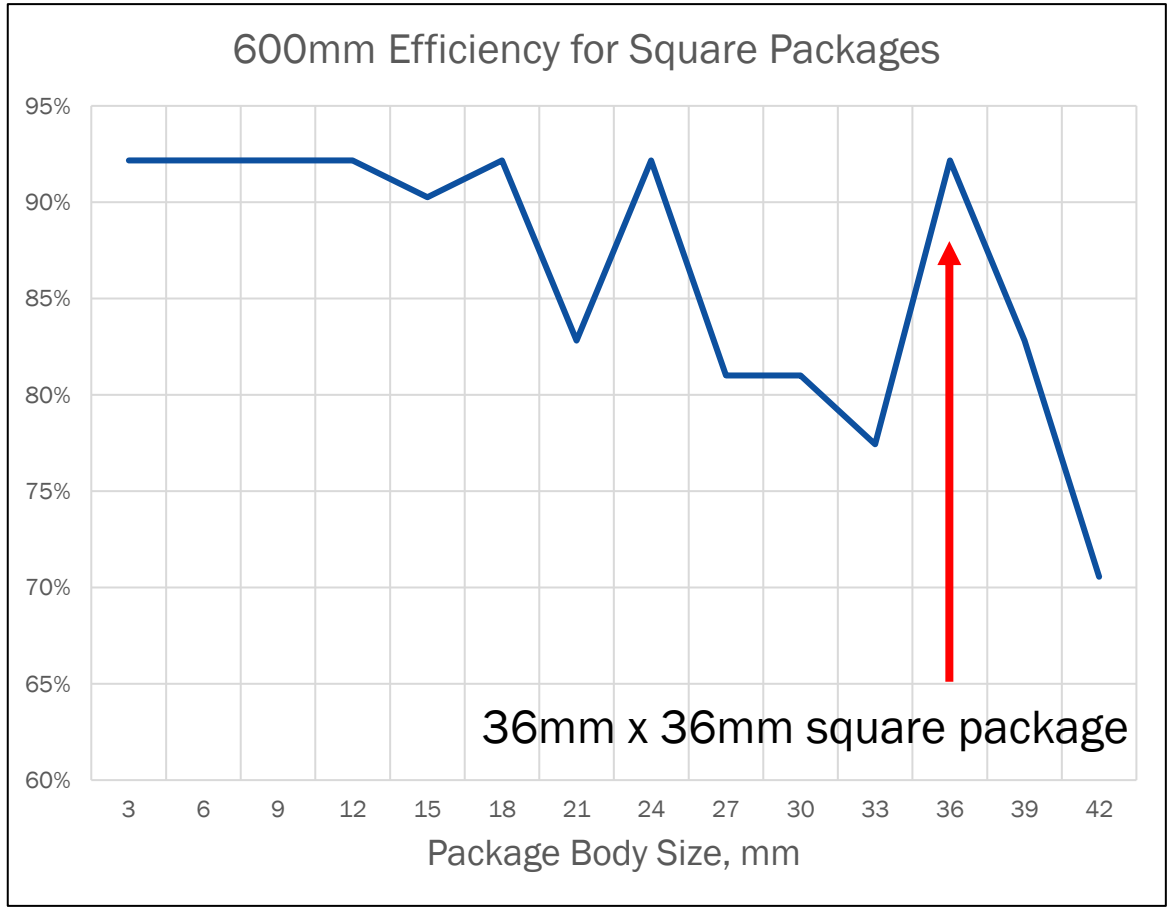


http://www.silicon-edge.co.uk/j/index.php/resources/die-per-wafer

- Format efficiency of 300mm = total package area divided by format area, assumed square packages
- 300mm = 73.3% for a 36mm x 36mm square package or 40 die per wafer (DPW)

Background – Example Chiplet Device





- Format efficiency of 600mm = total package area divided by format area, assumed square packages
- 600mm = 92% for a 36mm x 36mm square package or 256 die per panel (6.4x)
- Placement area per section is 290mm square (10mm panels saw region and 5mm edge exclusion)

Setting the 600mm Standard with M-Series

1. Background
2. Cost
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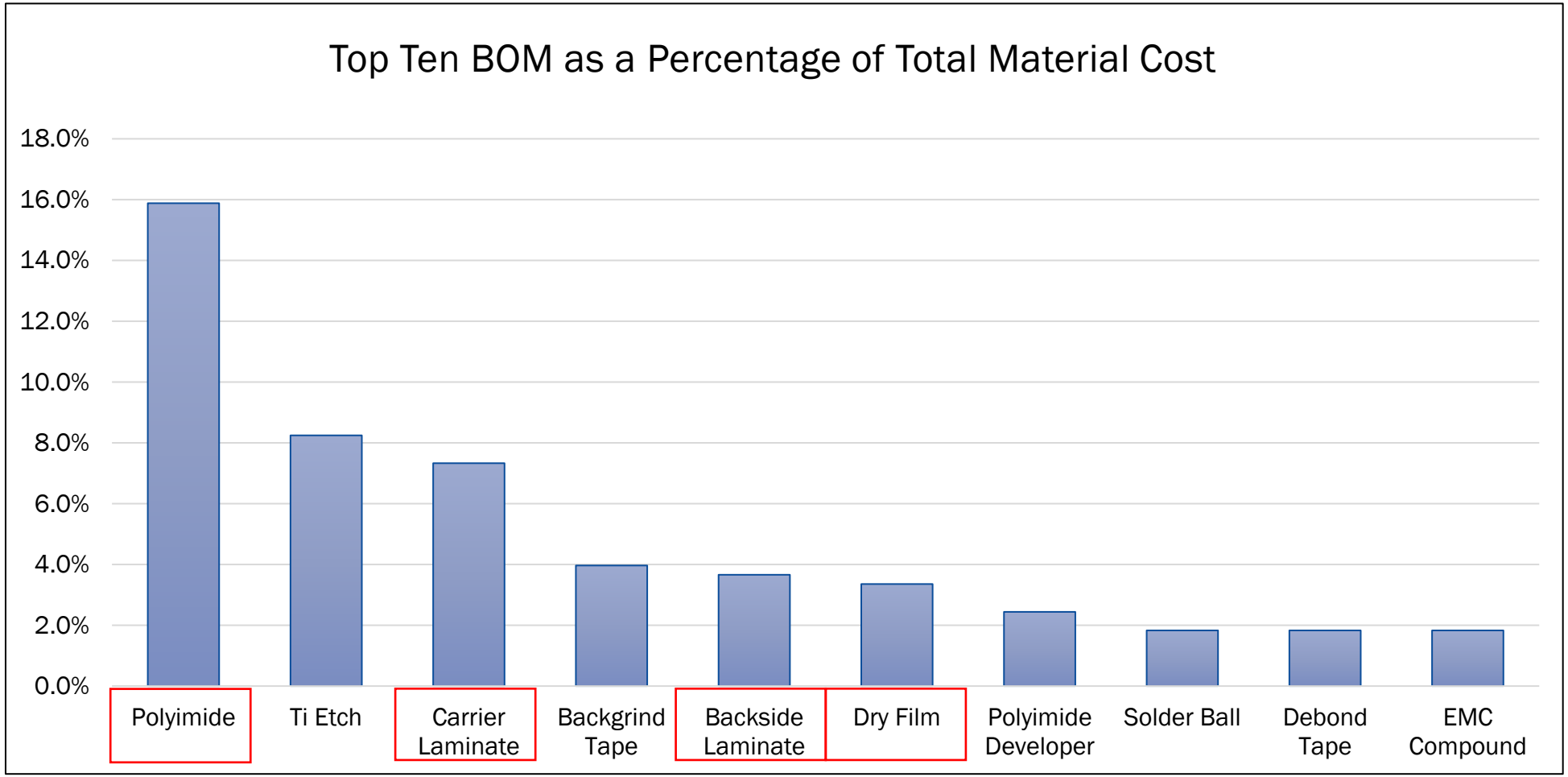
M-Series 300mm BOM Pareto

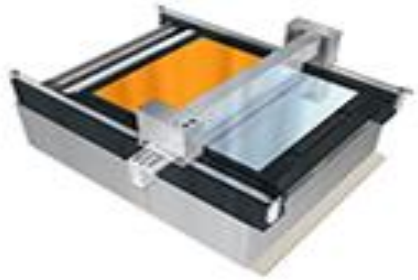


These ten materials represent 50% of the total BOM cost. Red boxes represent potential 600mm cost savings per square mm over 300mm

600mm Slot Coat Example

- Slot die coating using current polyimide with the following attributes:
  1. 600mm x 600mm format
  2. Polyimide diluted by 30% over current 300mm material
  3. Slot coated to 12µm thickness followed by a vacuum dry bake
- Was able to coat using 22ml of polyimide vs 8ml on 300mm format
- Uniformity across a 600mm panel <3% (see right)
- Example: for a standard high runner M-Series production fan-out part, there are 12,648 candidates on a 600mm panel and 2,567 candidates on 300mm (4.5mm square package)
- For 300mm, this is 0.00312ml per die and for 600mm 0.00174ml per die or 44% reduction in usage on a per die basis
- For our 36mm package, 256 die per panel at 22ml vs 40 die per wafer at 8ml,

  a 57% reduction (0.086ml per die vs 0.2ml per die)



Edge cut 10mm	Grid Measurement	
Max.	12.18	um
Min.	11.49	um
Range	0.69	um
Ave.	11.93	um
Uniformity	2.87	±%

Uniformity = (Range/(2XAve.))X100

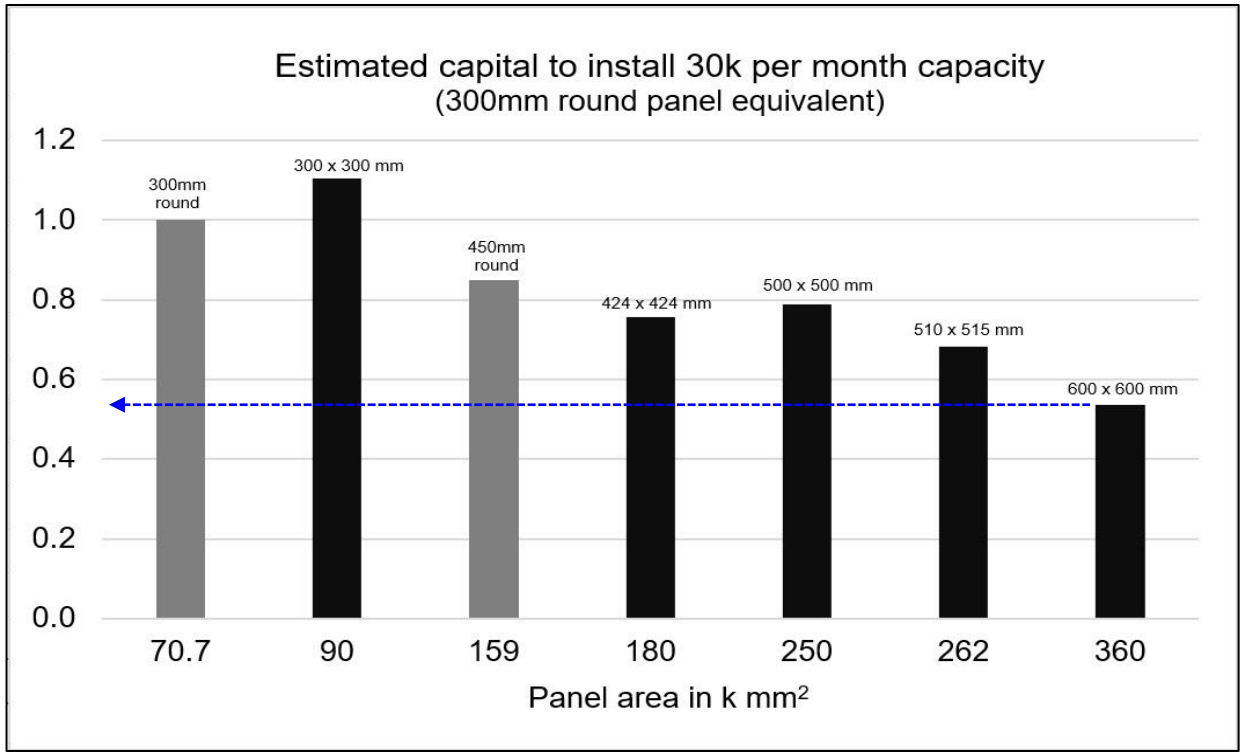
600mm Laminated Film Example

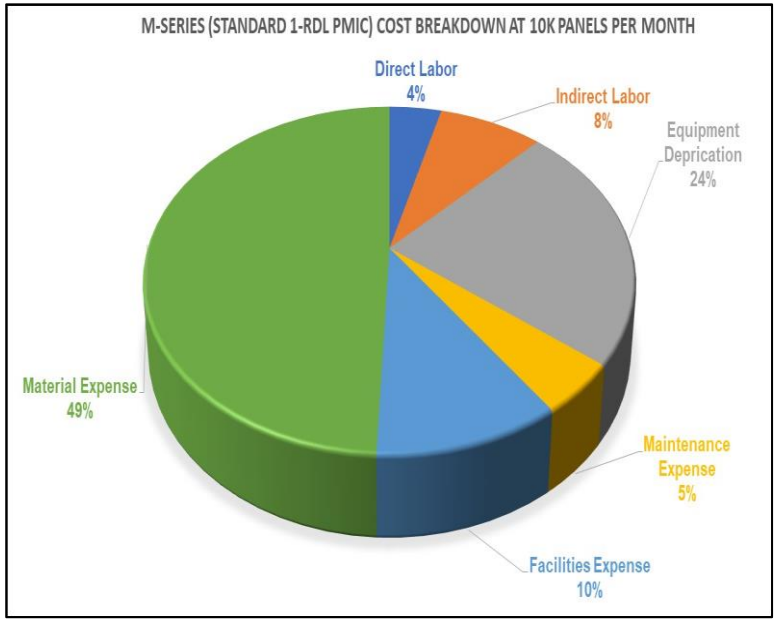
- Lamination rolls for 300mm in current fab are 320mm wide with a 20mm panel to panel dead zone
- Lamination rolls for 600mm are 620mm wide with the same 20mm panel to panel dead zone
- Films use in the M-Series flow include:

    1. Die attach tape
    2. Mold release tape
    3. Backside laminate used for warpage control
    4. Photoresist dry films for RDL and UBM (two or more)

- For our square 4.5mm package on 300mm, this is 39.9 square mm per die and for 600mm 30.4 square mm per die or 24% reduction in cost on a per die basis across five or more laminates due to wastage from using a round format
- For our square 36mm package on 300mm, this is 2560 square mm per die and for 600mm 1502 square mm per die or 41% reduction in cost on a per die basis

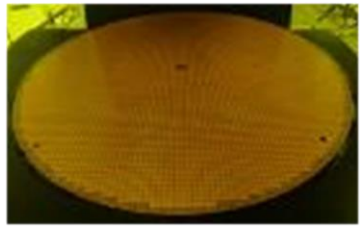
Cost – Capital & Materials



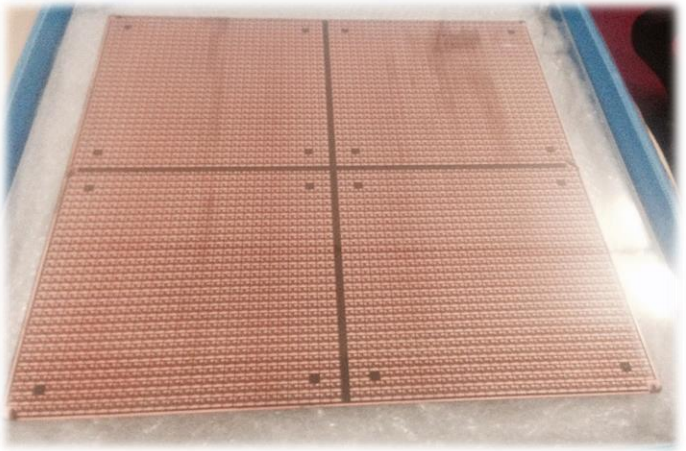


25% overall cost reduction with 600mm

- Capital productivity (> 40%)
- Material efficiency (> 20%)

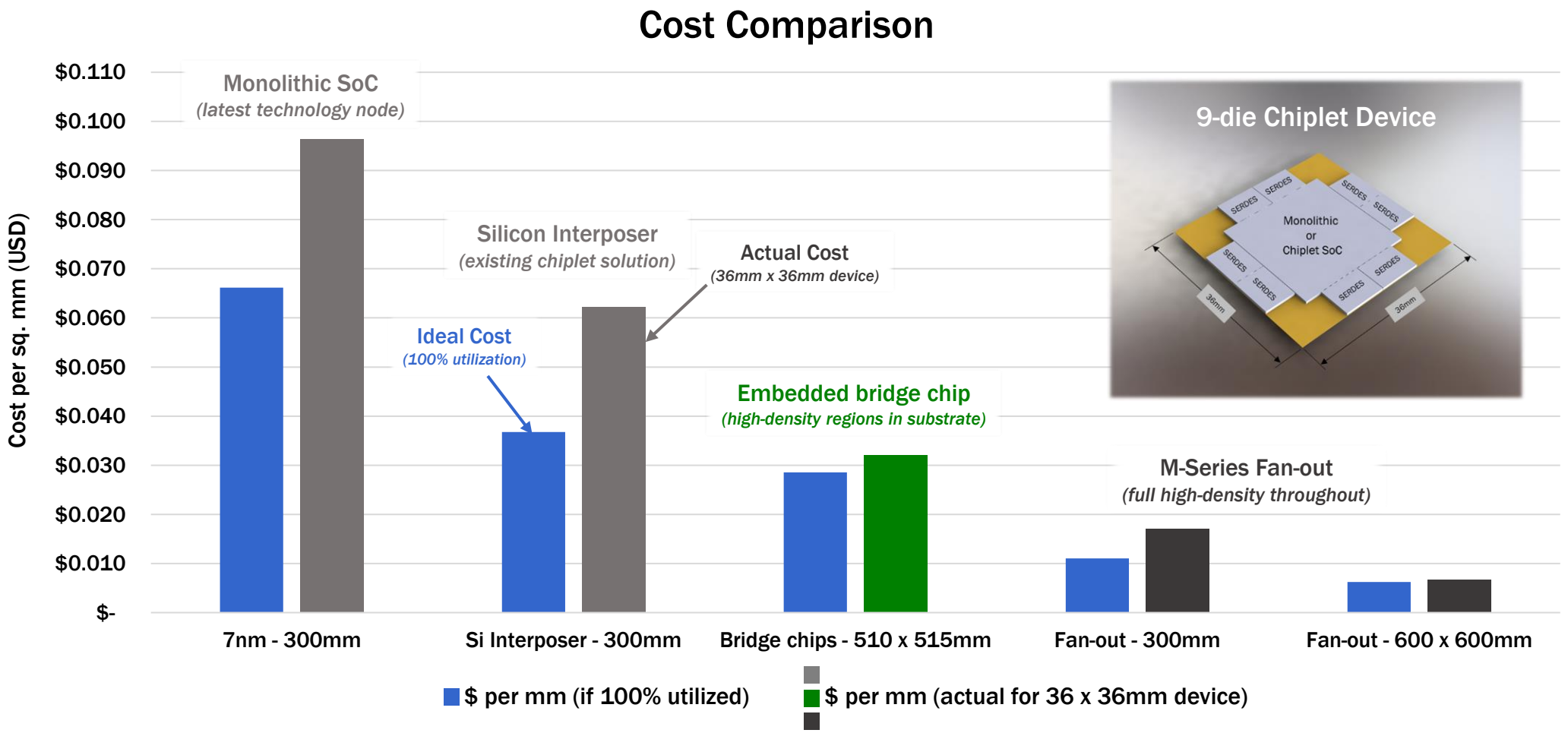


M-Series
300mm round



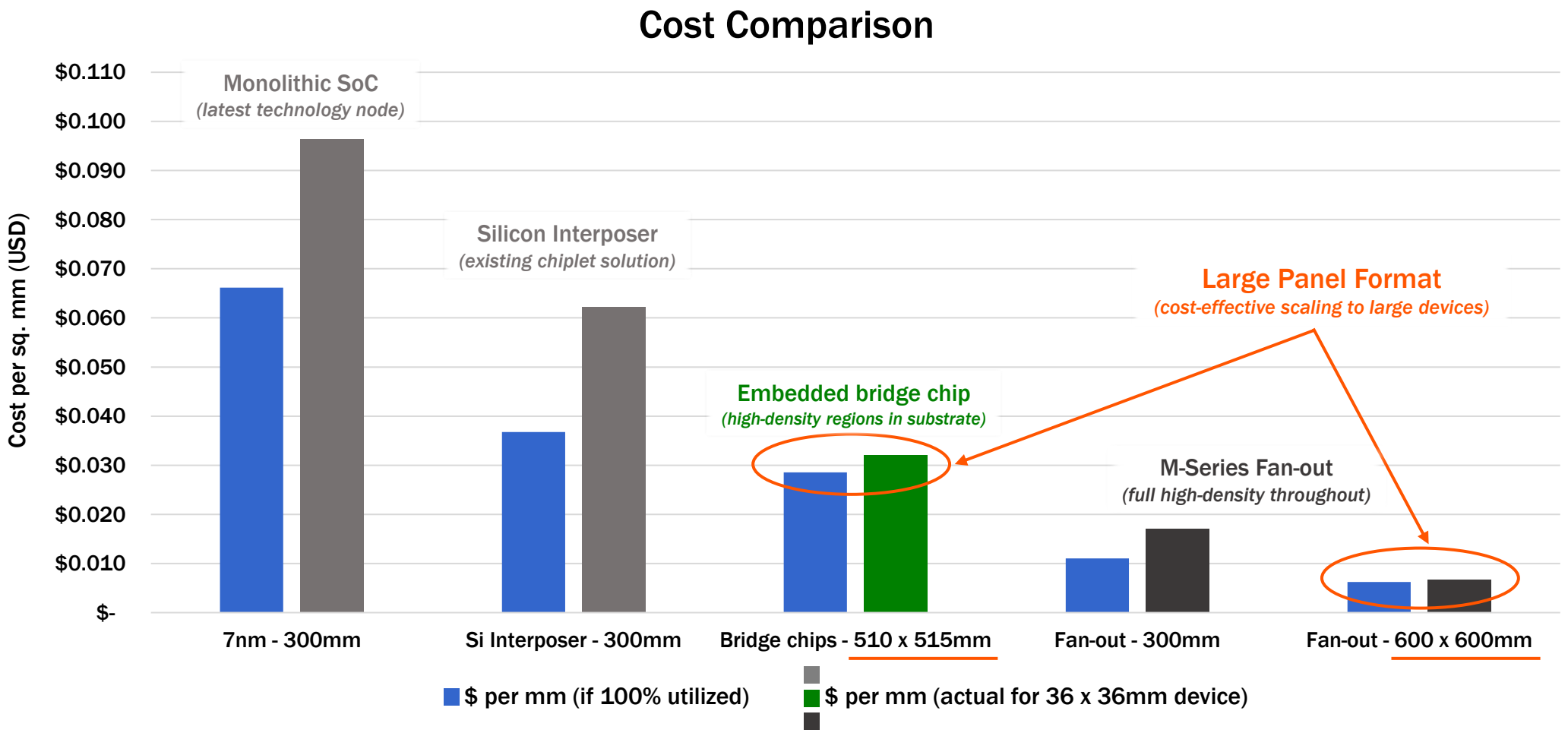
M-Series - 600mm square (500% area increase)

Cost – Normalized in $ per mm²

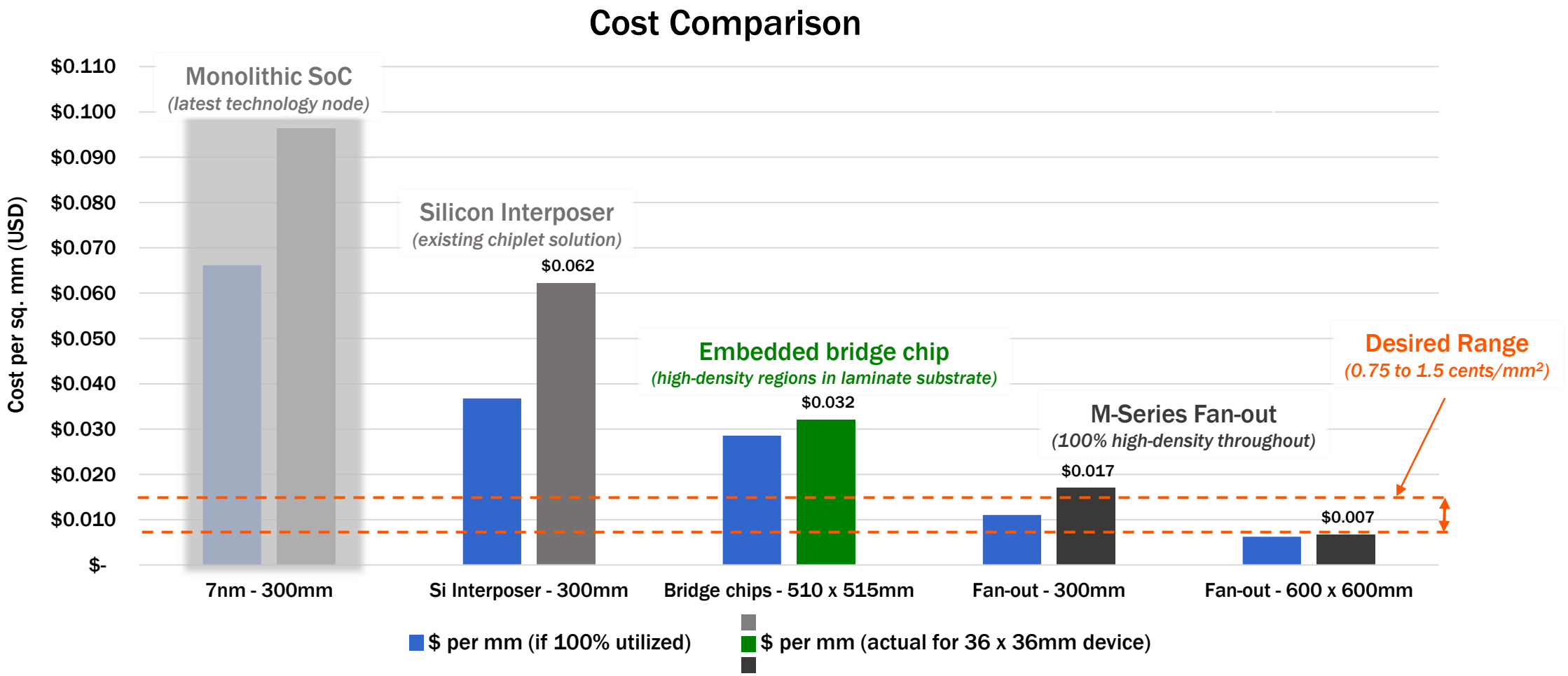


Sources: Yole Advanced Substrates 2018, Customer feedback, Deca estimates

Cost – Normalized in $ per mm²



Cost – Normalized in $ per mm²



One cent ($0.01) per mm² key target for mainstream (mass market) chiplet adoption

Setting the 600mm Standard with M-Series

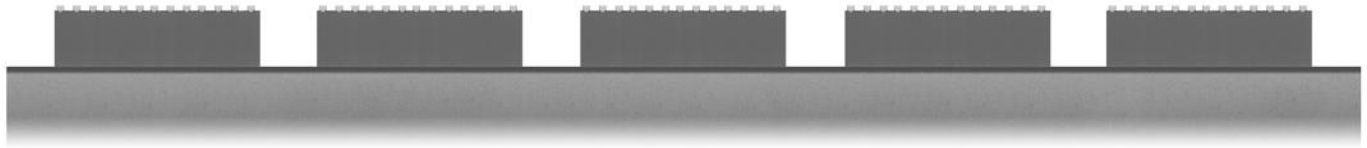
1. Background
2. Cost
3. Yield
4. Scaling
5. Conclusion

Yield Considerations

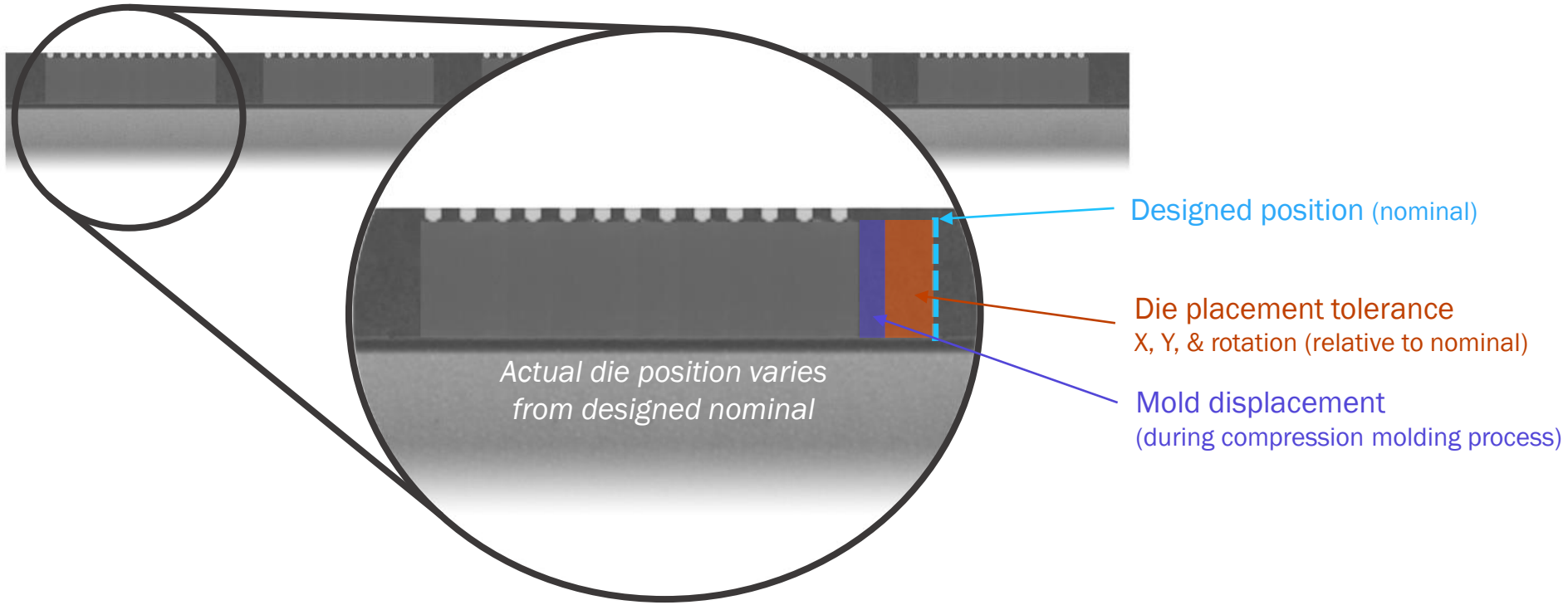
- Besides the processing tools, automation is crucial for large panel yield
- No standards exist, so invention is needed to standardize how carriers, handlers and tools interface…..currently designed around close carriers
- By sub-dividing into 300mm square segments, each segment is treated independently for yield so in terms of process risk is considered low
- The higher risk remains in terms of scrap or the loss of panels either from physical damage or mis-processing
- Therefore, tool automation and time to information (process to the next metrology step) are critical to reduce the material at risk. In-line inspections are key and should be re-evaluated base on die risk.
- Users making this format transition must weigh the added cost of next-generation equipment versus the risk of material in process and the volume necessary to support the benefits of cost

Yield - The Die Shift Problem (in embedded structures)

1. Die placement tolerance



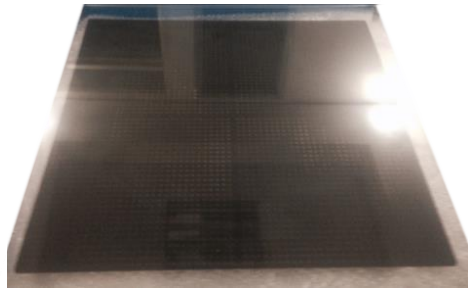
2. Displacement during encapsulation (molding)



Yield – Solving Die Shift with Adaptive Patterning™

1. Measure actual die positions using high-speed optical scanner

Planarized molded panel
(Cu studs exposed)



High speed precision optical scanner

Per die measurement

-101640	-94380	6.6	-19.6	0.00210
-101640	94380	1.8	-12.9	0.00293
0	0	-13.7	-4.3	0.00012
101640	-94380	-7.2	-7.9	0.00105
101640	94380	-5.5	6.2	0.00042
-137495	-21310	7.6	-7.1	-0.00039
-137495	-6790	-3.7	13.8	-0.00202
-137495	7730	-31.5	-5.8	-0.00658
-137495	22250	-4.9	-7.8	0.00351
-115715	-79390	-6	5.1	0.0000
-115715	-64870	-8.5	-12.8	0.00095

2. Generate unique lithography patterns for polyimide & photoresist layers during manufacturing (every device, every panel)

Actual die position measurements

-101640	-94380	6.6	-19.6	0.00210
-101640	94380	1.8	-12.9	0.00293
0	0	-13.7	-4.3	0.00012
101640	-94380	-7.2	-7.9	0.00105
101640	94380	-5.5	6.2	0.00042
-137495	-21310	7.6	-7.1	-0.00039
-137495	-6790	-3.7	13.8	-0.00202
-137495	7730	-31.5	-5.8	-0.00658
-137495	22250	-4.9	-7.8	0.00351
-115715	-79390	-6	5.1	0.0000
-115715	-64870	-8.5	-12.8	0.00095

Real-time design

ENGINE

The lithography pattern for the whole panel is dynamically generated real-time for each panel

Mask-less LDI lithography system

High throughput scan of panel

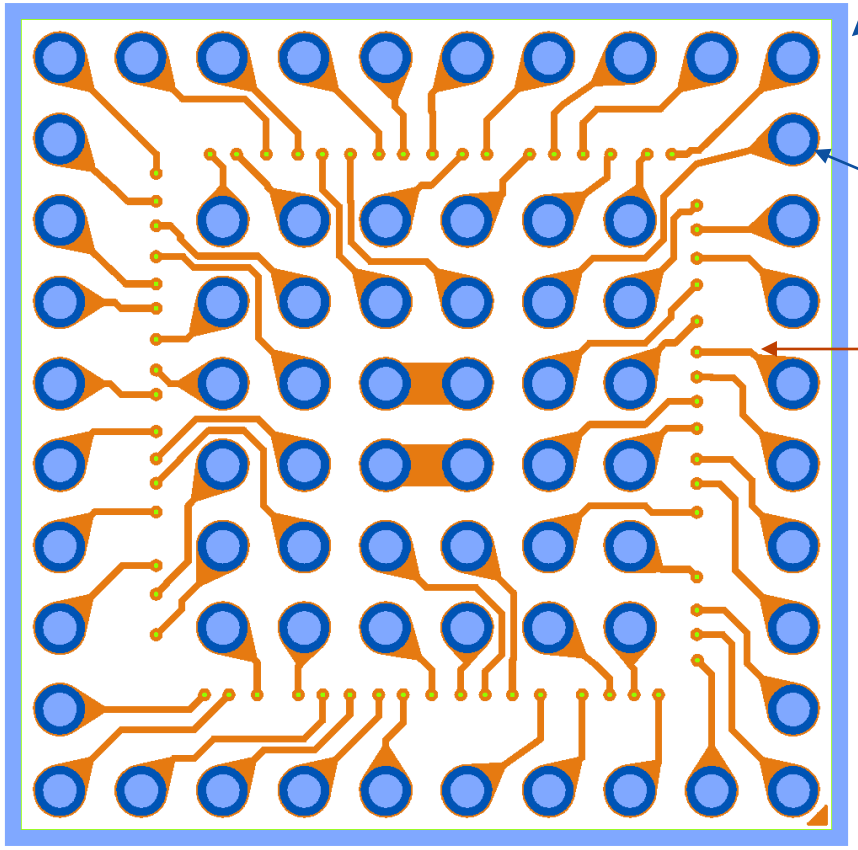
Unique lithography pattern per panel

Entire panel is one GDSII file
(no reticle size limitations)

Yield - Adaptive Patterning™ Methods

Adaptive Alignment

Align the entire RDL pattern to the measured die position



Enables high metal density designs
Precisely aligns inductors to the die

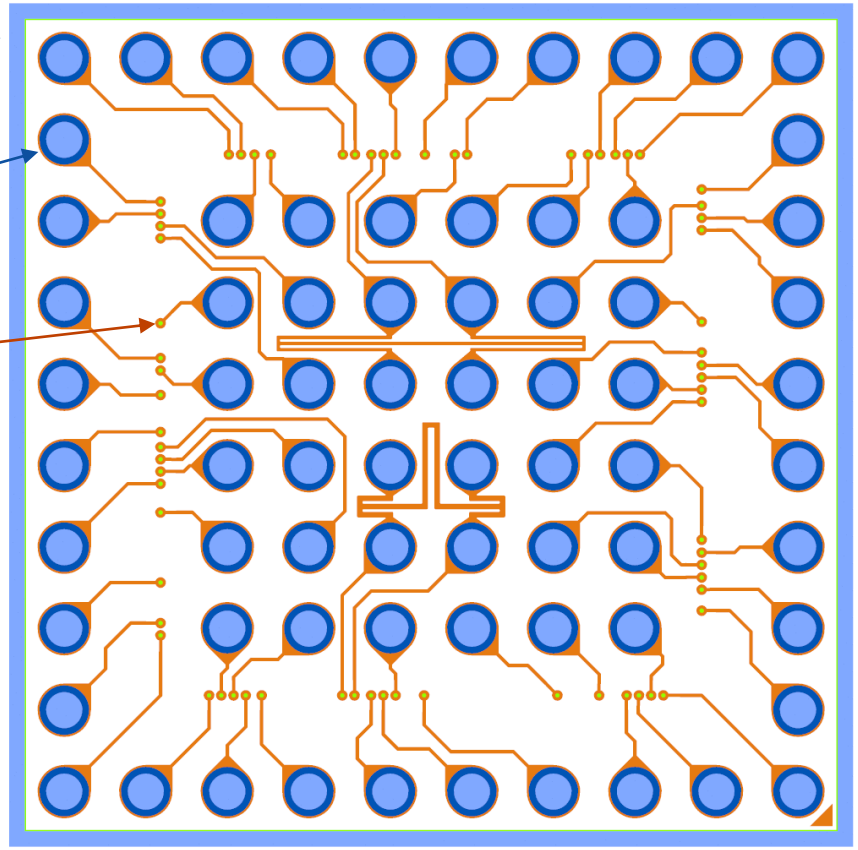
Fixed package outline

Fixed solder balls

RDL pattern moving per unit for precision alignment

Adaptive Routing

Dynamically adapt RDL routing to the measured die position



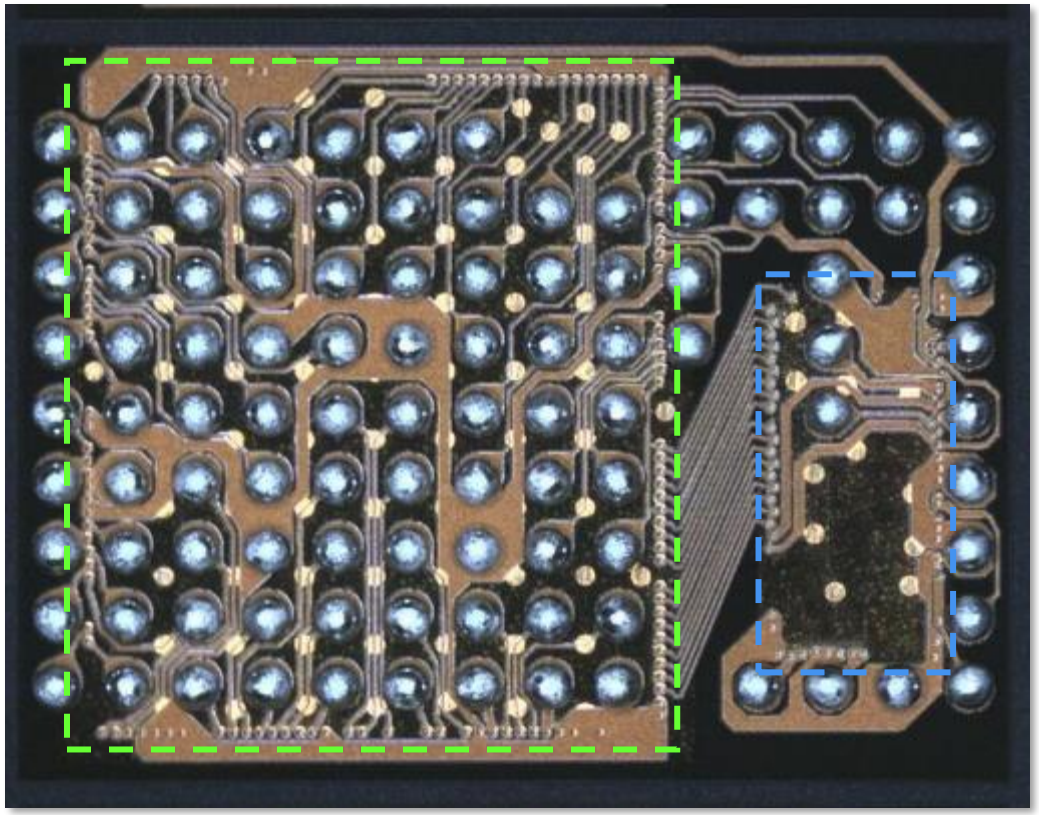
BGA array fixed to package outline
Enables multi-die fan-out

Note: Multiple patents issued & pending covering all facets of Adaptive Patterning

Yield - Multi-Mode Adaptive Patterning

IoT Application – Control & Communication

- Highly integrated MCU
- Bluetooth radio device



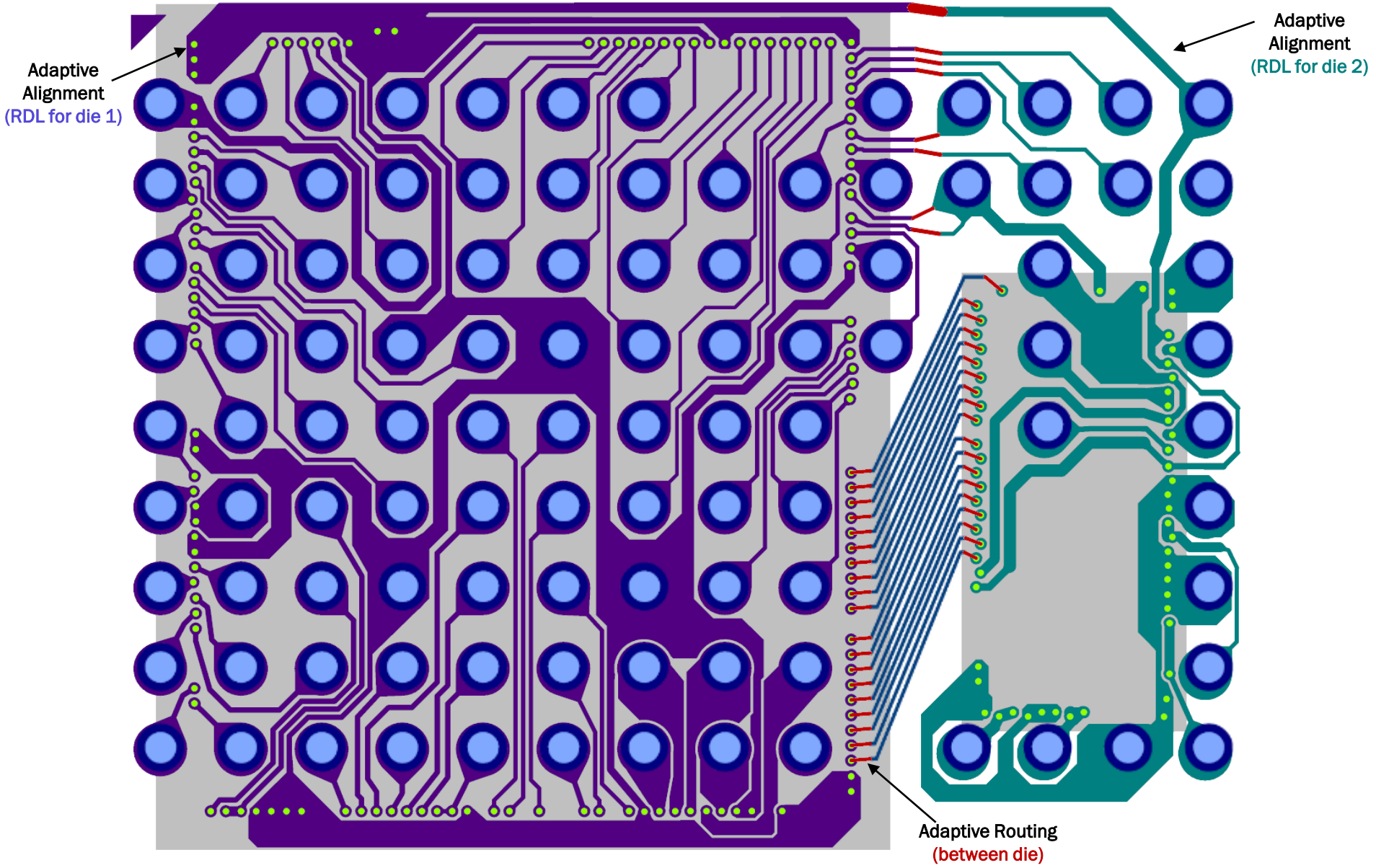
Package 5 x 3.8 mm

104 IO, 0.4mm pitch

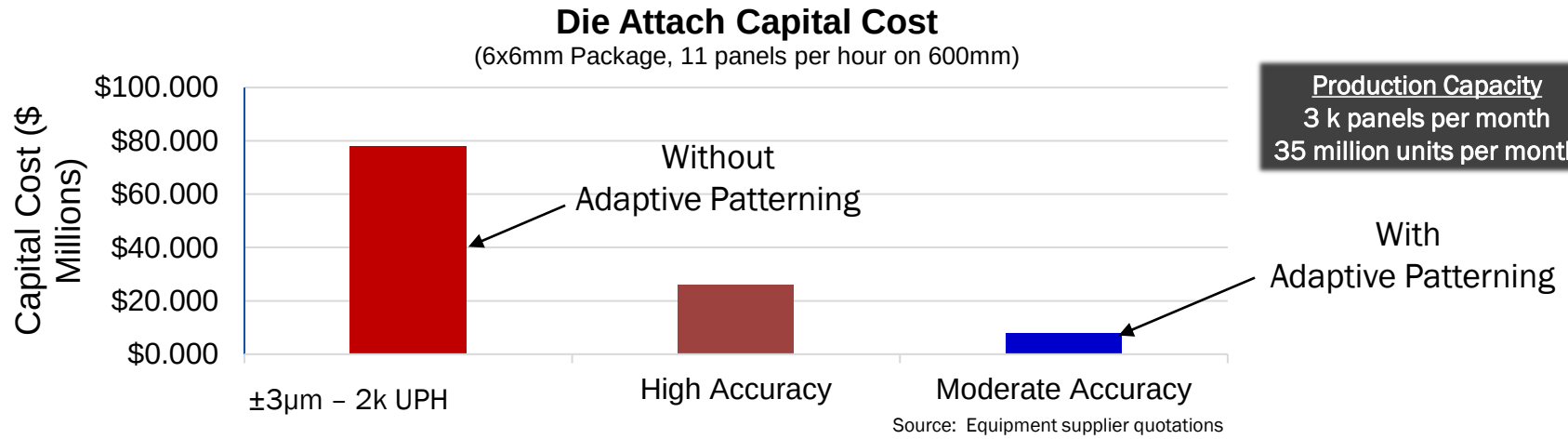
Die 1: 3.7 x 3.2 mm

Die 2: 1.0 x 2.0 mm

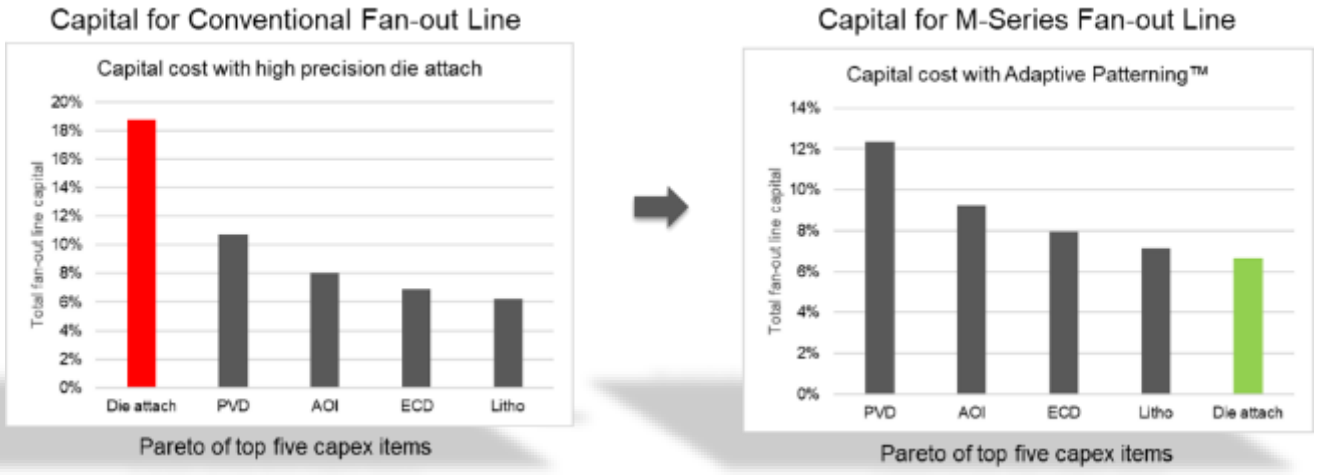
Yield - Multi-Mode Adaptive Patterning



Yield – Achieved Cost-Effectively



Source: Equipment supplier quotations



Chip Attach Equipment Options

Very high accuracy	± 3µm @ 3σ	$1.1M	2,000 CPH
High accuracy	± 8µm @ 3σ	$0.9M	5,000 CPH
Moderate accuracy	± 15µm @ 3σ	$1.3M	22,000 CPH

Adaptive Patterning enables an effective ± 3µm @ 3σ performance using the 22,000 CPH machine

Source: Deca calculations

10X reduction in highest capex process with Adaptive Patterning

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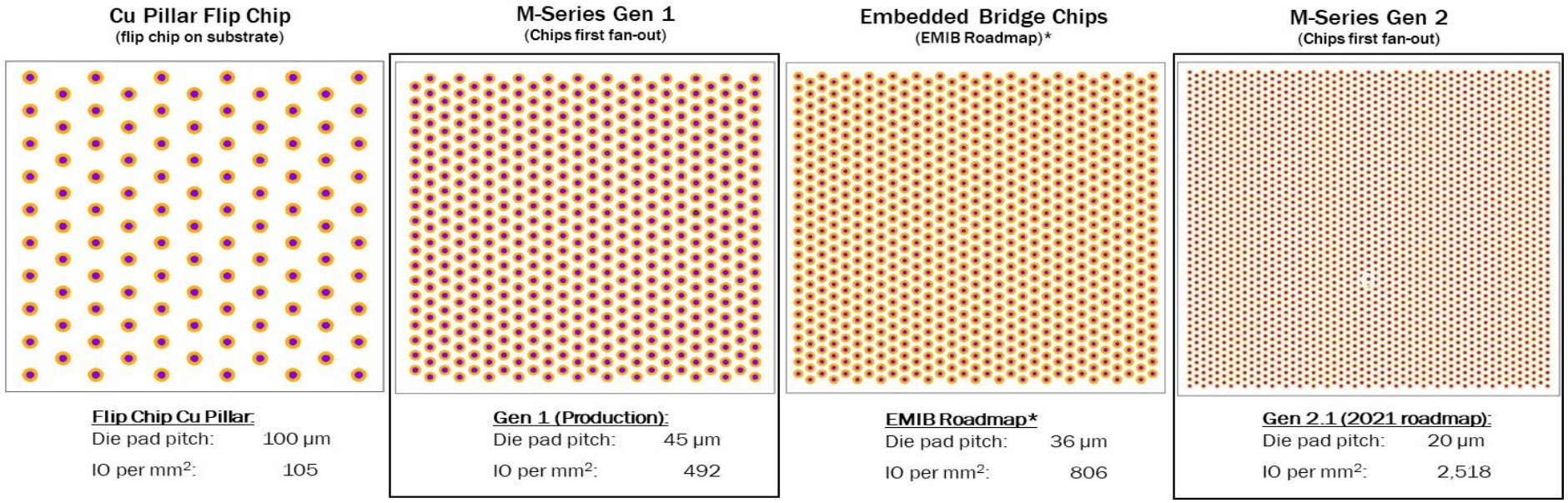
Scaling

- In addition to the physical RDL lines, increasing via density is critical for achieving high density for heterogeneous integration and chiplets
- Below provides an overview of current limits for via density by technology of well-known Cu pillar flip-chip on laminate and Intel's EMIB (embedded interconnect bridge) technology vs. existing both Gen 1 and Gen 2 M-Series.



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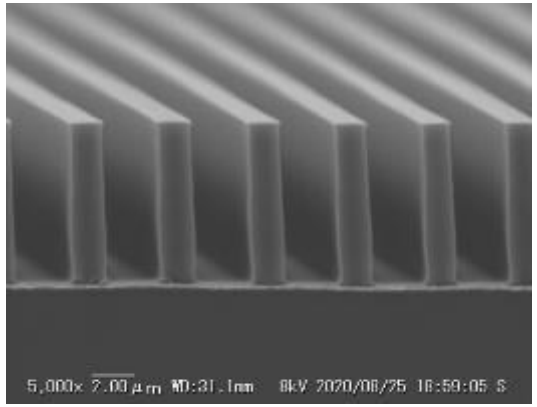
*https://www.anandtech.com/Show/Index/15980?cPage=2&all=False&sort=0&page=1&slug=intel-next-gen-10-micron-stacking-going-3d-beyond-foveros

Adaptive Patterning – Scaling to Ultra-high Density

- Gen 2 progress using maskless lithography
- Maskless provides the benefits of unlimited reticle size (ideal for chiplets)
- Adtec's alpha tool (Demo machine) in Nagaoka factory
- Production machine scheduled for later this year

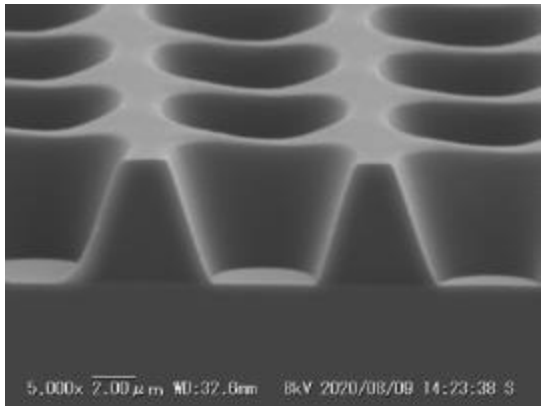
Alpha tool

TOK PR



Line and Space=2um
Liquid resist, positive tone thickness 7μm

Toray PI

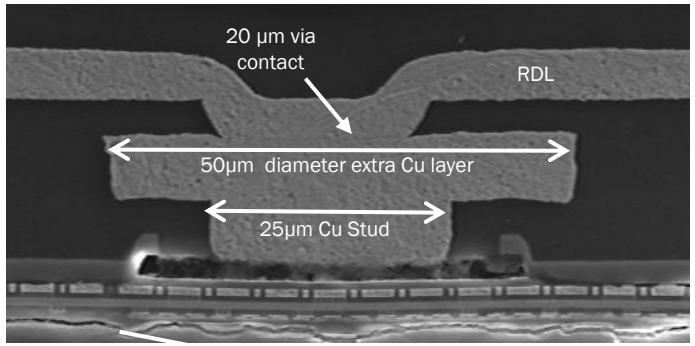


5um via, 10um pitch
Photo-sensitive polyimide positive tone, thickness 7μm

Inside tool

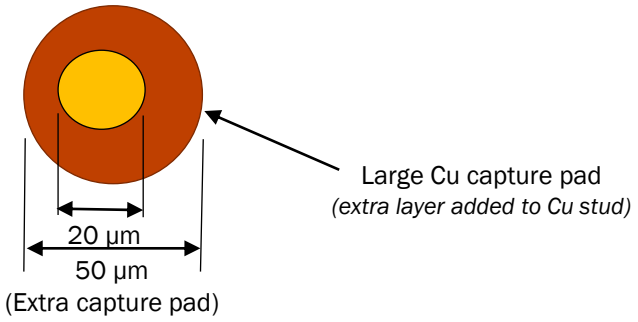
Adaptive Patterning – Scaling to Ultra-high Density

InFO™ without Adaptive Patterning (Latest Gen – iPhone 12)



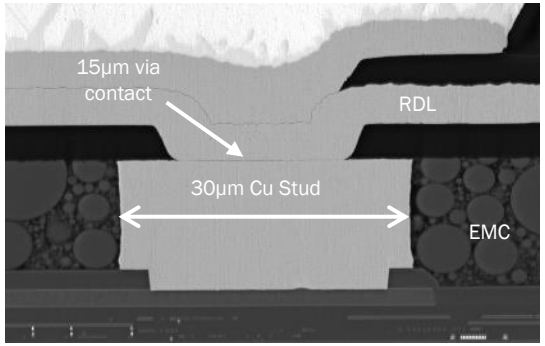
Source: Prismark – Apple A14 in iPhone 12

InFO via connection without Adaptive Patterning (Latest Gen – iPhone 12)



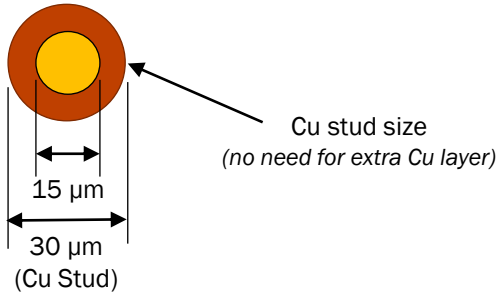
75µm capable Bond Pad Pitch

M-Series™ with Adaptive Patterning (Gen 1)



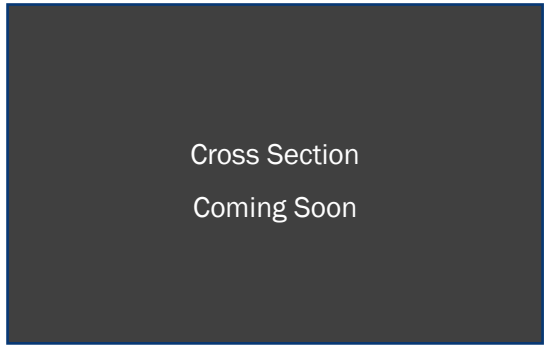
Source: Deca – Customer PMIC

M-Series via connection with Adaptive Patterning (Gen 1)

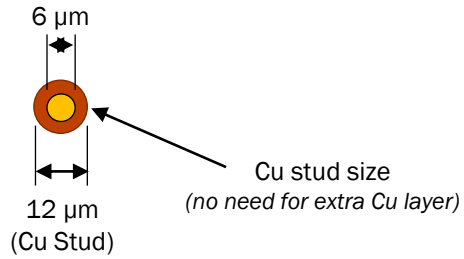


45µm capable Bond Pad Pitch

M-Series™ with Adaptive Patterning (Gen 2)



M-Series via connection with Adaptive Patterning (Gen 2)



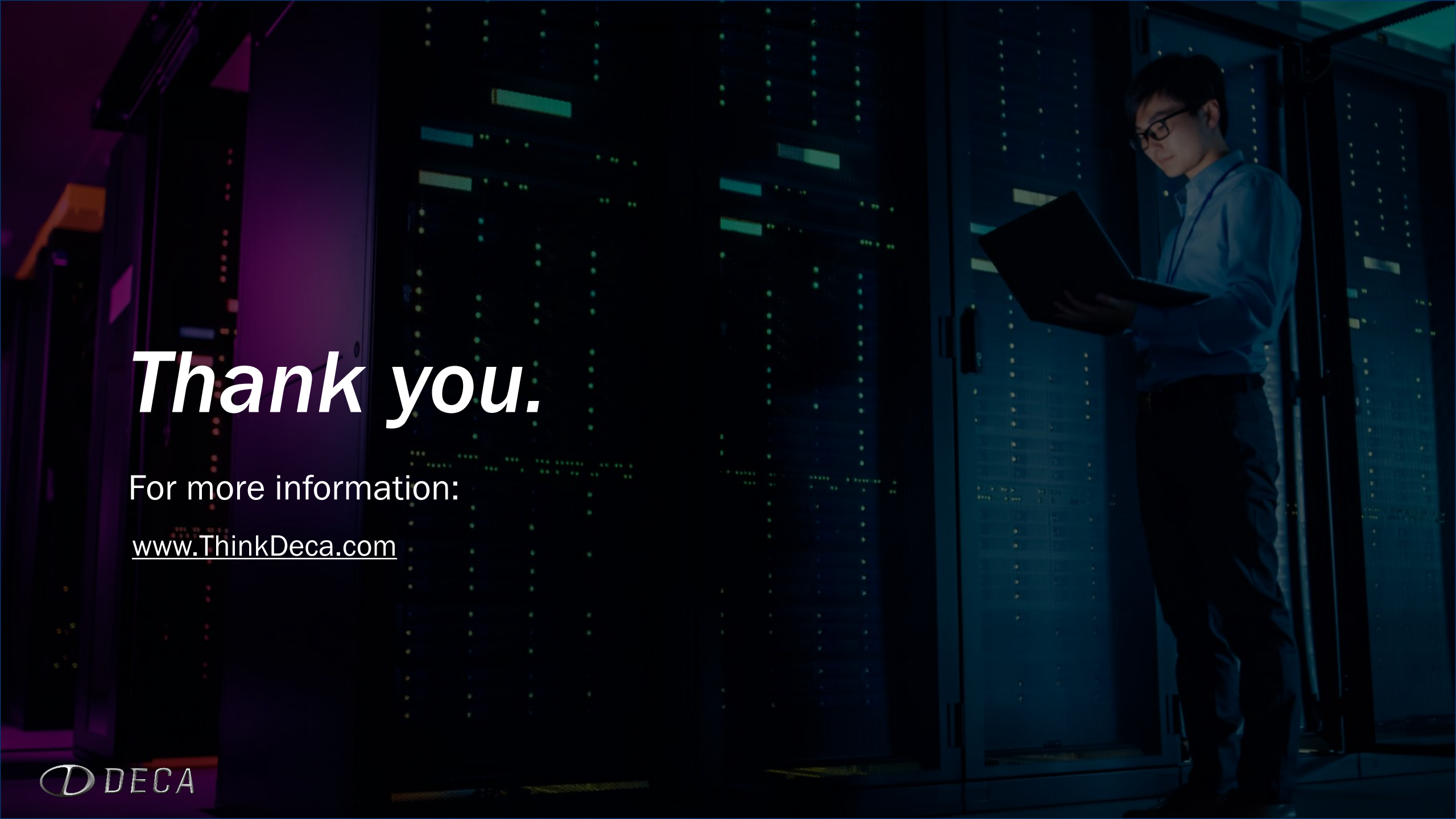
20µm capable Bond Pad Pitch

Setting the 600mm Standard with M-Series

1. Background
2. Cost
3. Yield
4. Scaling
5. Conclusion

Large Panel Possibilities … Conclusion

- Chiplets are close for mass market adoption
- Heterogenous integration advantages of integrating chips of different process nodes and functions to solve a scaling problem in the front-end, large monolithic chips are expensive
- Breaking through the barriers for cost-effective high-density integration is required
- Innovation in cost, yield & scalability on large panels provides a promising future for chiplets
- Efficiency of using a 300mm format fall below 75% for packages above for >30mm square
- Interconnect distances within a die using Adaptive Alignment and die to die using Adaptive Routing provides both cost and scaling advantages
- Challenges for large panels will be line yield and volume support, especially for new products



Thank you.

For more information:

www.ThinkDeca.com

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