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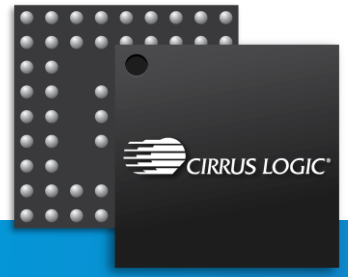
Effect of Silicon BEOL Presence on Solder Fatigue Life During Board-Level Thermal Cycling of WLCSP

IMAPS Device Packaging Conference 2021



Experts in Low-Power, Mixed-Signal Processing

Rameen Hadizadeh, Yaoyu Pang, Anuj Patel

Speaker

Rameen Hadizadeh received his M.S. degree in Mechanical Engineering from the Georgia Institute of Technology and B.S. degree in Mechanical Engineering from the University of Kentucky. He is the Manager of Packaging Development at Cirrus Logic and has previously held various technical positions with Texas Instruments, Qualcomm, and Wispry. Rameen has an extensive background in the wafer-level packaging field, including technology development, new product introduction and package characterization.

Yaoyu Pang received the M.S. and Ph.D. degrees in Engineering Mechanics from the University of Texas at Austin. He joined Cirrus Logic in 2017 as the Packaging Reliability Simulation Engineer and has previously held positions at Texas Instruments and Cisco Systems. He has authored and co-authored more than 20 peer reviewed papers in journals and conference proceedings and has 6 issued US patents on semiconductor packaging technologies. His professional experience mainly focuses on the reliability performance of integrated semiconductor structures, particularly in electronic material characterization, solder interconnects fatigue analysis, and advanced packaging technologies.

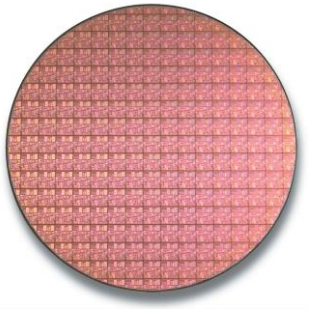
Anuj Patel received the M.S. degree in Electrical Engineering from the University of Wisconsin-Madison and B.S degree in Electrical Engineering from the University of Texas at Austin. He joined Cirrus Logic as a Product Reliability Engineer and has previously worked at Samsung. He has extensive experience in semiconductor reliability across multiple technology nodes and products in both digital and analog space. His current focus is in the area of product reliability failure characterization and acceleration modeling for both component level and board level reliability stress methodologies.

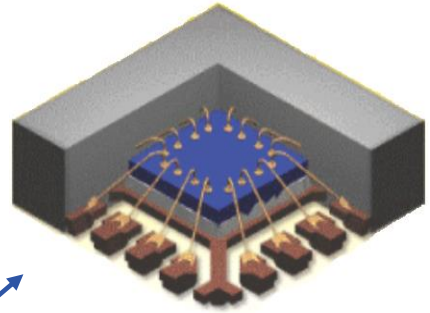
Presentation Guide

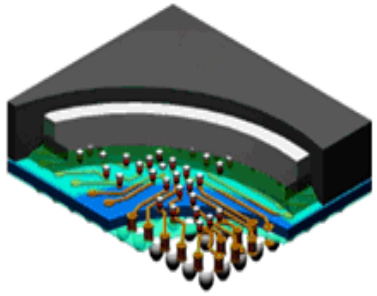
- Introduction
- WLCSP Test Vehicles
- Experimental Setup
- Modeling and Simulation
- Experimental Results
- Summary and Conclusions

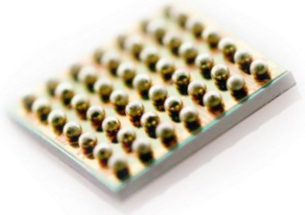
Introduction: Common IC Packaging Choices

IC devices on Silicon wafer









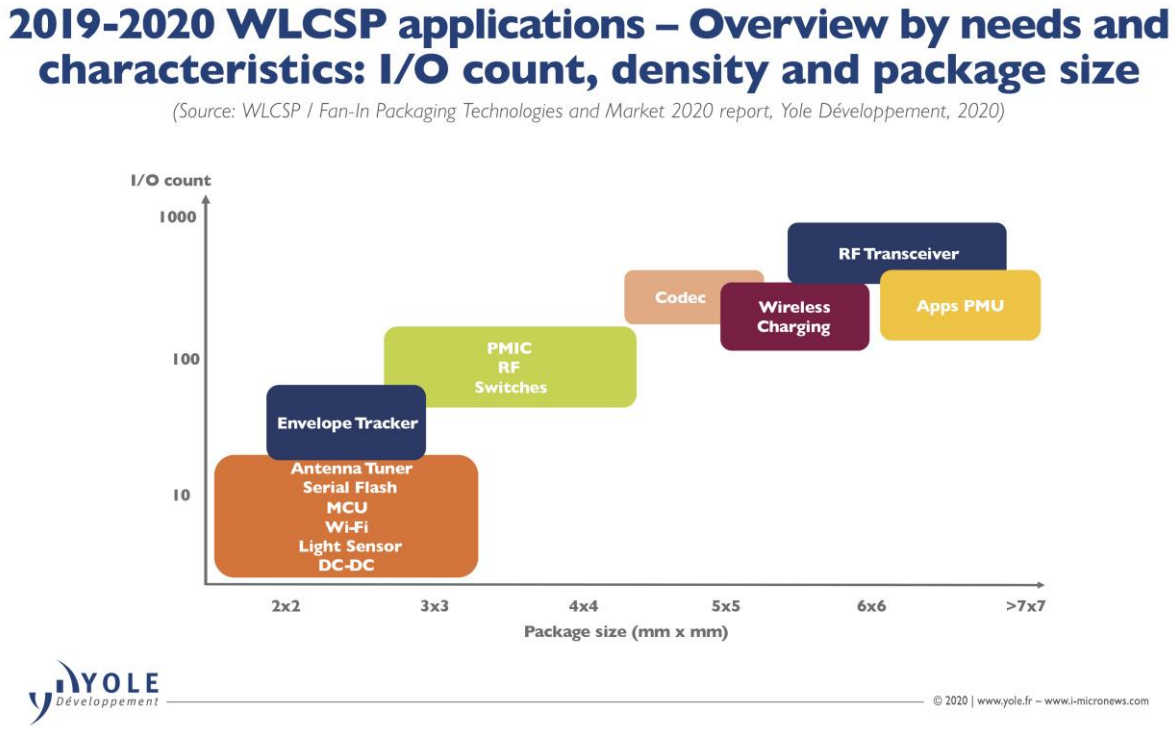
Quad-Flat No Leads (QFN)
- Attach backside of die to leadframe
- Wire-bond and over-mold
- **Pros**: robust, ubiquitous, thermally efficient, highly reliable
- **Cons**: size, high parasitic inductance

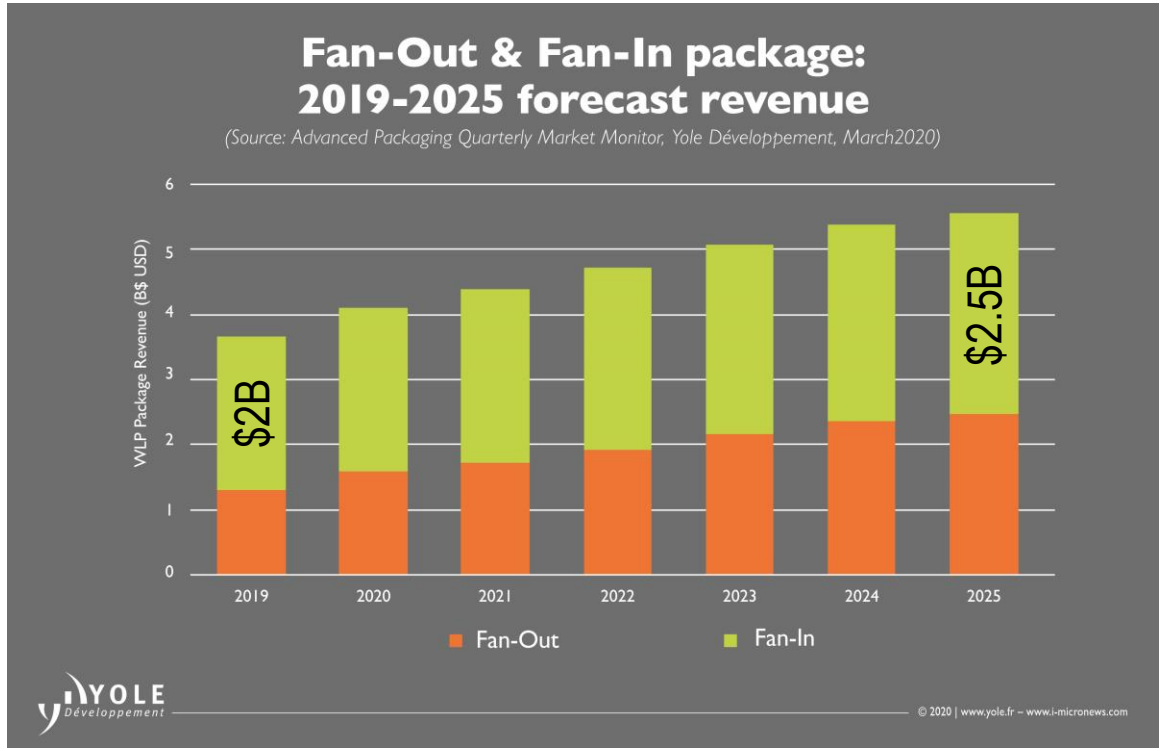
Flip-Chip Chip-Scale Package (FC-CSP)
- Wafer-level copper pillar process
- Attach active side of die directly to substrate, over-mold
- **Pros**: robust, low parasitics, reliable
- **Cons**: cost, complexity, supply chain

Wafer-Level Chip-Scale Package (WLCSP)
- Wafer-level RDL and ball drop process
- Singulated bumped die sold to customer
- **Pros**: small, low parasitics, cost
- **Cons**: fragile, thermally inefficient

Image sources
Wafer: Britannica
QFN: Advanced Interconnect Technologies Inc.
FC-CSP: ASE Korea
WLCSP: EEVBlog

Introduction: Wafer-Level Packaging Market





Introduction: Board-Level Integration Challenges

- Board-level reliability (BLR) qualification is intended to simulate the customer's system-level environment
- BLR is critical for wafer-level chip-scale packages (WLCSP) as body sizes continue to grow – particularly thermal cycling on PCB
- Global package attributes (die size, BGA pitch, solder alloy, etc.) influence solder joint integrity to a first order
- How do device attributes (e.g., foundry back-end-of-line) influence solder joint integrity during BLR?

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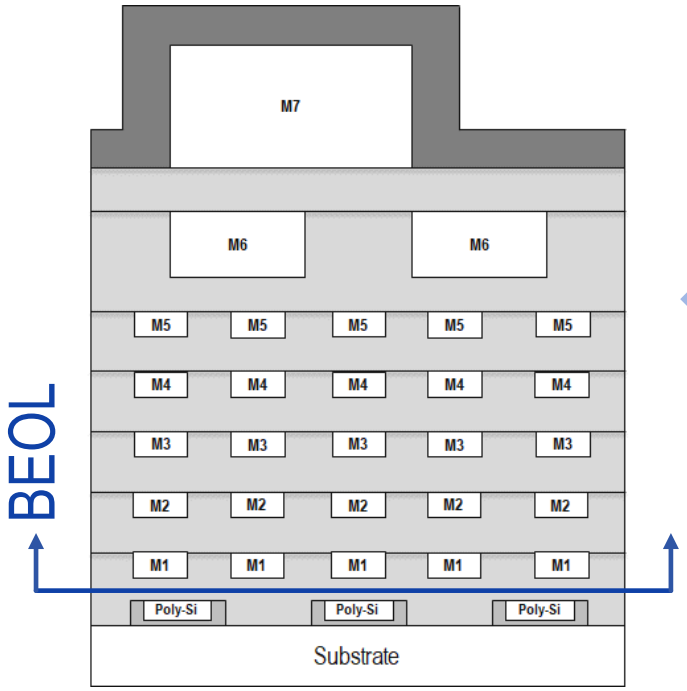
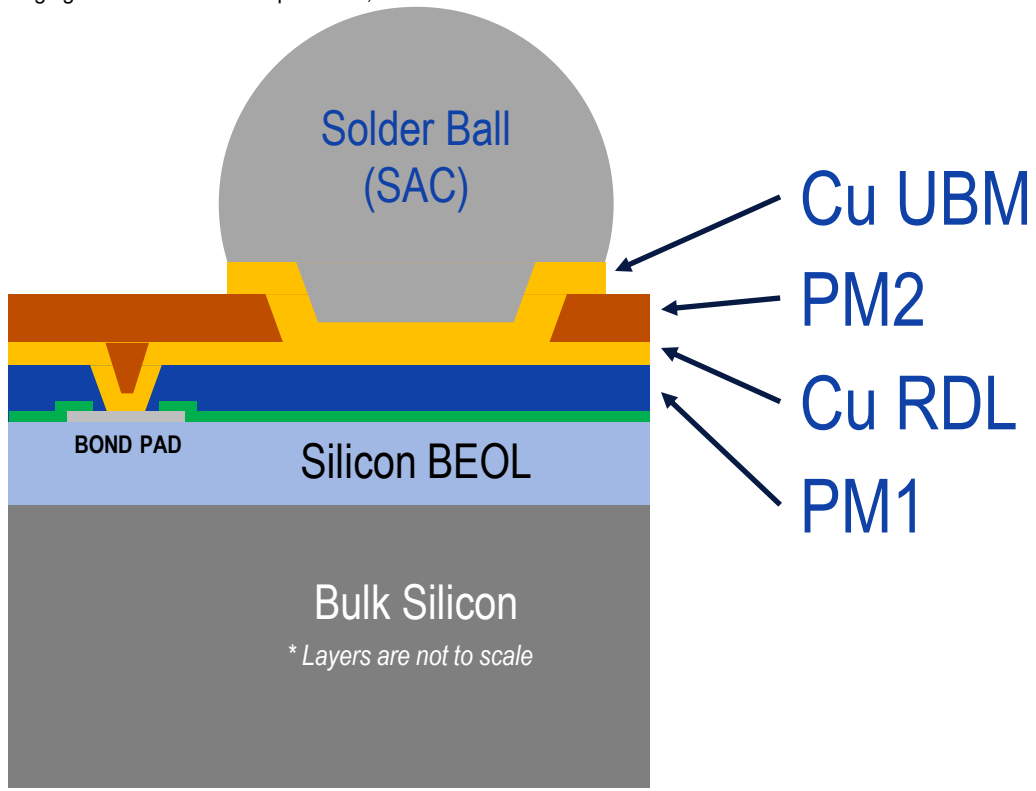
Test Vehicles: Overview



Foundry Stackup



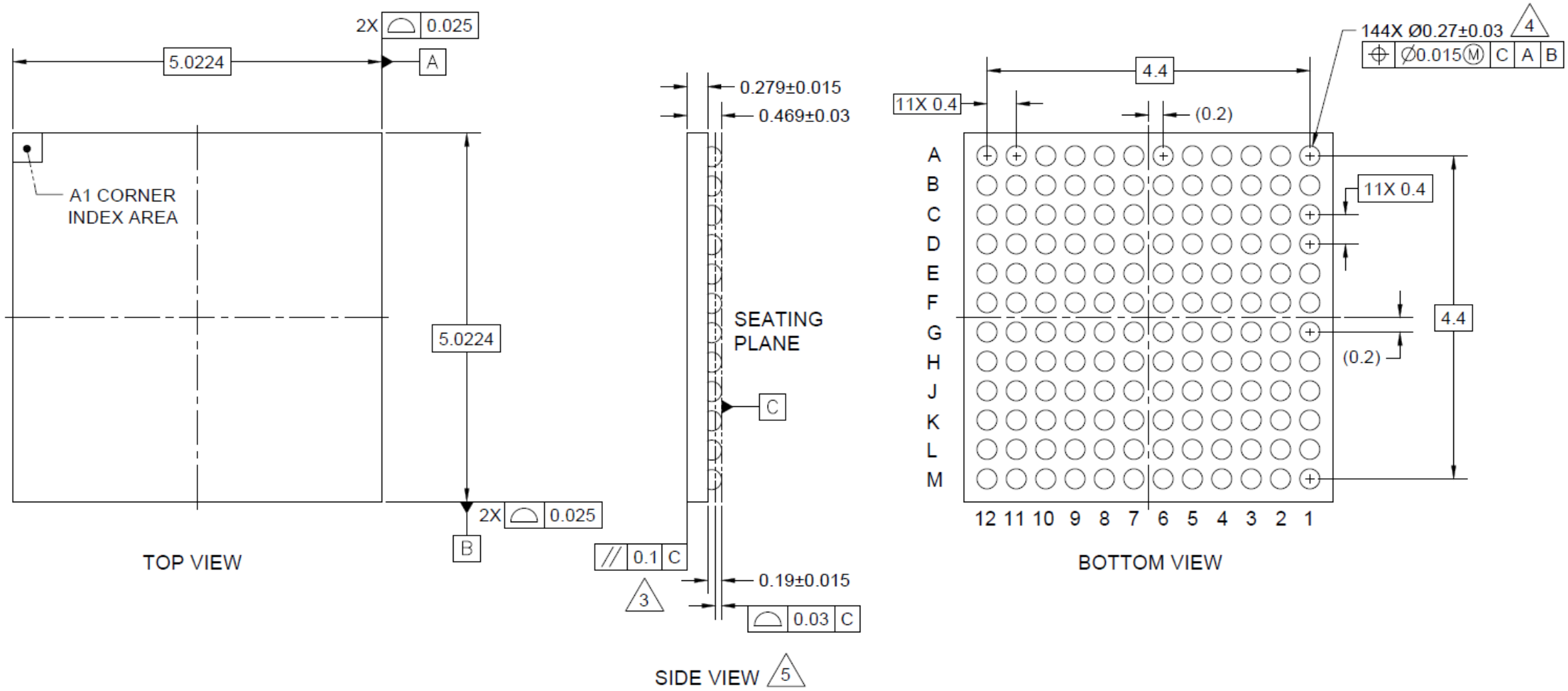
Primary Goals

- Explore effect of BEOL presence on solder fatigue life
- Determine if RDL density/routing has impact on solder fatigue life

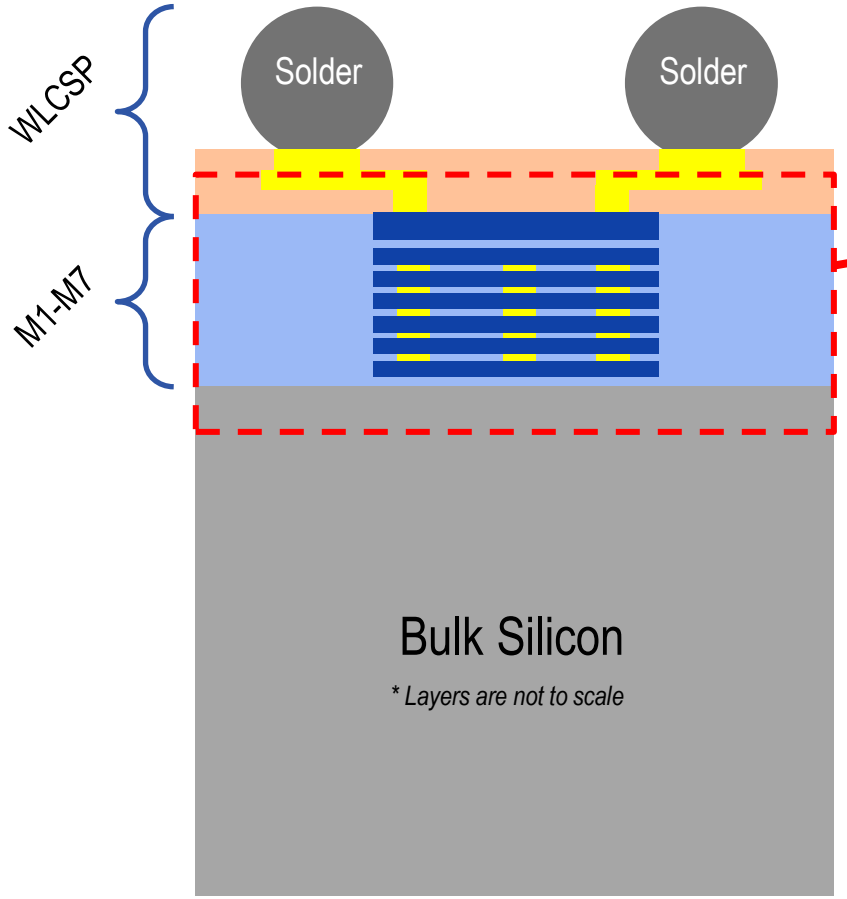
Test Vehicle	Stackup Includes
M1 Daisy Chain	BEOL (M1-M7) + WLCSP
M6 Daisy Chain	Shortflow (M6-M7) + WLCSP
RDL-Only Daisy Chain	WLCSP Only

** *Daisy chain structures do not contain silicon FEOL*

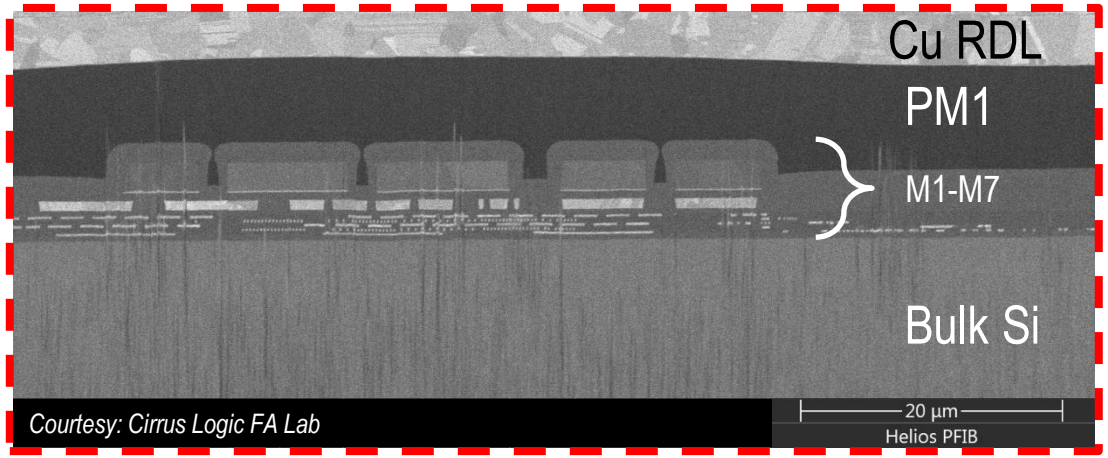
Test Vehicles: Package Outline

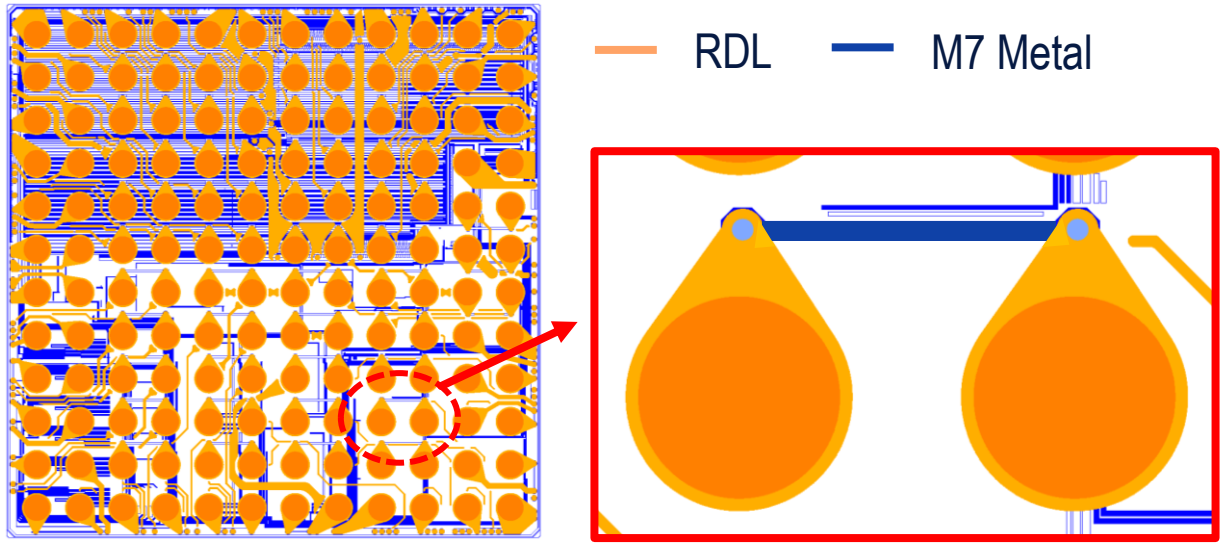


Test Vehicles: M1 Daisy Chain Structure

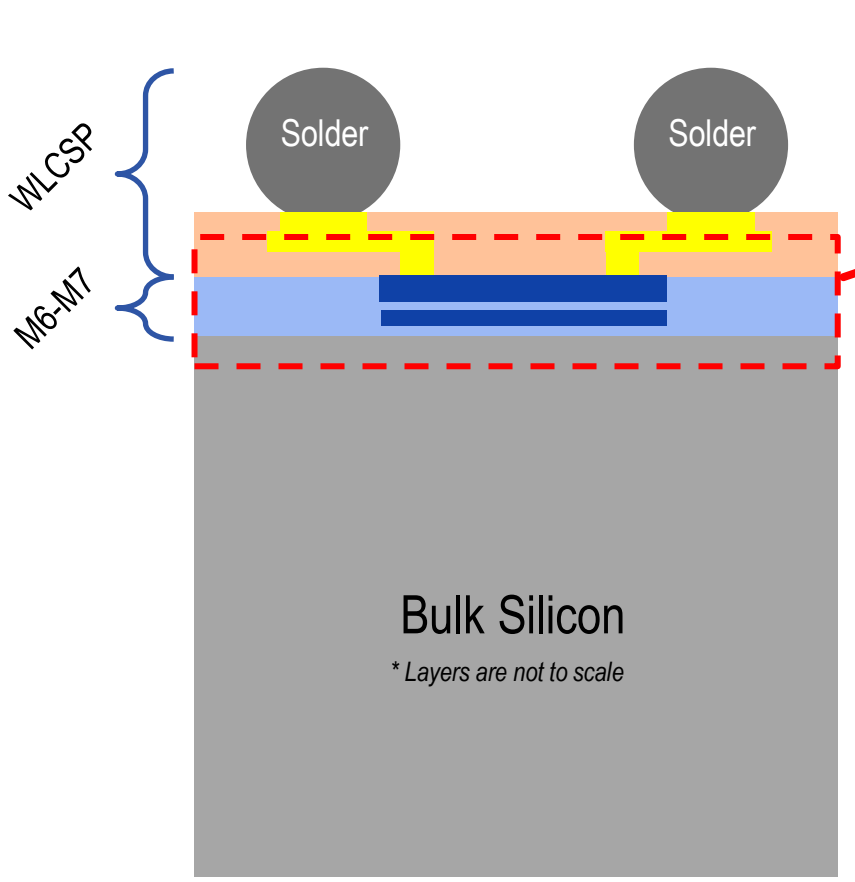


M7 integrated into daisy chain net, no continuity below M7

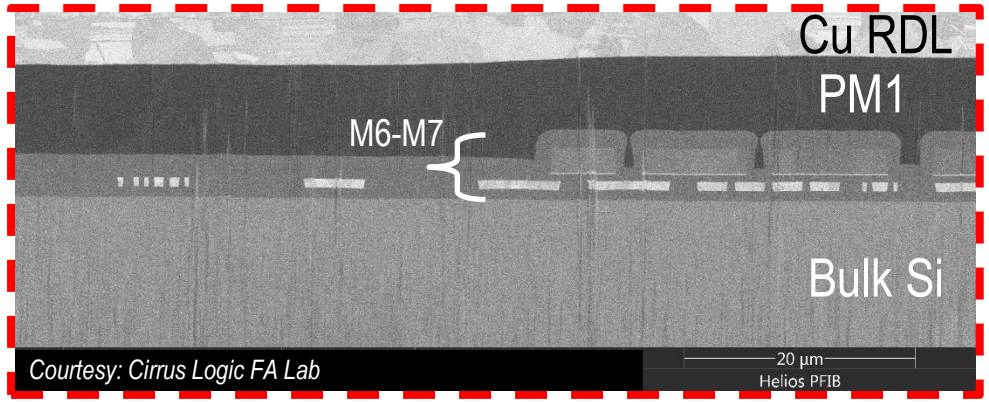


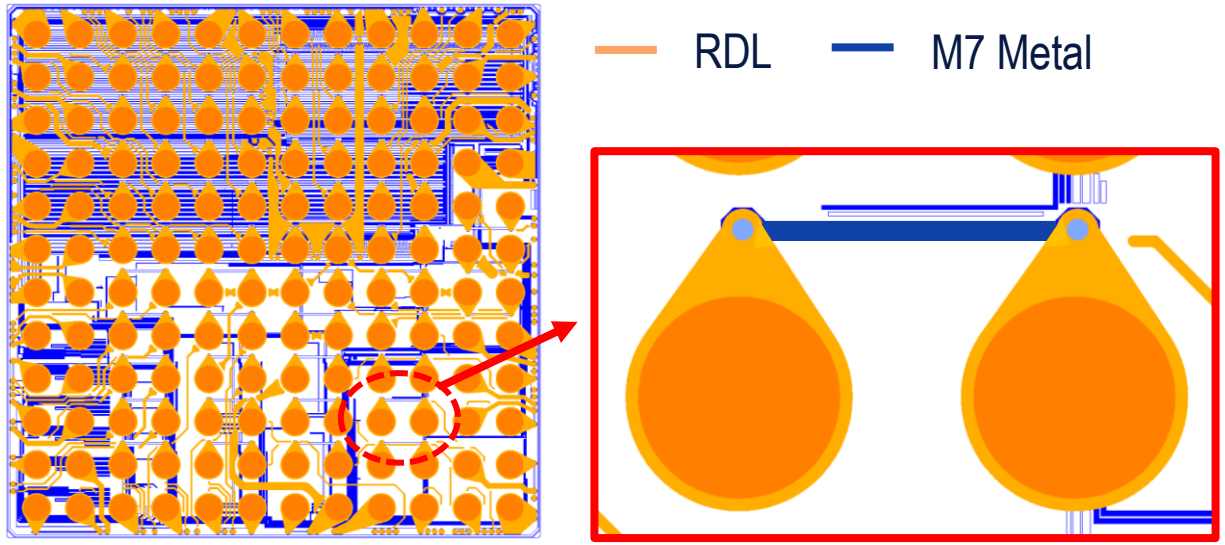


Test Vehicles: M6 Daisy Chain Structure

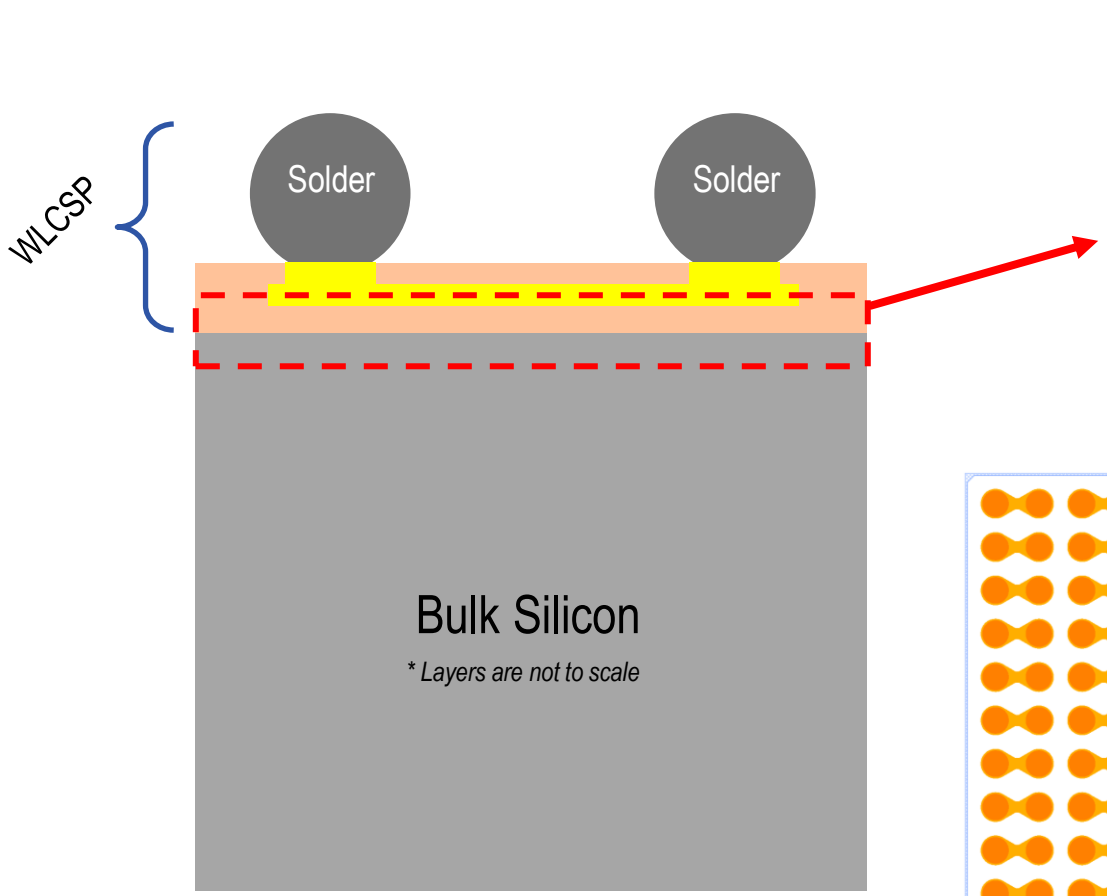


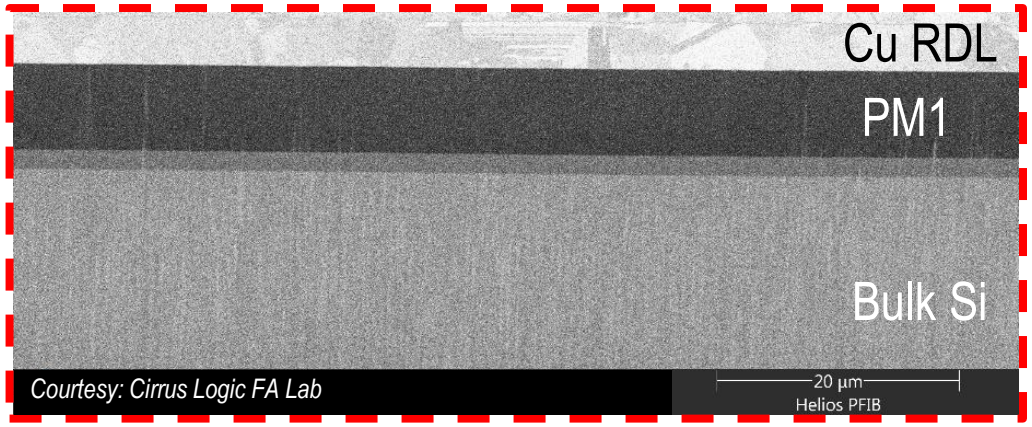
M7 integrated into daisy chain net, no continuity below M7

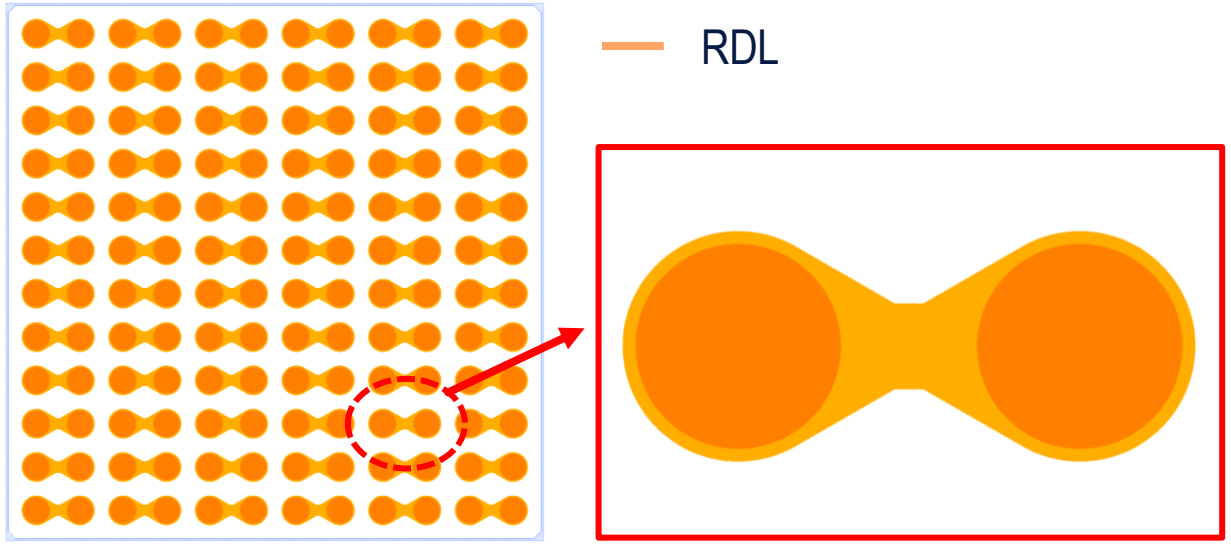




Test Vehicles: RDL-Only Daisy Chain Structure







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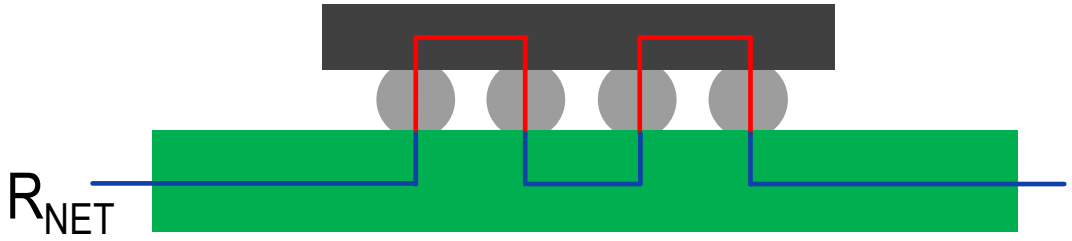
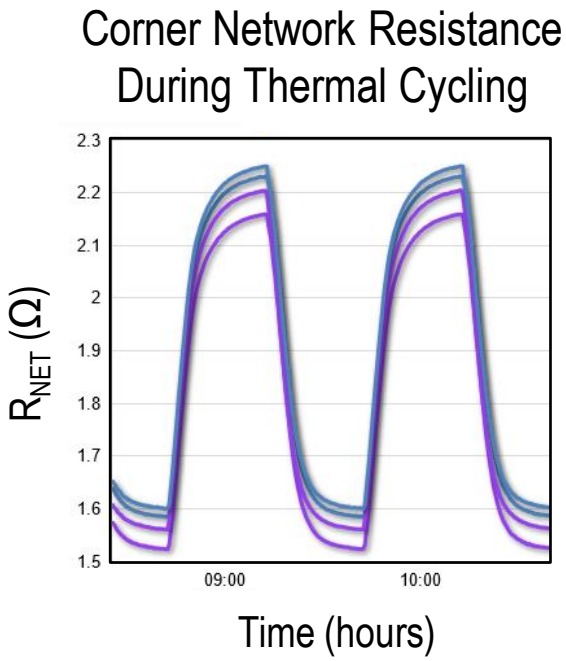
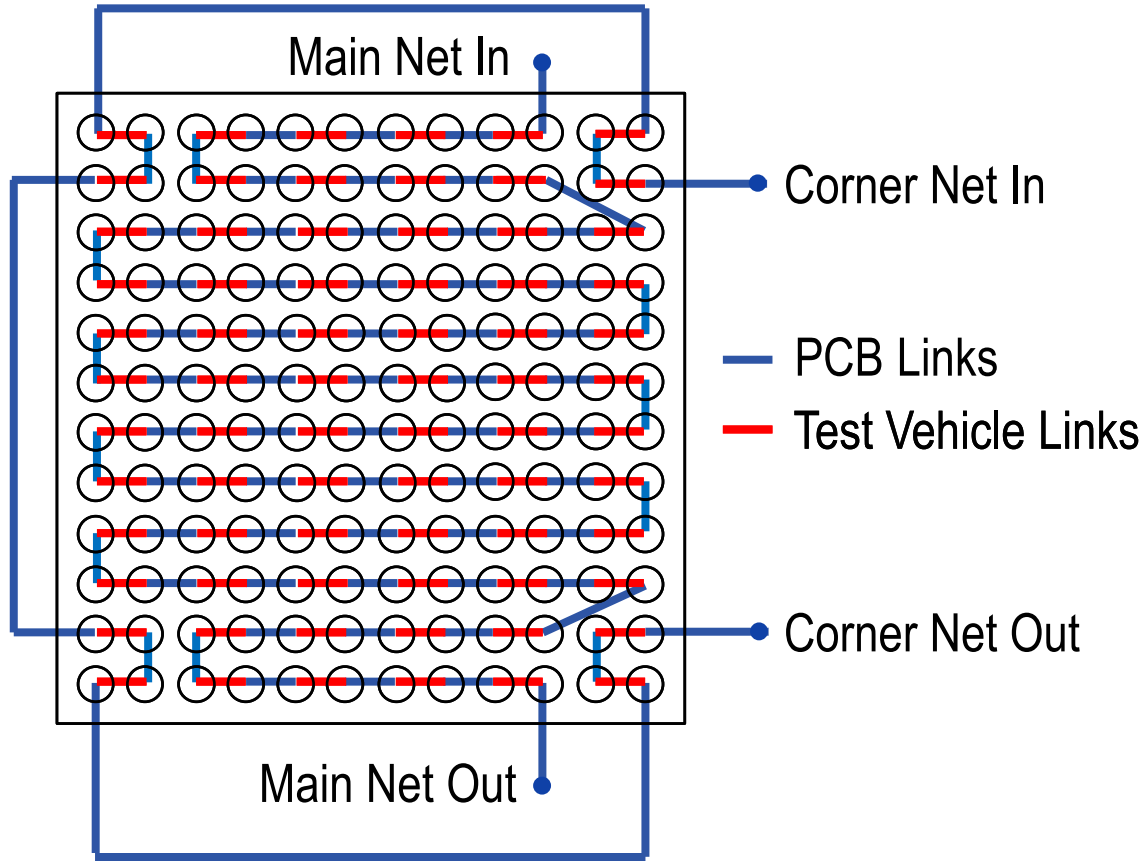
Experimental Setup: In-Situ Resistance Monitoring

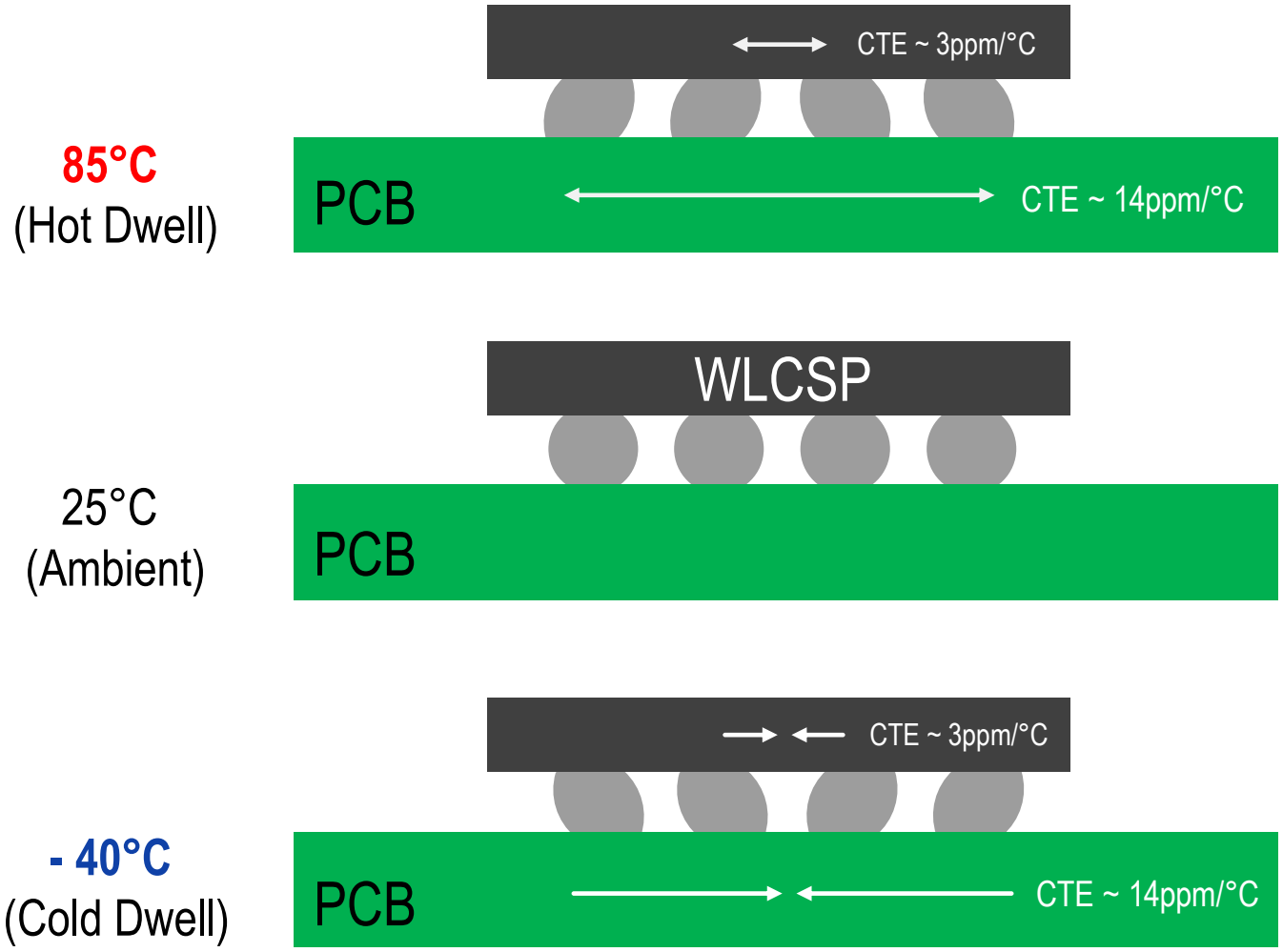


- Resistance for each network is sampled every 30 seconds by Keysight 34972A data logger
- An increase of 10% in network resistance is flagged as a failure
- Major resistance increases typically correspond to solder fatigue/fracture

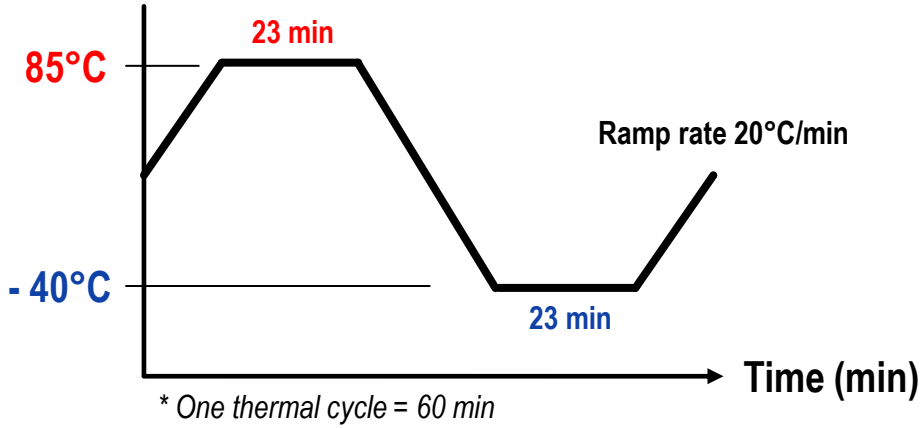




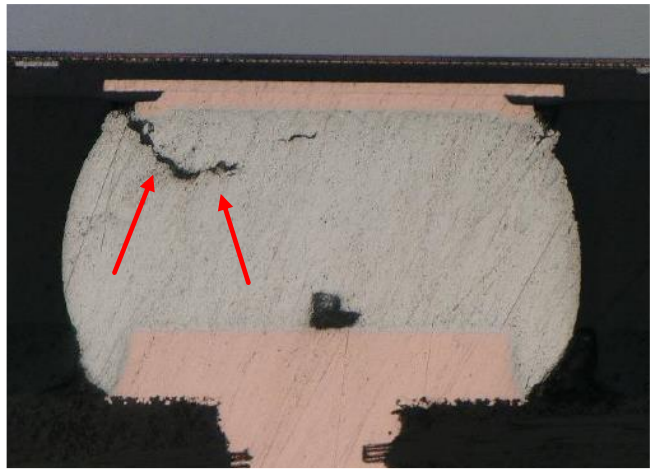
Experimental Setup: BLR Thermal Cycling



JEDEC BLR-TC condition N (JESD22-A104)



** One thermal cycle = 60 min*



Cyclic thermal stress ultimately causes bulk solder fatigue and crack propagation

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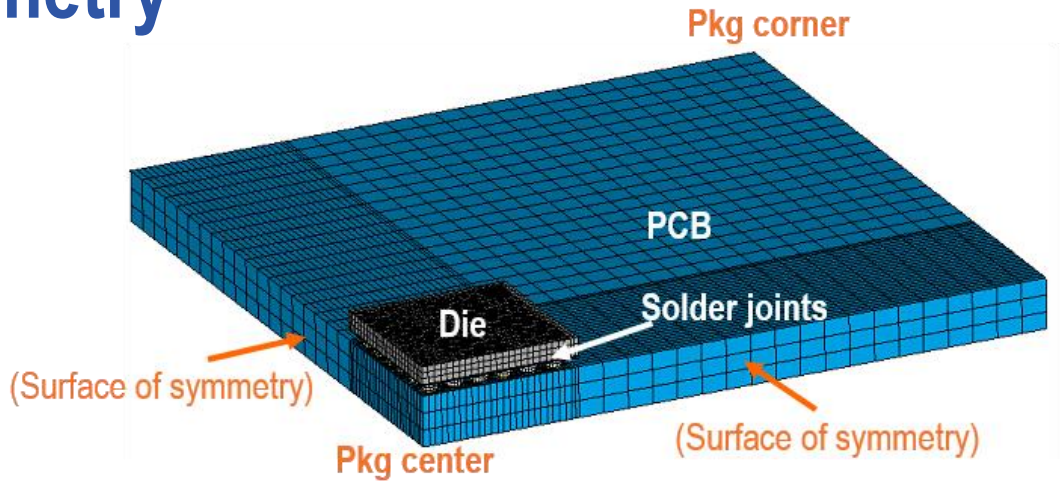
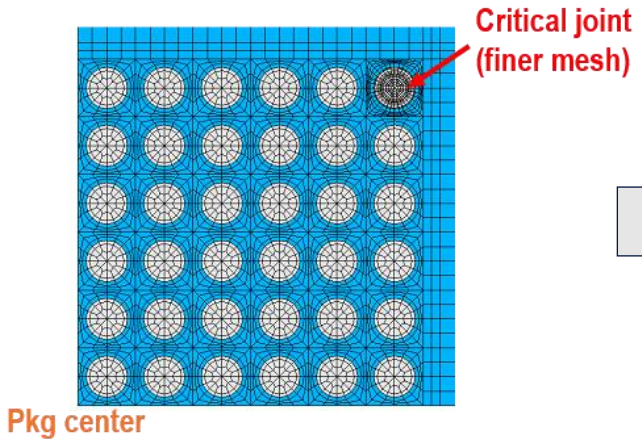
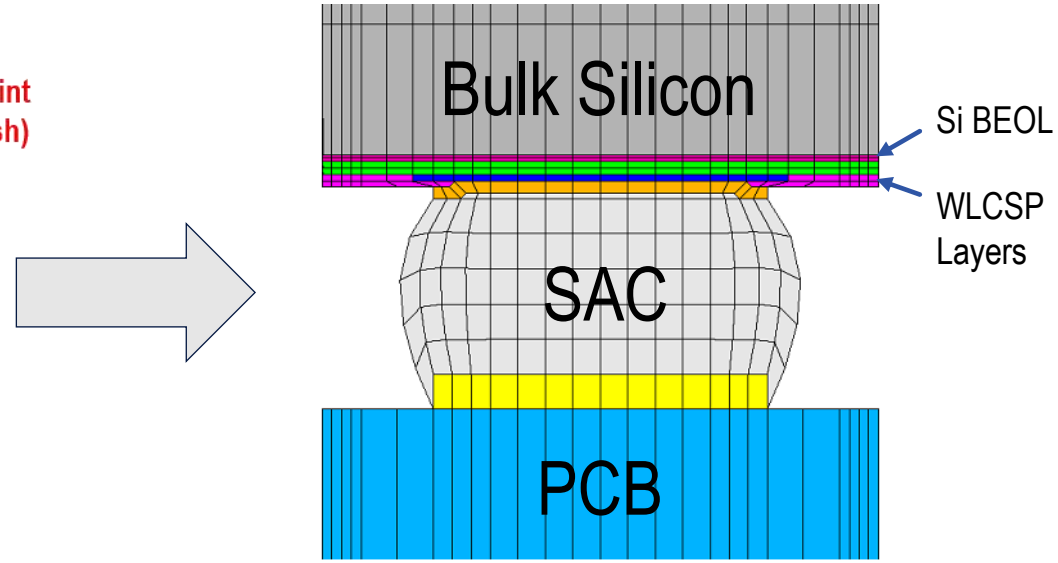
Modeling and Simulation: Geometry

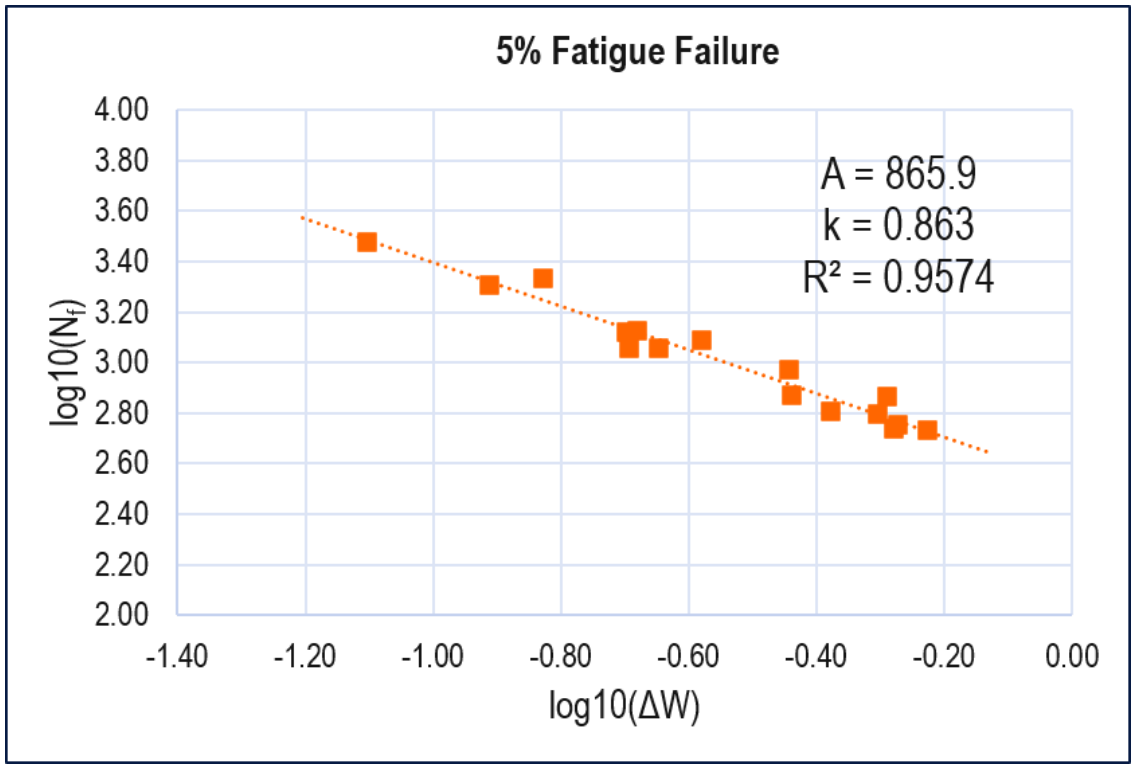
- 3D geometry, meshing, and solving in ANSYS
- Leverage package and BGA symmetry to create 3D quarter model
- Corner-most joints are critical and are meshed with finer elements







Modeling and Simulation: Correlation



- Energy-based fatigue model:

$$N_f = \left(\frac{A}{\Delta W}\right)^k$$

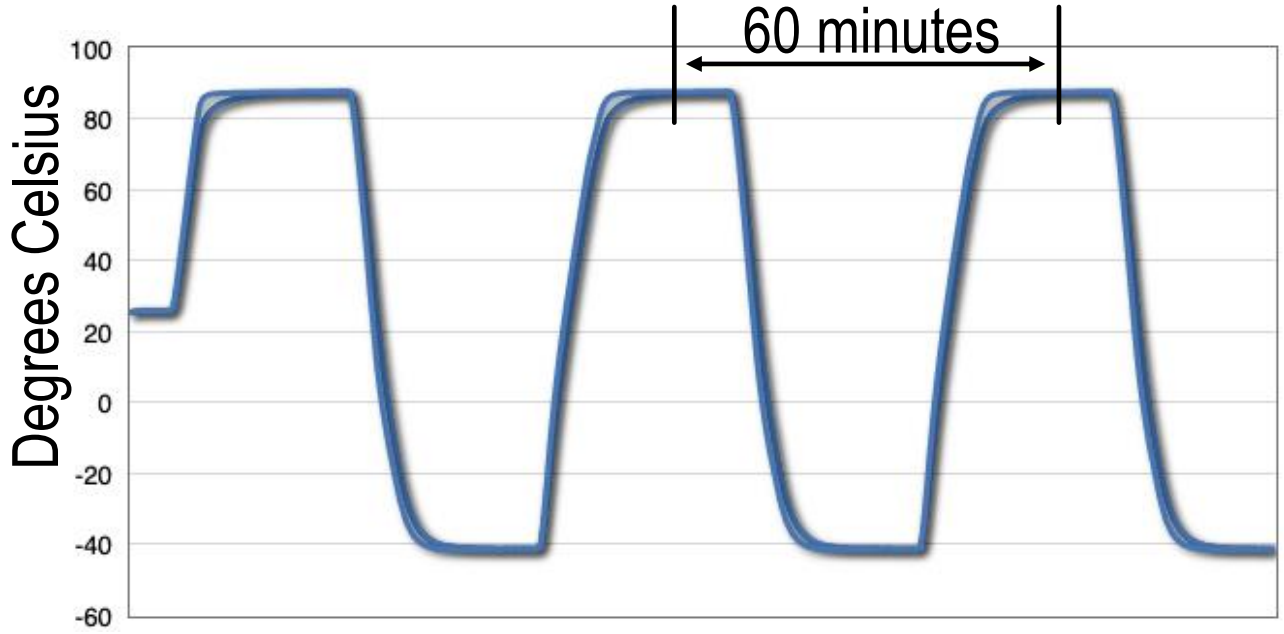
Cycles to failure

Correlation parameters

Inelastic work energy density (IWED)

- Correlation is drawn between historical test data and simulated IWED
- SAC correlation fit ($R^2 \approx 0.96$) suggests strong relationship
- *A* and *k* parameters determined from linear regression fit

Modeling and Simulation: Results



Test Vehicle	Predicted 5% Failure (cyc)
M1 Daisy Chain	1336
M6 Daisy Chain	1330
RDL-Only Daisy Chain	1298

- Simulation indicates variation of less than 3% for predicted 5% failure rate of all three test vehicle variations

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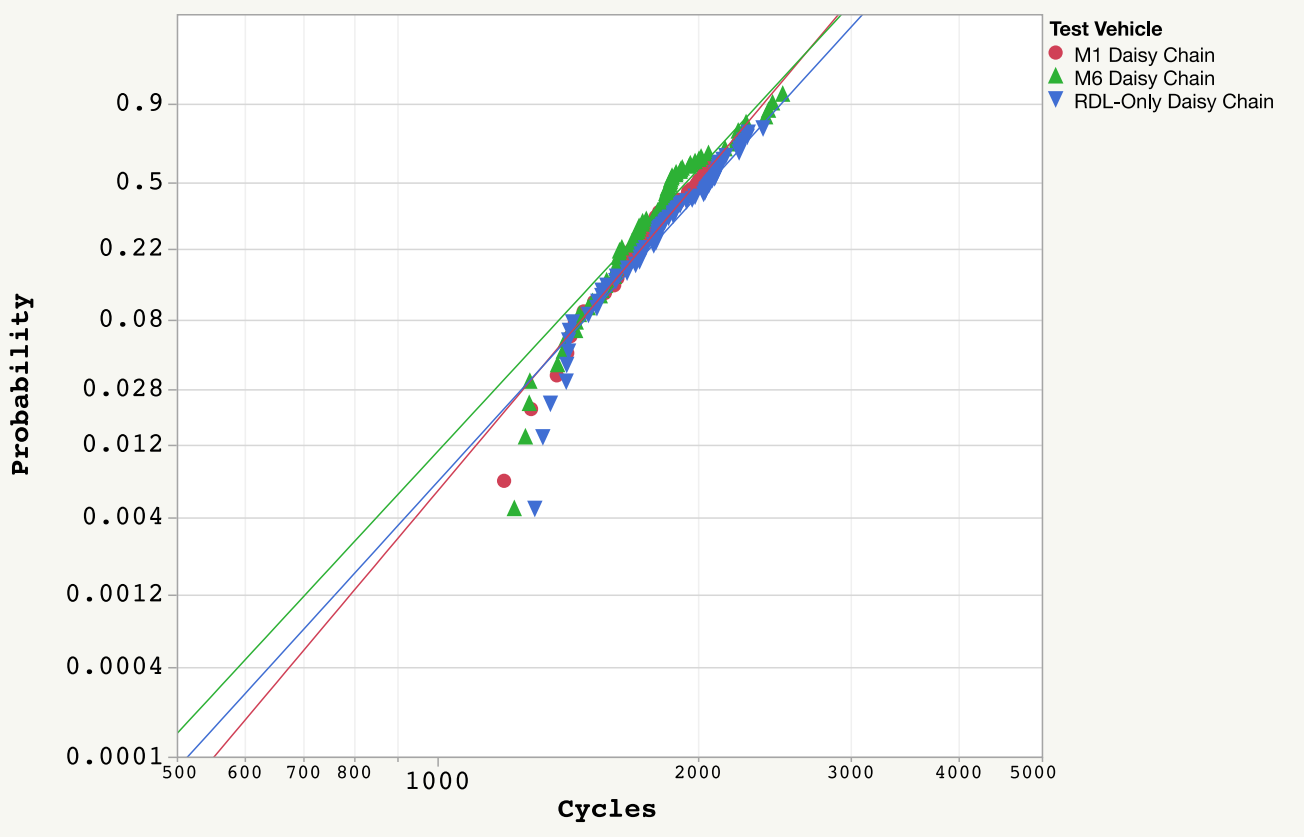
Experimental Results: Statistical Distribution

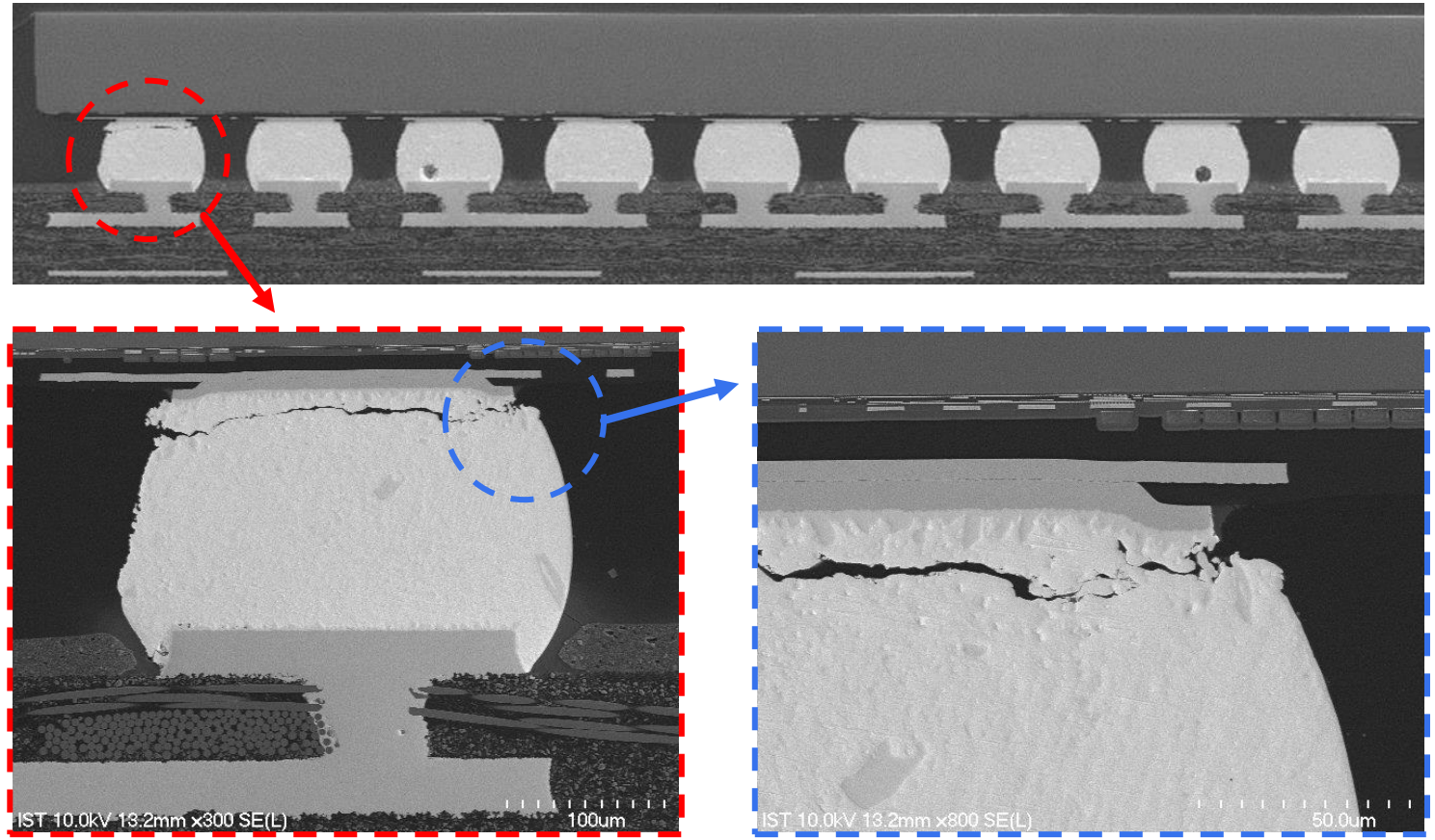


- Two-parameter Weibull fit of failures over time indicates no statistically significant difference between the three data sets
- Actual 5% failure results agree with predicted values within 5.4% percent error

Test Vehicle	Predicted 5% Failure (cyc)	Actual 5% Failure (cyc)	% Error
M1 Daisy Chain	1336	**1364**	2.1%
M6 Daisy Chain	1330	**1276**	4.1%
RDL-Only	1298	**1368**	5.4%

Experimental Results: Failure Analysis

- Early failures were isolated for debug and cross-section
- All failures exclusive to corner-most solder joint
- Zero failures on main daisy chain network
- Bulk solder fracture observed toward the package-side of solder joint (agrees with simulation)



Representative SEM images of corner ball solder fracture

Experimental Results: Applicability

- **Solder alloy** – results from this experiment may not be applicable to other solder alloys that result in failure modes other than bulk solder fatigue
- **Ball grid array** – variables such as pitch, orientation (orthogonal, staggered, etc.) should behave similarly as stress is a function of distance to neutral point (DNP)
- **Thermal cycling condition** – variables such as min/max temperature limit, soak time, etc. can potentially alter this result
- **Silicon node** – the similarity in outcome of the M1 and RDL-only test vehicles suggest that foundry process variation should not alter results

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Summary and Conclusions

- Outcome of study suggests that the presence of a full or partial Si BEOL does not have a statistically significant influence on solder fatigue life during BLR-TC
- WLCSP RDL layout does not have a statistically significant impact on solder fatigue life
- Numerical FEA predictions are within less than 5.4% error of actual results
- Results indicate that it may be possible to reduce the complexity of BLR daisy chain structures for product qualifications, especially when coupled with FEA, and maintain confidence in survival of solder joint interconnects in the field

Acknowledgements

The authors would like to acknowledge a multitude of cross-functional teams within Cirrus Logic that worked in concert to enable this study: Package Design, IC Layout Design, CAD Engineering, Supply Chain, Quality and Reliability, Silicon Technology, and Failure Analysis. We are also grateful for the guidance provided by David Patten (Cirrus Logic), as well as the diligent support of our outsourced manufacturing partners.

Thank You!!

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