Die-first and RDL-first FOWLP Processing for Flexible Hybrid Electronics

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Outline

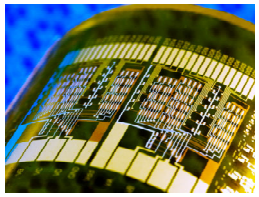
1. Background on Flexible Hybrid Electronics (FHE)

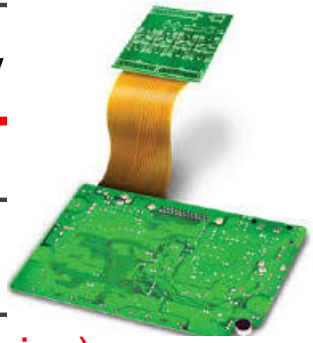
2. FHE Based on Fan-Out Wafer-Level Packaging Technology
   - 2.1. Process Integration
   - 2.2. Characterization
   - 2.3. Warpage and Die Shift Evaluation

3. Application of Flexible FOWLP with Embedded Chiplets

4. Summary

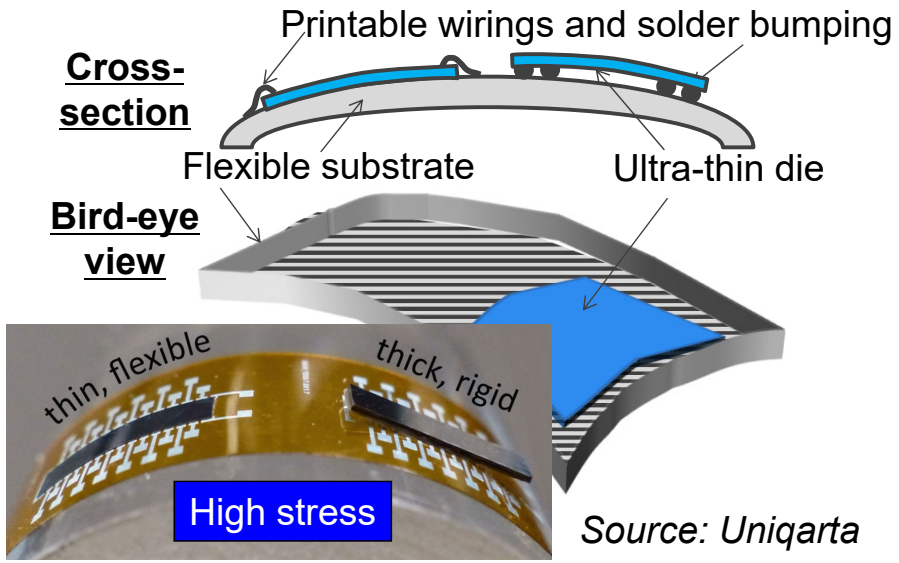
Comparison between Rigid and Flexible Electronics

	Rigid Si electronics	Flexible electronics
		Source: Purdue University. 
Devices	Inorganic single crystalline semiconductors (Si and III-V)	Organic semiconductors, amorphous or Poly Si etc.
Interconnects	PVD-based metals	Specialty inks and pastes
Processing	Wafer-level	Sheet-level (roll-to-roll)
Manufacturing technology	Photolithography	Printing (screen- / inkjet- / gravure-)
Scalability	High	Low
Performance	High	Low
Flexibility	Low (rigid/flex electronics)	High



FHE: Ultrathin Die Bonding on Flexible Substrates

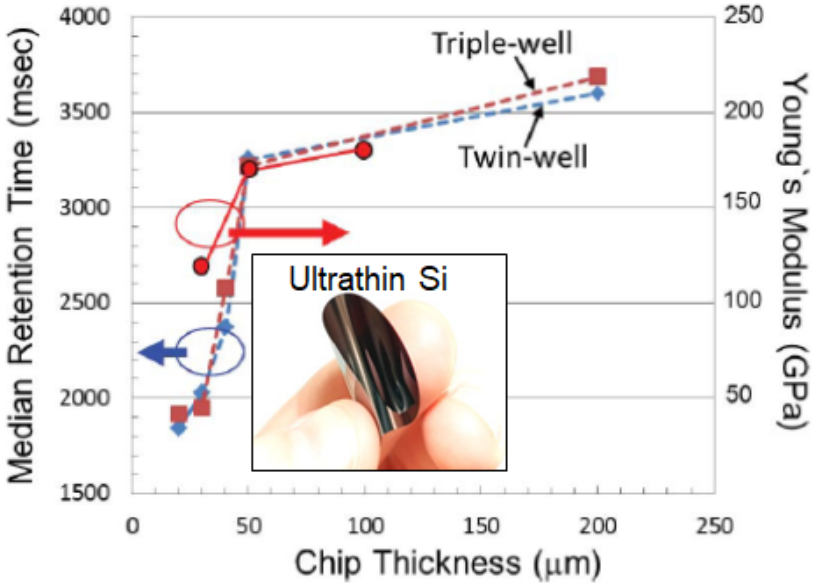
Conventional work



Source: Uniqarta

Sheet-level processing using printing

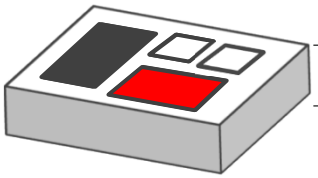
Source: K. Lee, T. Fukushima, M. Koyanagi *et al.*, *IEEE ELECTRON DEVICE LETTERS*, Vol. 34, 1038 (2013)



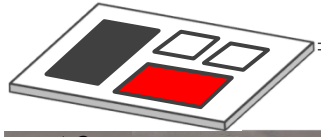
Relationship between chip thickness and retention time of thinned DRAM with planar capacitor.

Ultrathin Si is flexible. That is true, but the ultrathin Si is unstable toward repeated bending with a small curvature radius, and Si devices are sensitive to mechanical stresses that cause serious reliability issues to give characteristics variation etc.

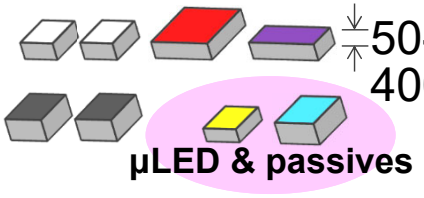
Concept of New FHE with Embedded Chiplets



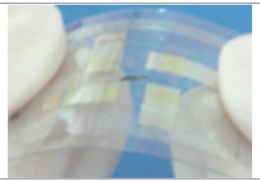
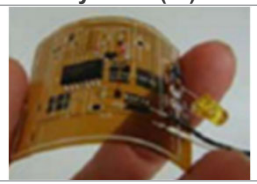
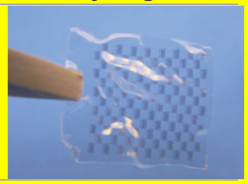
Typical large chip (rigid electronics)



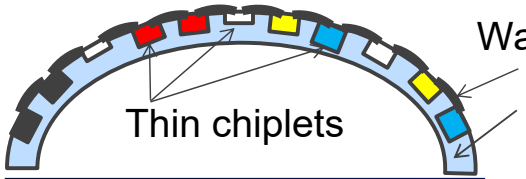
Ultrathin chip (conventional FHE)



Thin chiplets (new FHE)

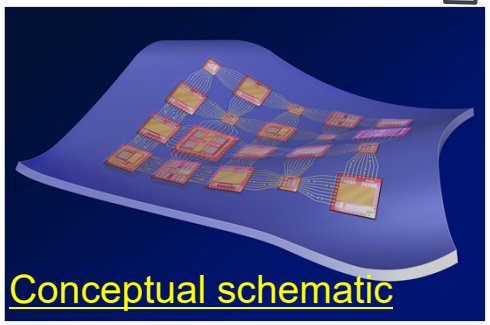
	Polyethylene telephthalate (PET)	Polyimide (PI)	Polydimethyl-siloxane (PDMS)	Hydrogel
				
Adaptability	△	△	○	○
Biocompatibility	×	△	○	○
Permeability	×	×	×	○
Breathability	×	×	×	○
T_g	50℃	>350℃	< -100℃	-

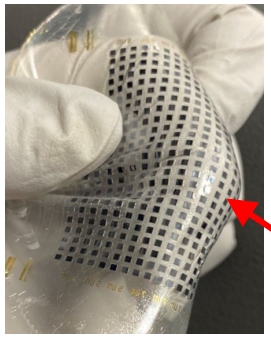
Cross-section



Wafer-level high-density wirings

Flexible substrate





New FHE with 400 pcs embedded 0.1-mm-thick /1-mm-square chiplets in PDMS

TOHOKU UNIVERSITY

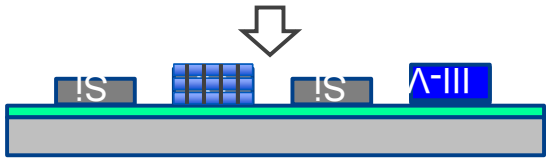
CHIPS CENTER FOR HETEROGENEOUS INTEGRATION AND PERFORMANCE SCALING

UCLA

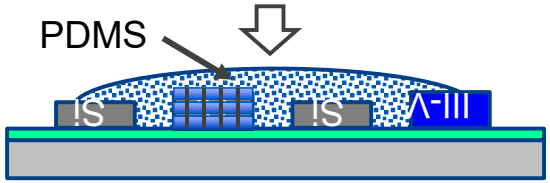
T. Fukushima, A. Alam, & S. S. Iyer *et al.*, *IEEE Trans. CPMT*, 8 (2018), p. 1738.

A Fabrication Flow of FlexTrate™ using Flexible Fan-Out WLP Process with a Biocompatible PDMS

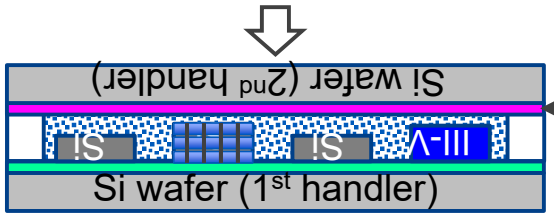
1) Temporary adhesive layer formation



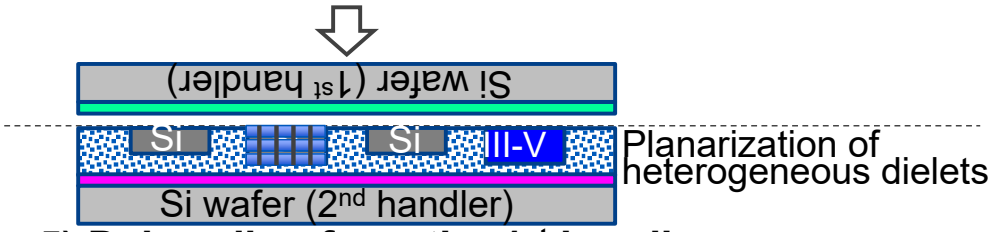
2) Multichip flip-chip assembly on 1st handler



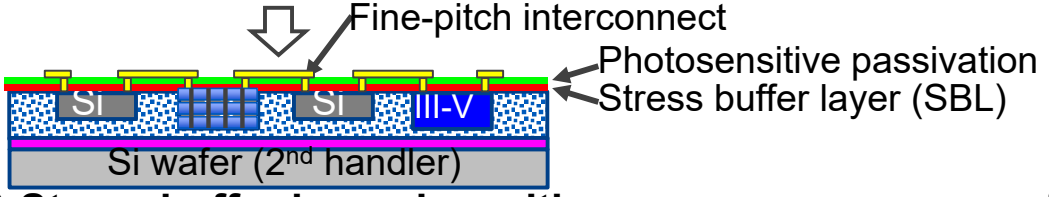
3) PDMS supply



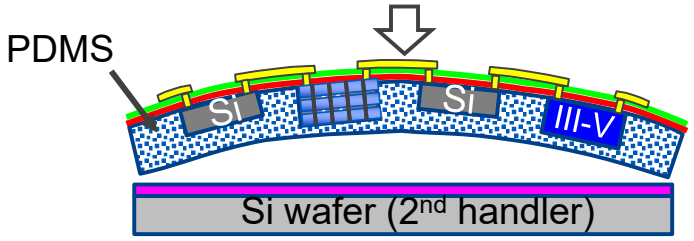
4) Wafer-level compression molding



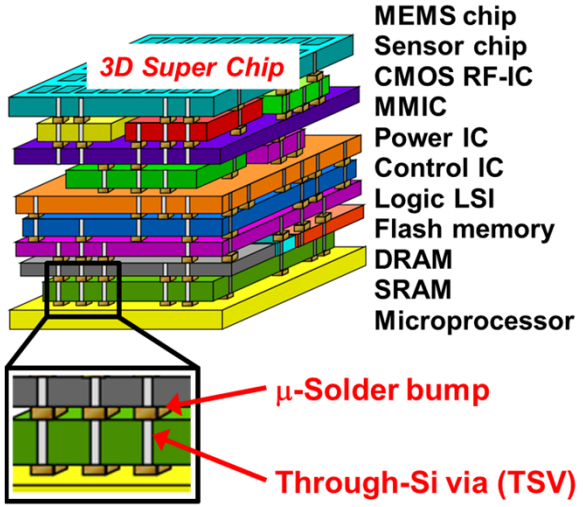
5) Debonding from the 1st handler



6) Stress buffer layer deposition and metallization on Si and PDMS



7) Debonding from the 2nd handler



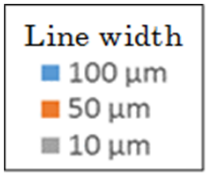
This transfer process allows wafer-level processing to make embedded chiplets in flexible substrates with fine-pitch interconnects.

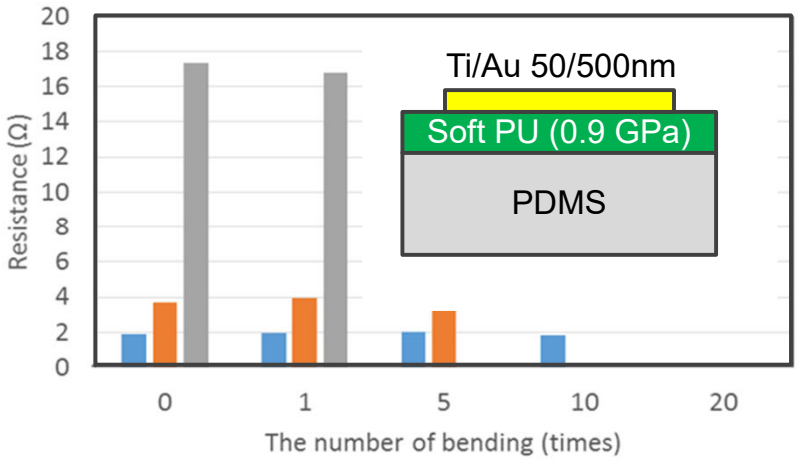
Effect of Young's Modulus/CTE of SBL on Bending Property

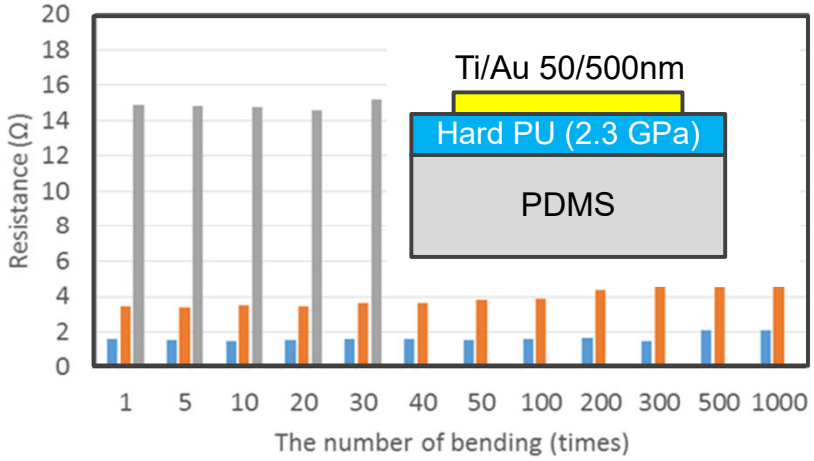
Metal	Young's modulus (GPa)	CTE (ppm/K), α1/α2 (Tg)
Photoresist	0.25-5	30-70
Au	~80	14.2
Cu	100-120	17
SBL: Soft PU SBL: Hard PU	0.9 2.3	100/190 (Tg: 49) 70/150 (Tg: 47-58°C)
PDMS	0.0005	~ 300

Au wirings formed on hard Polyurethane layer as a SBL exhibit the highest bendability.
Au wirings with a hard Polyurethane show high bendability to mitigate the Young's modulus and CTE mismatches.

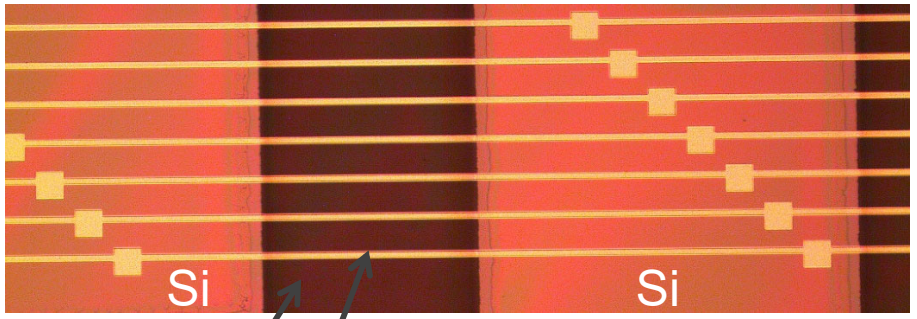
PDMS thickness: 500 μm
SBL thickness: 30 μm
Bending radius: 20 mm

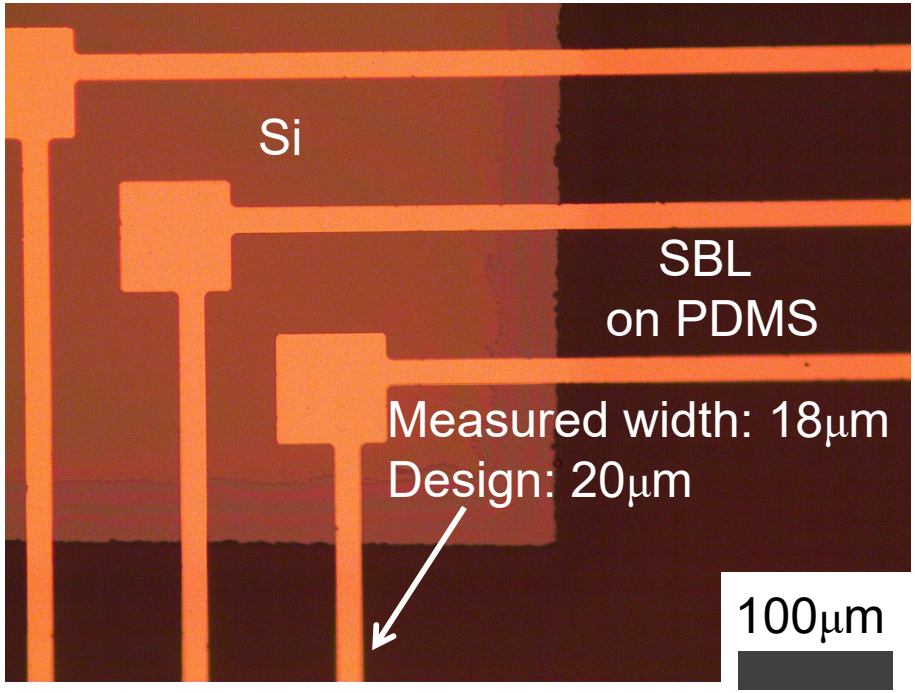




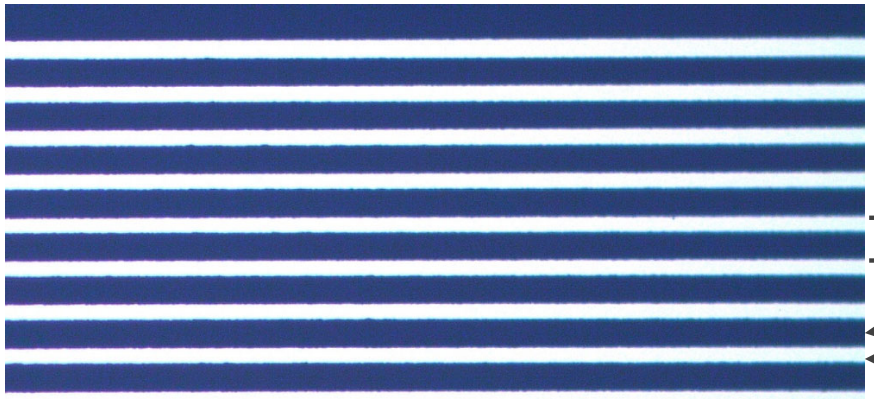


High-Density Interconnects Connecting Neighboring Si Chiplets Embedded in PDMS



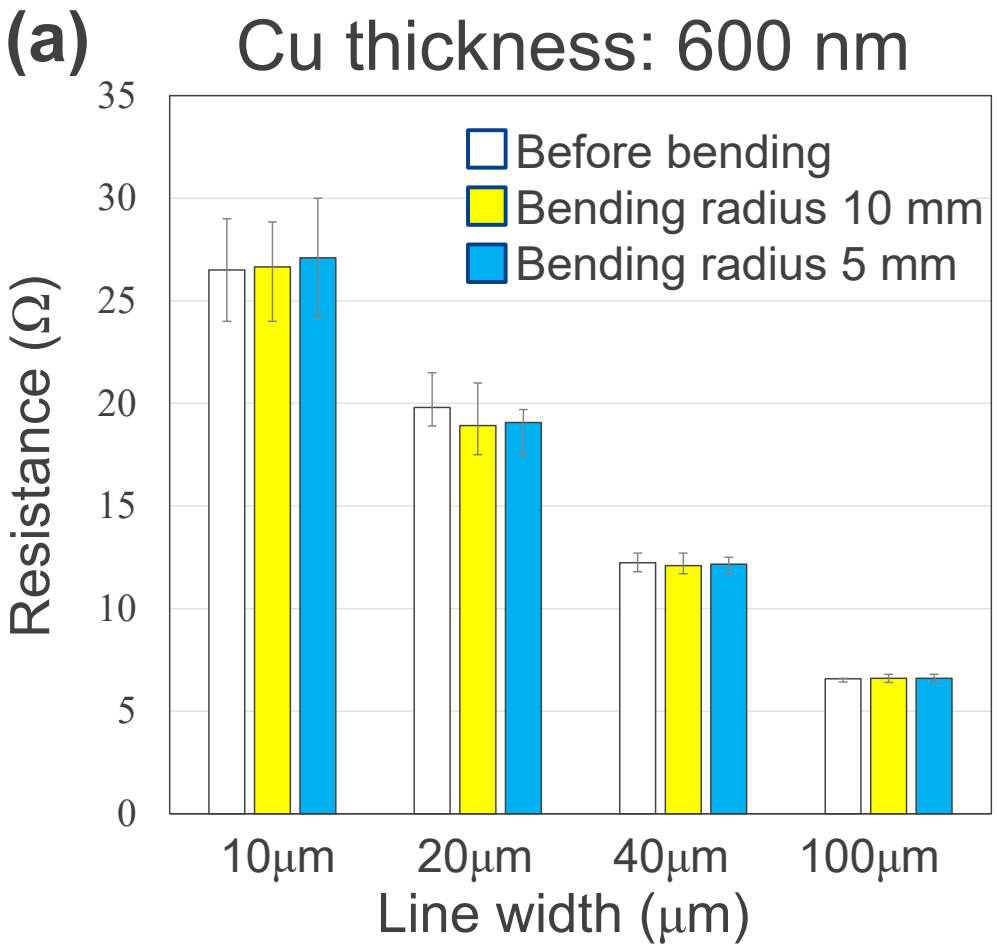


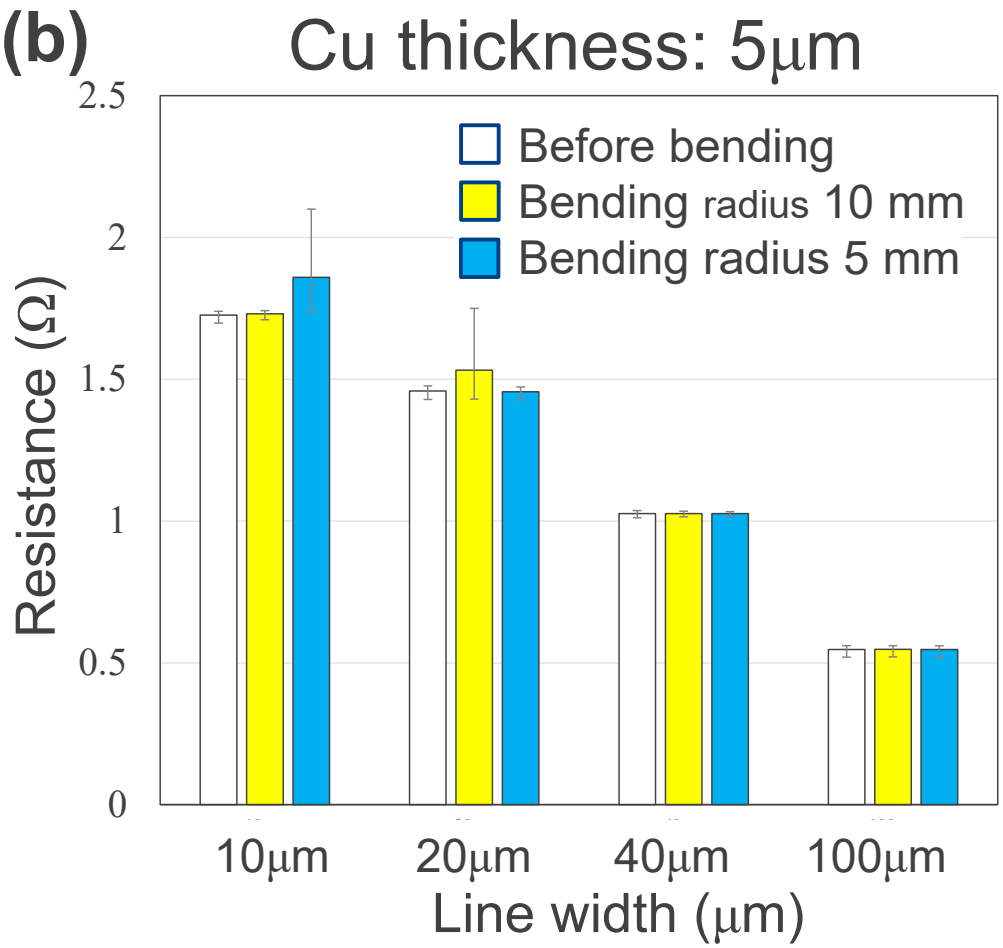
Line/space: 3.6μm/4.4μm



Fine-pitch (pitch: 8μm) wirings are successfully formed on PDMS.

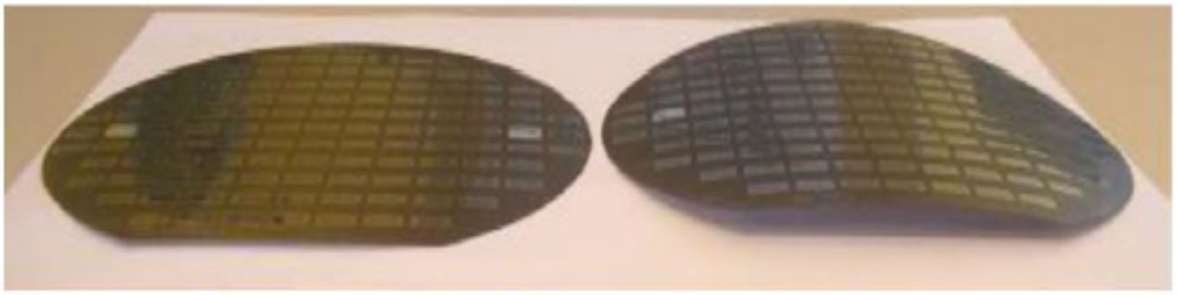
Resistance Comparison before/after 1,000-Cycle Bending





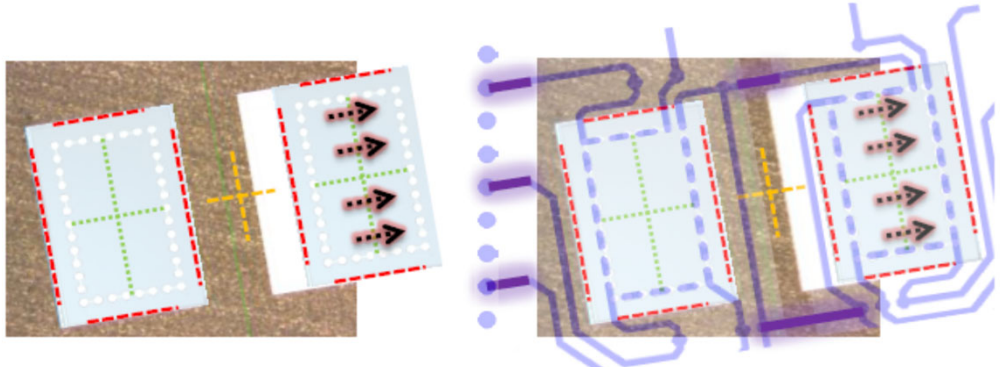
The Biggest Two Concerns in Typical FOWLP with Rigid Epoxy

1. Wafer bow (warpage)



1 mm or more

2. Die shift (chip drift)



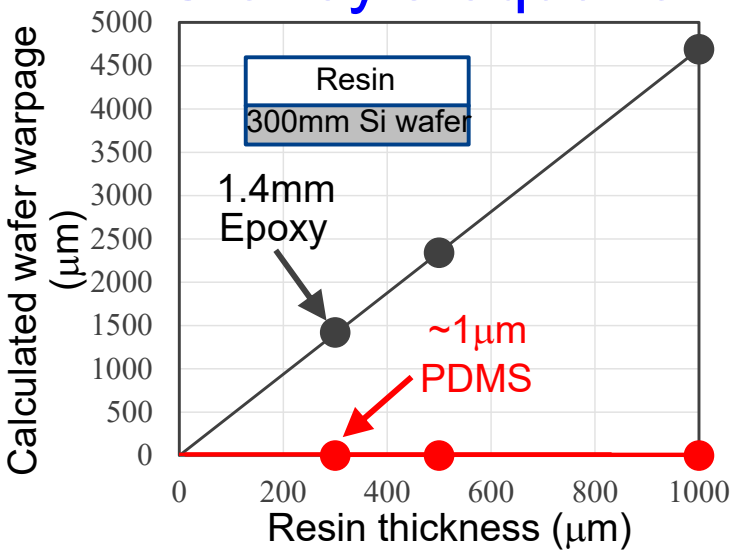
Average die shift: 45μm

Sharma et al, IEEE CPMT vol. 1, p.502, 2011

Wafer Bow Comparison between PDMS and Epoxy

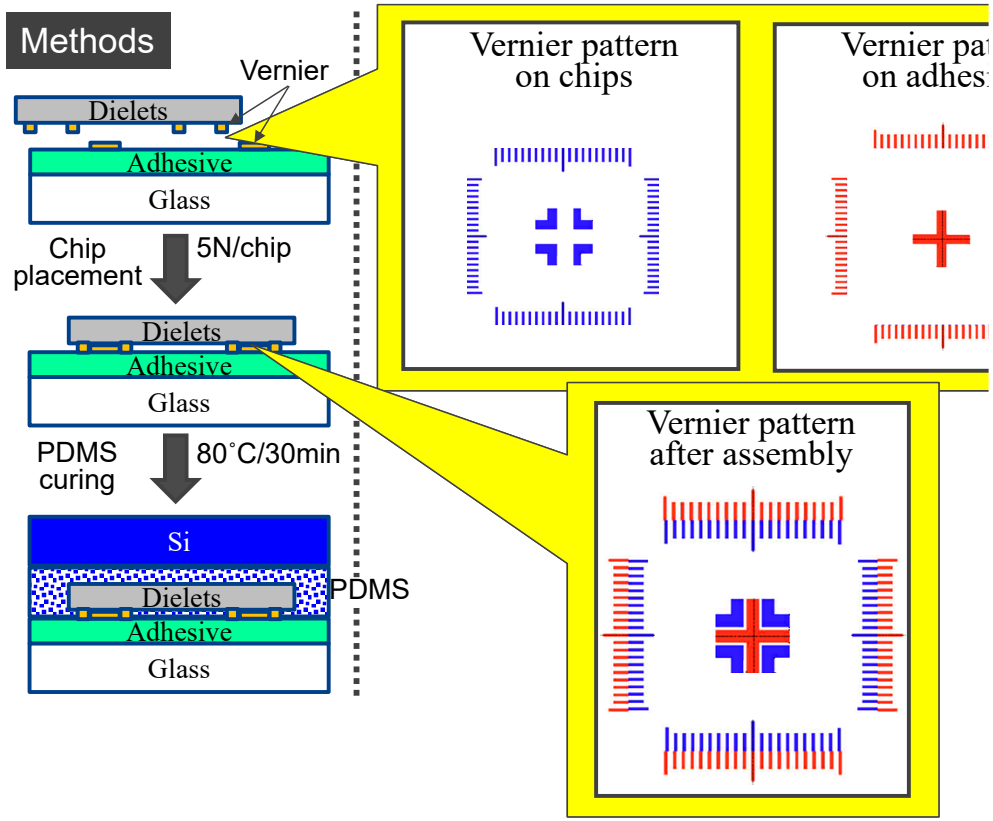
Properties	PDMS (MDX4-4210 / Dow)	Epoxy Mold Compound (EMC)
Hardness	30 (Shore A)	
Tensile strength	5 MPa	
Elongation at break	~500%	< 1%
ε @ 100kHz	3.0 (3.01@100Hz)	
tan δ @ 100KHz	0.001 (0.0009@100Hz)	
CTE	~300 ppm/K	7.5 ppm/K
Young's modulus	**0.5 MPa**	**22 GPa**
Tg	-120˚C	165˚C
Decomposition temp.	200˚C or more	~ 200˚C
Curing temp.	25-80˚C	125-150˚C
Biocompatibility	Passed up to 29 days for the human body implantation	None

Calculated by Stoney's equation



Die Shift Evaluation with PDMS

Die shifts were reduced down to several micrometers by using PDMS

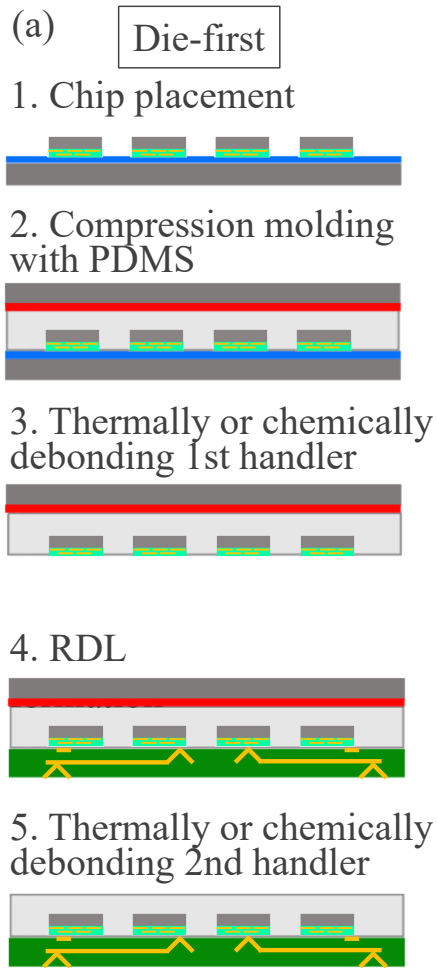


	Thermo-Mechanical (TM) effect	Fluidic-Force (FF) effect
 Die-Shift increase	High compression speed Large warpage (large CTE mismatch between carrier wafers and mold) High curing temperature High Young's modulus High CTE from r.t. to T_g Thick mold The outermost dies	Thin and small dies High-density die pitch Low placement load Low adhesion between dies and adhesions/tapes High viscosity mold Thin mold The outermost dies
Die-Shift decrease 	Low compression speed Small warpage (small CTE mismatch between carrier wafers and mold) Low curing temperature Low Young's modulus Low CTE (r.t. $< T < T_g$) Thin mold The central dies	Thick and large dies Low-density die pitch High placement load High adhesion between dies and adhesions/tapes Low viscosity mold Thick mold The central dies

Advantages of Die-first and RDL-first Flexible FOWLP

Advantages in die-first (flexible) FOWLP

- No bonding processes, Just only gentle placement
- Small die shift with PDMS, Compared with EMCs
- Higher adaptability than conventional PI substrates



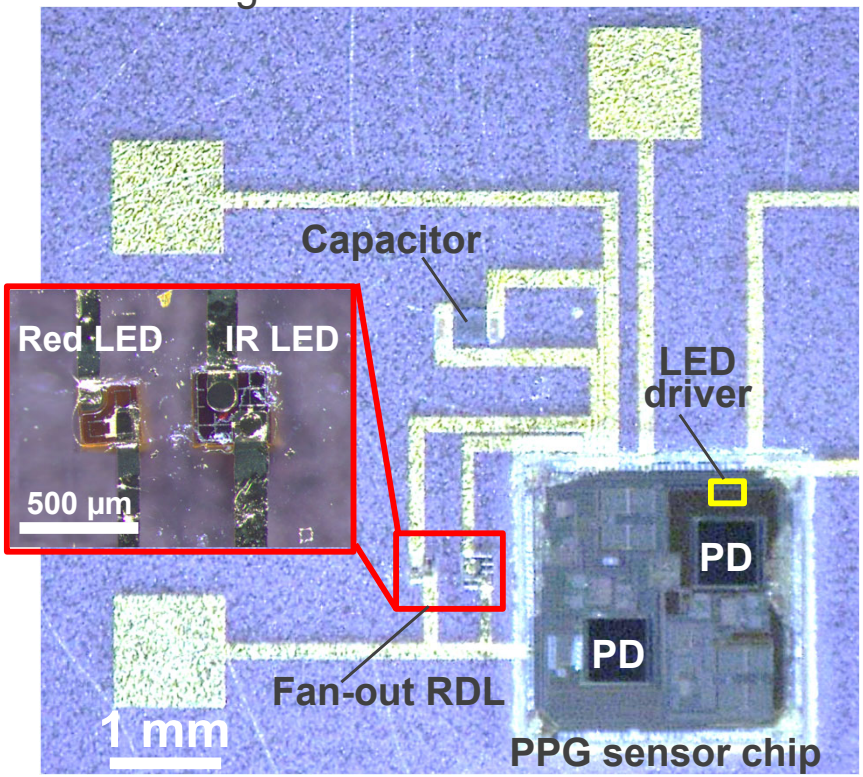
Advantages in RDL-first (flexible) FOWLP

- Fine-pitch RDLs can be fabricated
- No die shift resulting from RDL-first FOWLP methodology
- Water-based hydrogels can be used: higher biocompatibility and breathability

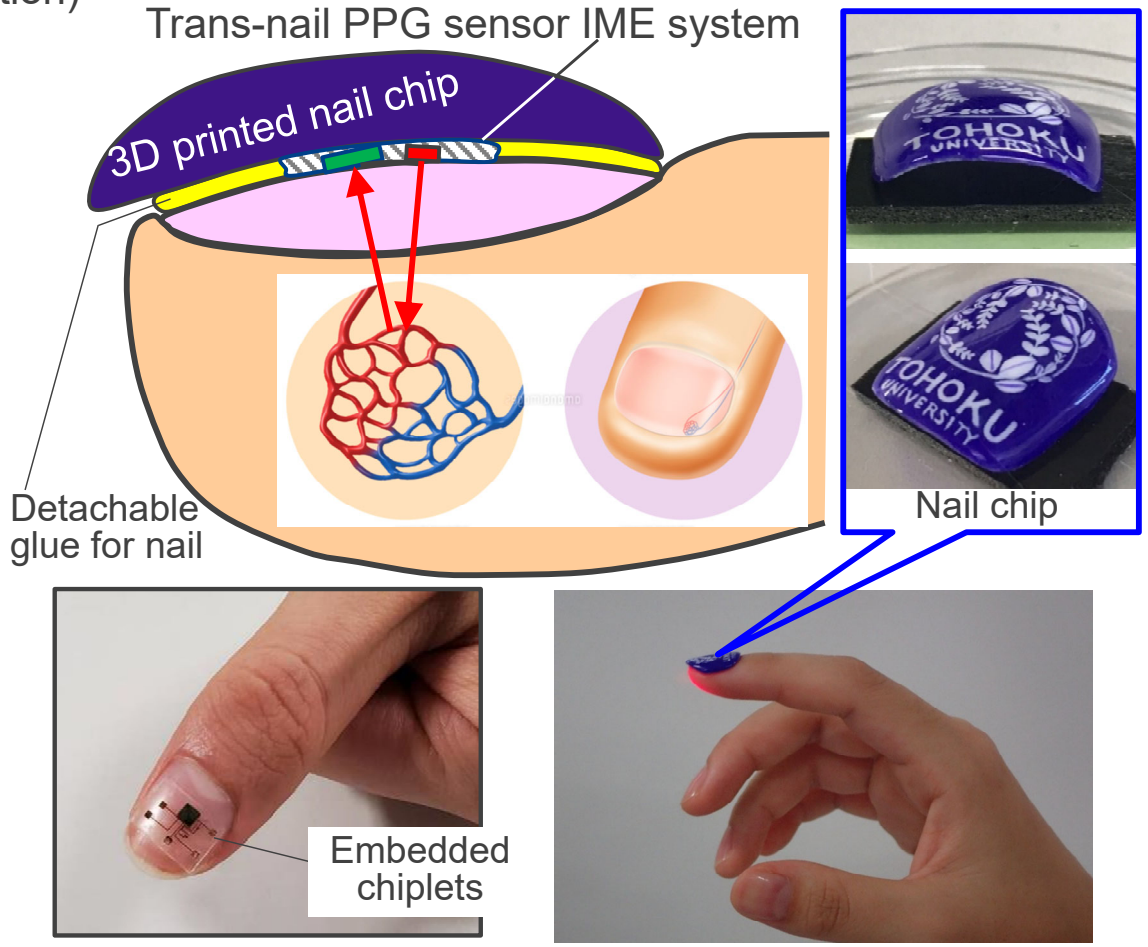
Applications

1. Trans-Nail photoplethysmogram (PPG) Sensor

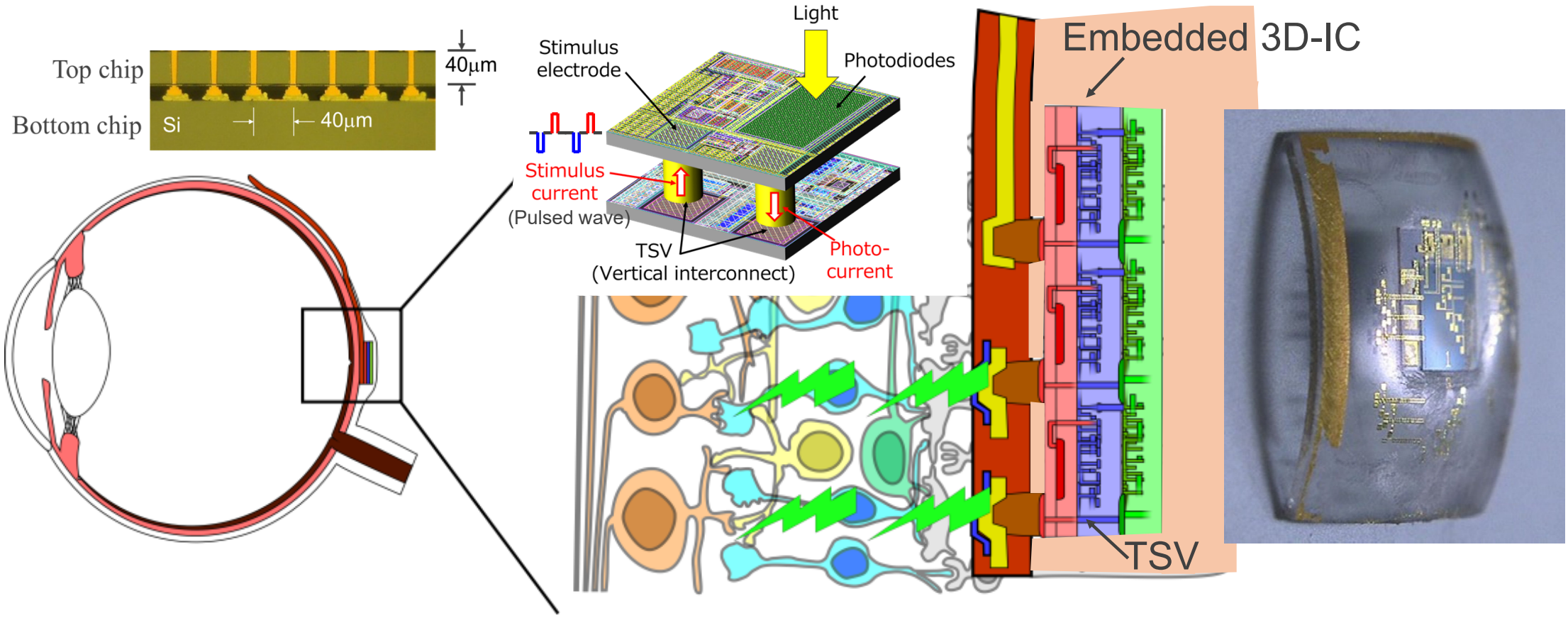
For pulse wave and SpO_2 (percutaneous oxygen saturation) monitoring on nail where there is no sweat



A photo of a flexible IME system with a PPG sensor and micro-LED chiplets

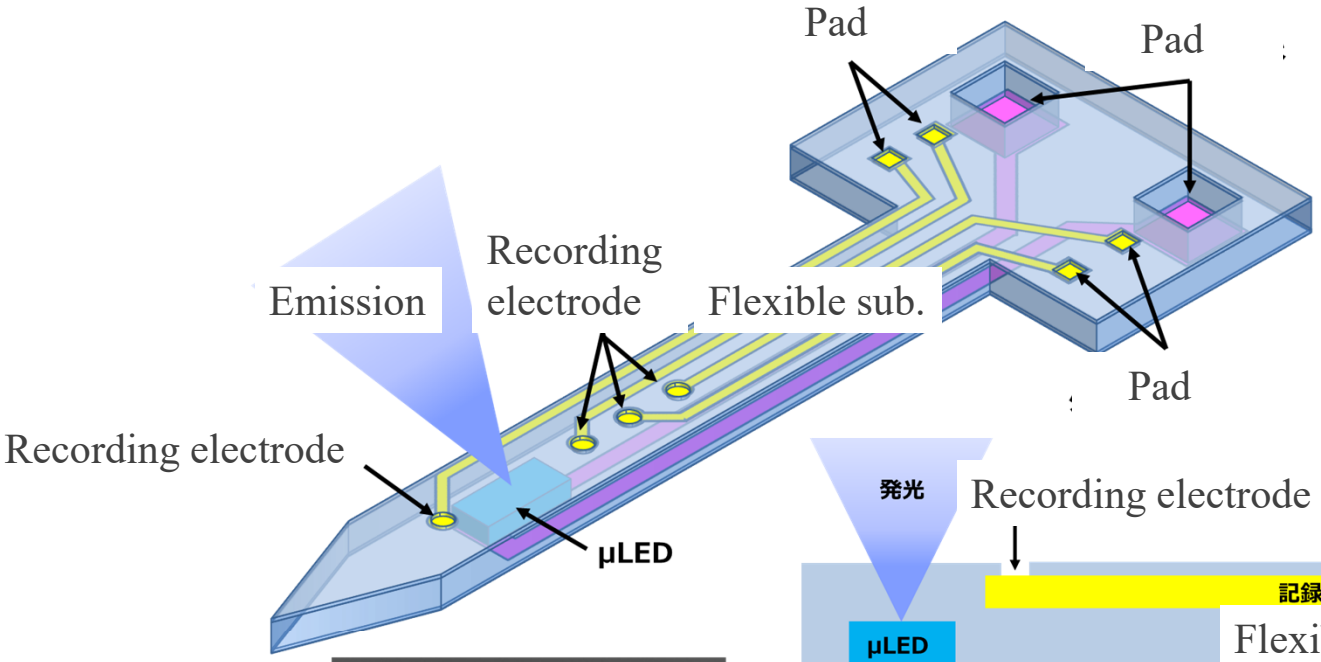


2. Flexible Retina Prosthesis System

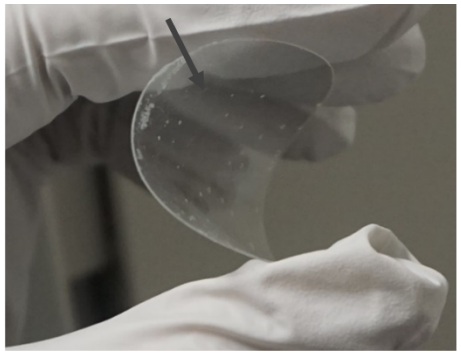


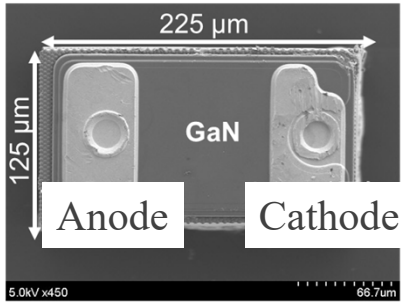
Subretinal 3D retinal prosthesis chiplet with TSV will be implanted behind eyeball.

3. Flexible Neural Probes for Deep Brain Stimulation with micro-LED for Optogenetics



Medical-grade flexible epoxy



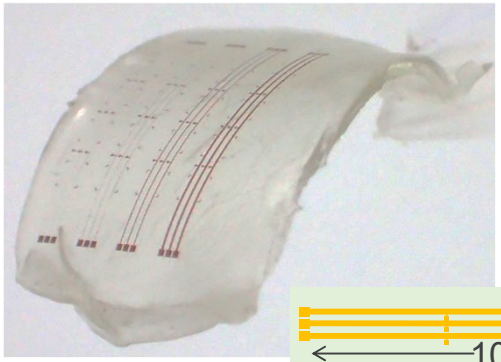


Blue micro LED

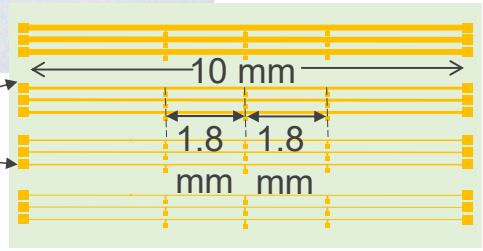
- ✓ **Optical stimulation and electrical recording of neural signals**
- ✓ **High biocompatibility for long-term implantation**

4. Hydrogel-Based FHE by RDL-first FOWLP

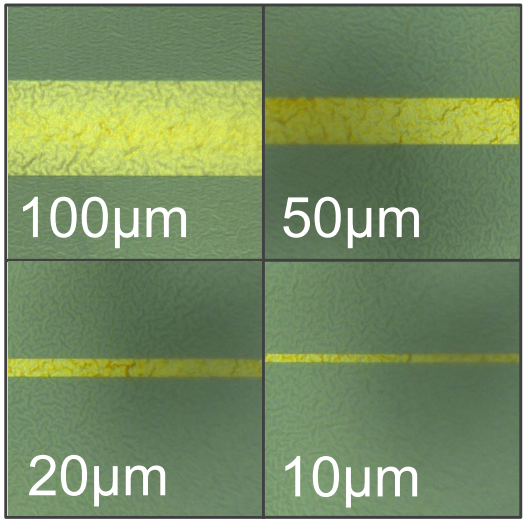
Bending test of Au wire formed on hydrogel



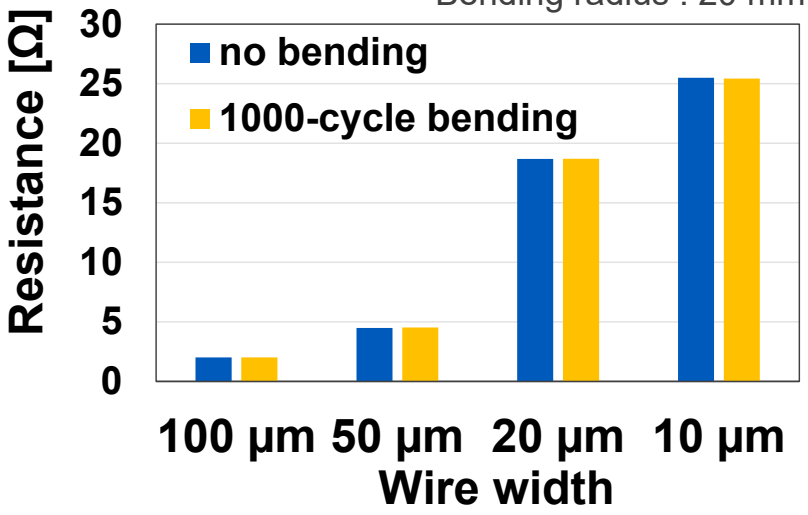
< Top view >



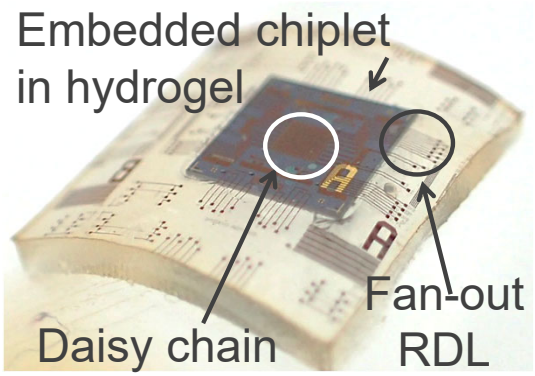
< Optical micrograph>



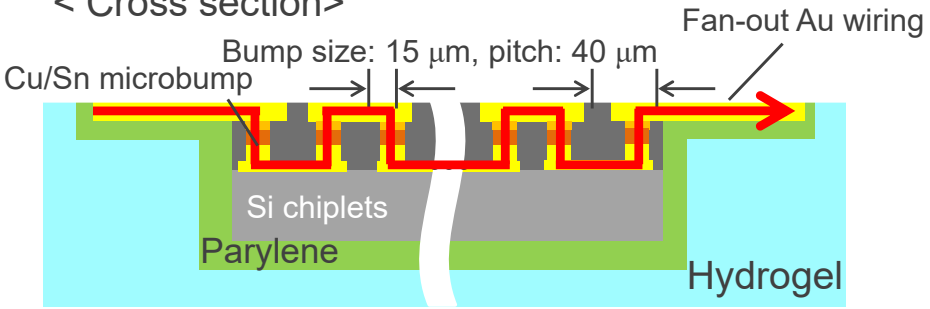
Bending radius : 20 mm

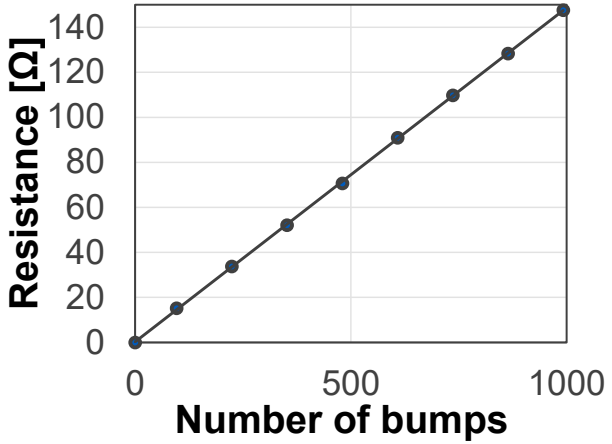


Daisy chain characteristics of Si chiplet embedded in hydrogel

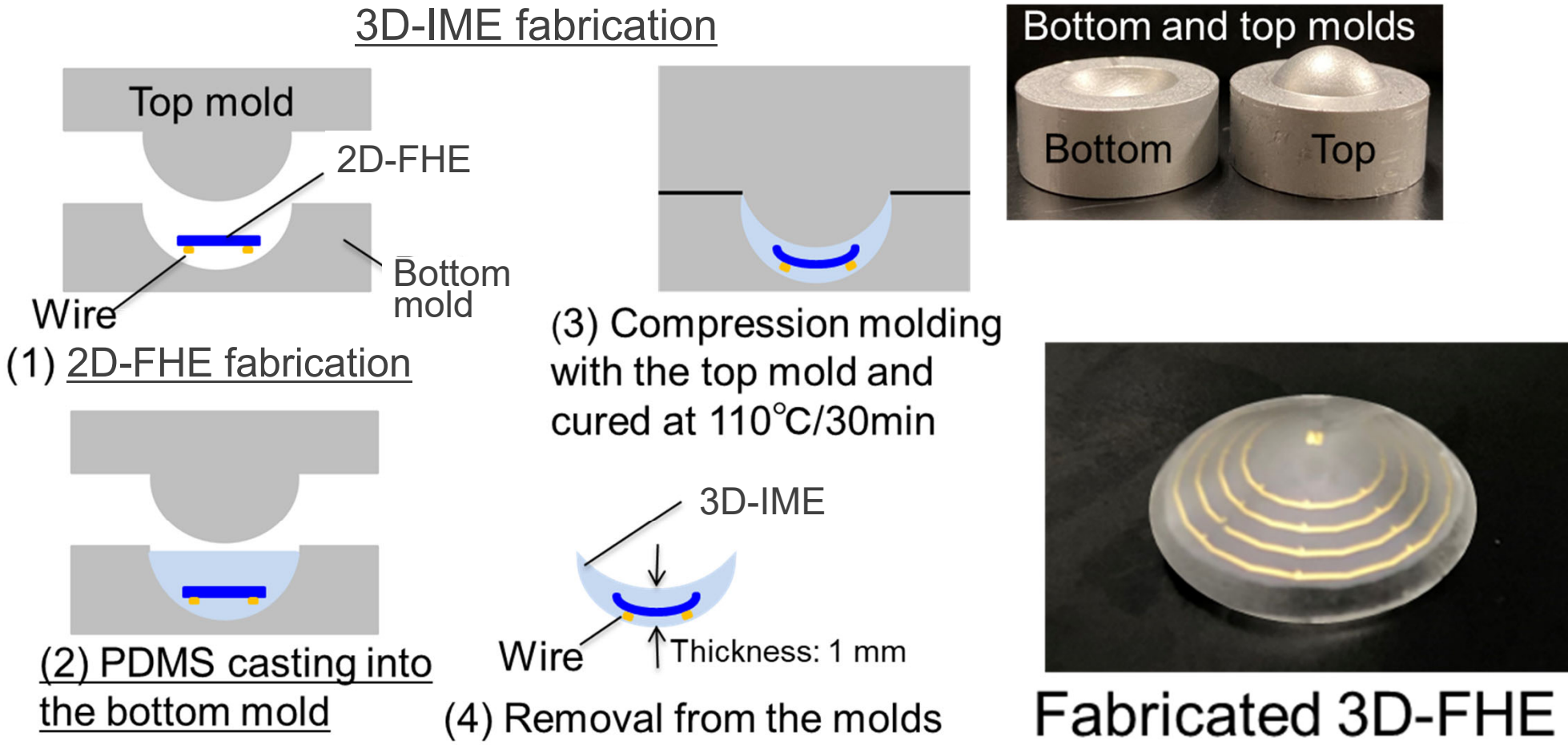


< Cross section>

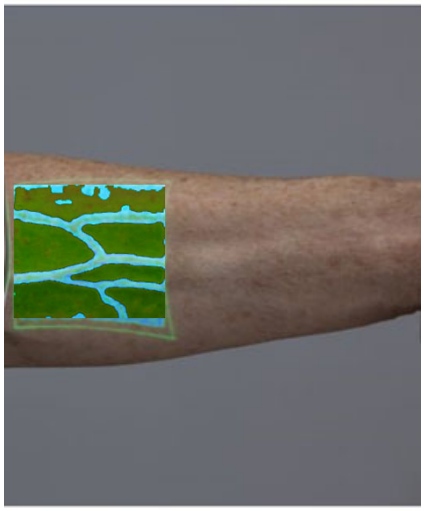




5. 3D In-Mold Electronics (IME) with Embedded Chiplet: Contact Lens-Shaped FHE by using Cast Re-molding



6. Smart Skin Display for Monitoring Pulse Wave, SpO_2, & Blood Volume



Expected image

Summary

- We have developed a technology for new flexible hybrid electronics (FHE) called Flexible FOWLP with small/thin/rigid monocrystalline chiplets ranging in thickness from 50 μm to several hundreds μm.

- Fine-pitch interconnects less than 10 μm were successfully formed on a large number of the Si chiplets embedded in PDMS and Hydrogel by FOWLP technologies.

- Stress Buffer Layer (SBL) can mitigate bending stress to give high bendability with a bending radius of 5 mm. PDMS can drastically reduce wafer warpage and die shift.

- The new FHE can be used for various wearable and biomedical applications requiring high-performance and scalable heterogeneous integration with fine-pitch interconnects.

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