i3 Microsystems Inc.

2-High Stacked Heterogeneous System-in-Package (HSIP) Modules Using Solder Assembly

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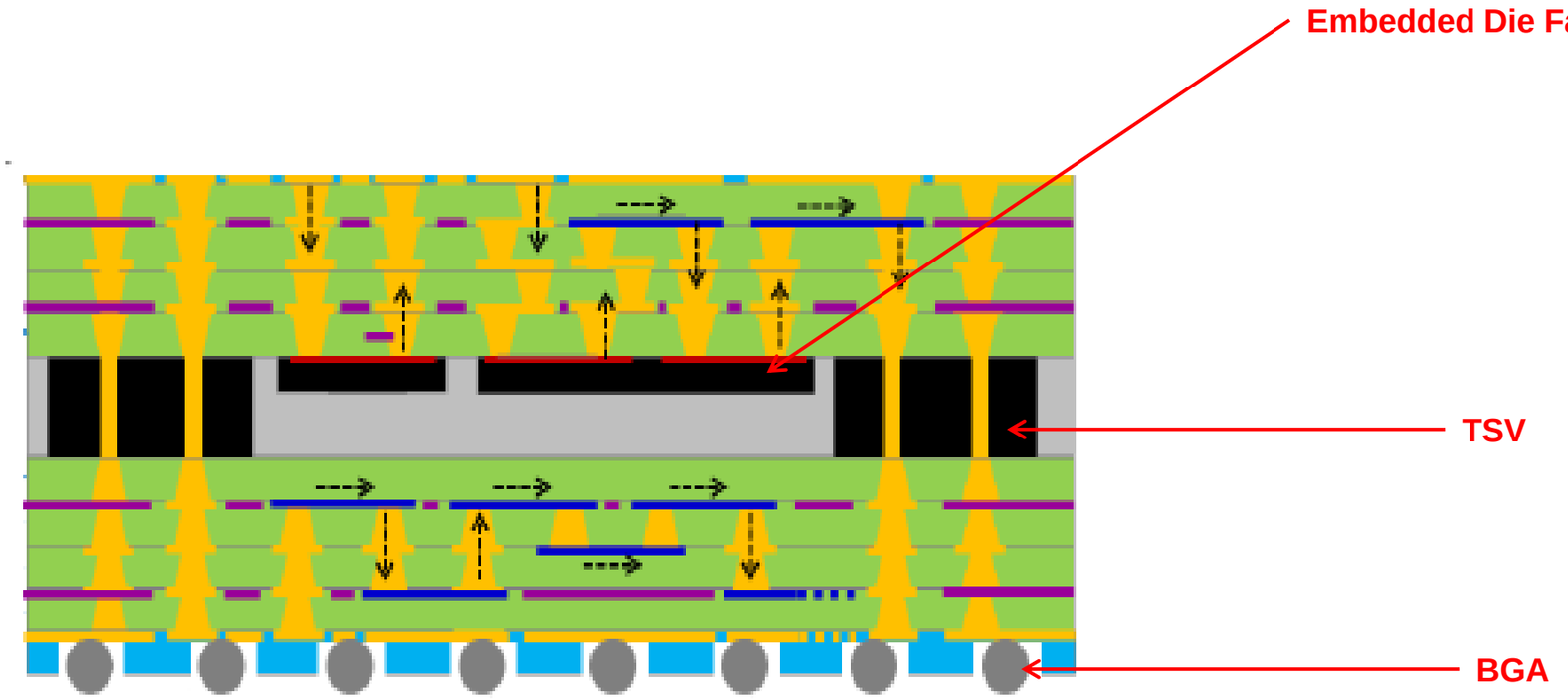
Device Packaging Conference
April 12-15, 2021

Outline

- Test Vehicle Design
- HSIP Module Build
- Results
- Discussion
- Conclusions
- Acknowledgements

Test Vehicle Design – Single Slice

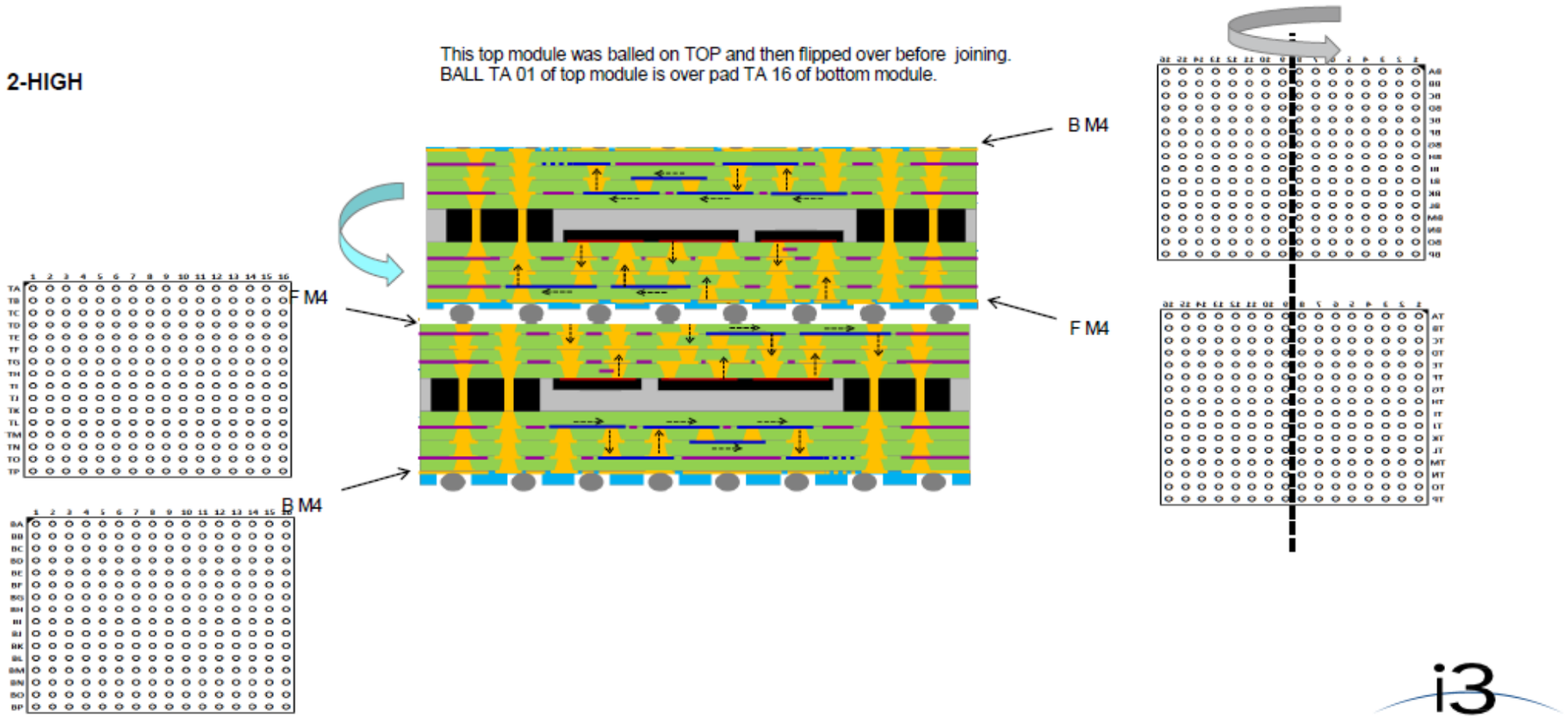


Test Vehicle Design – Double Slice

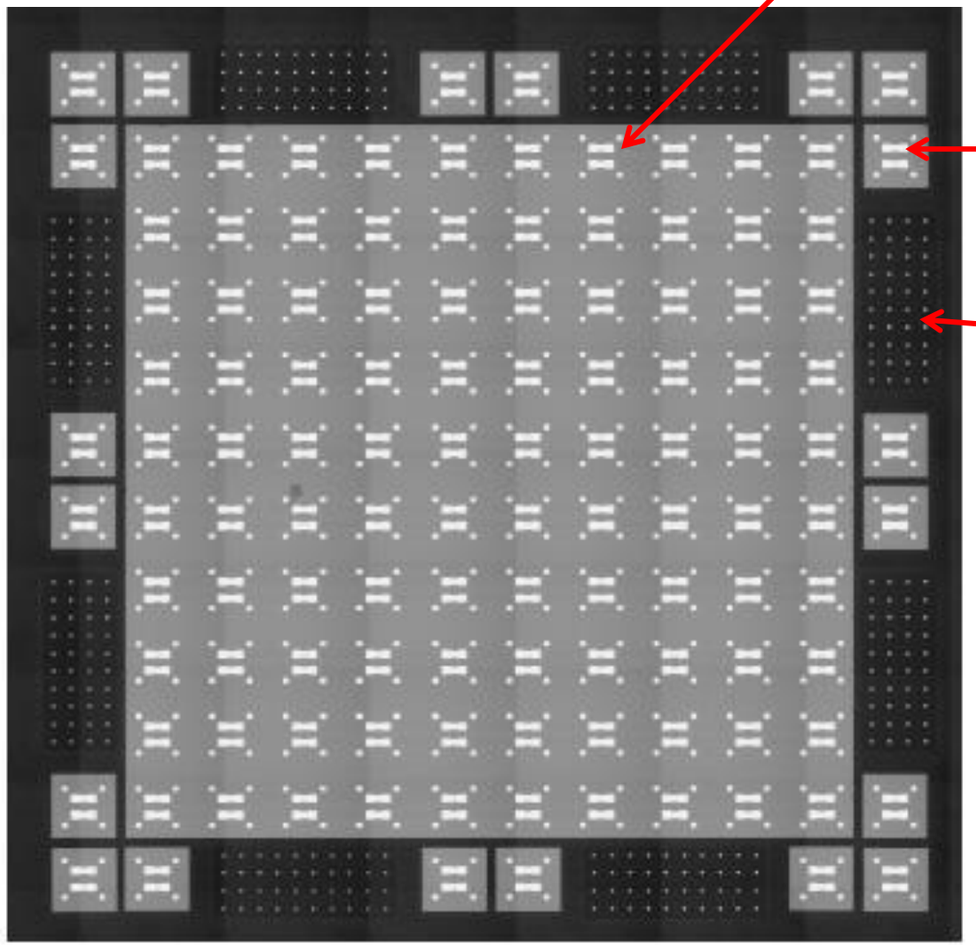
Need Fiducials and POD Notes to cover 1 high AND **2-HIGH** configurations

2-HIGH

This top module was balled on TOP and then flipped over before joining.
BALL TA 01 of top module is over pad TA 16 of bottom module.



RTV Molded Module Layout



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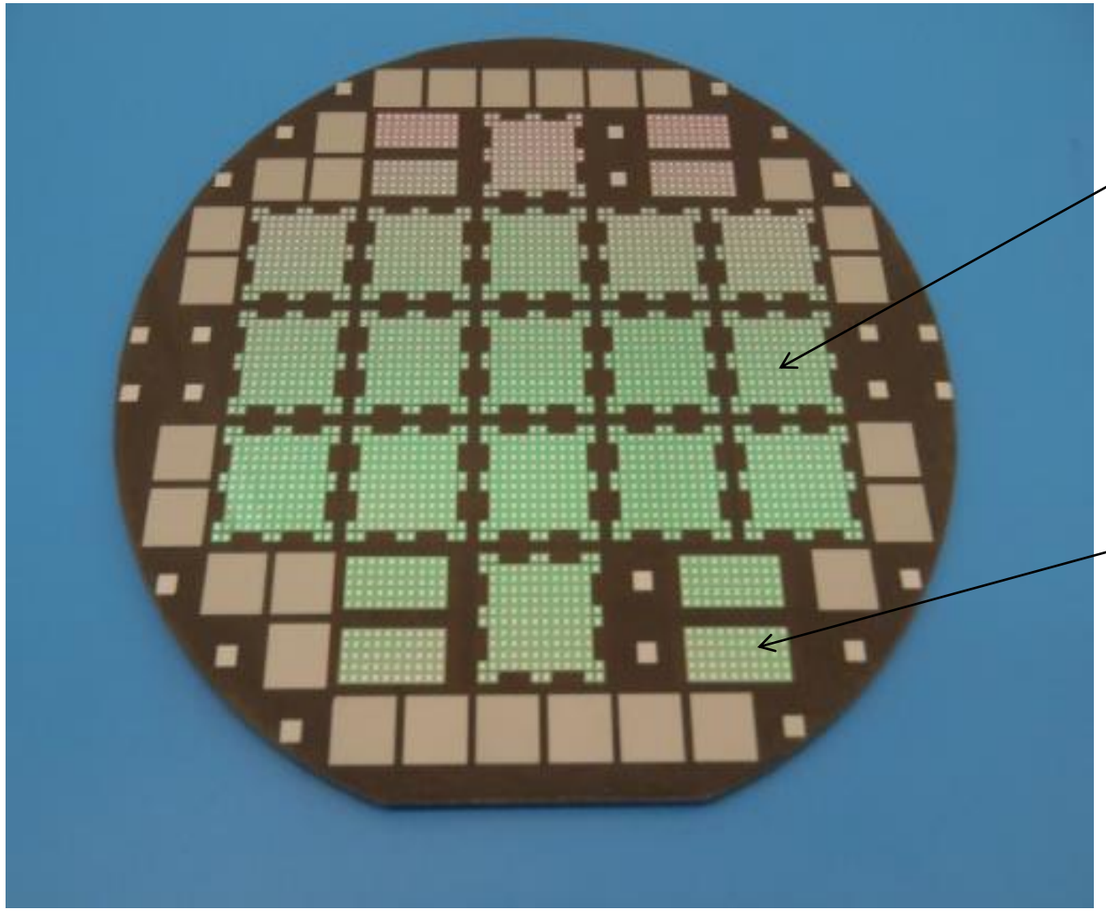
Embedded Core Layout



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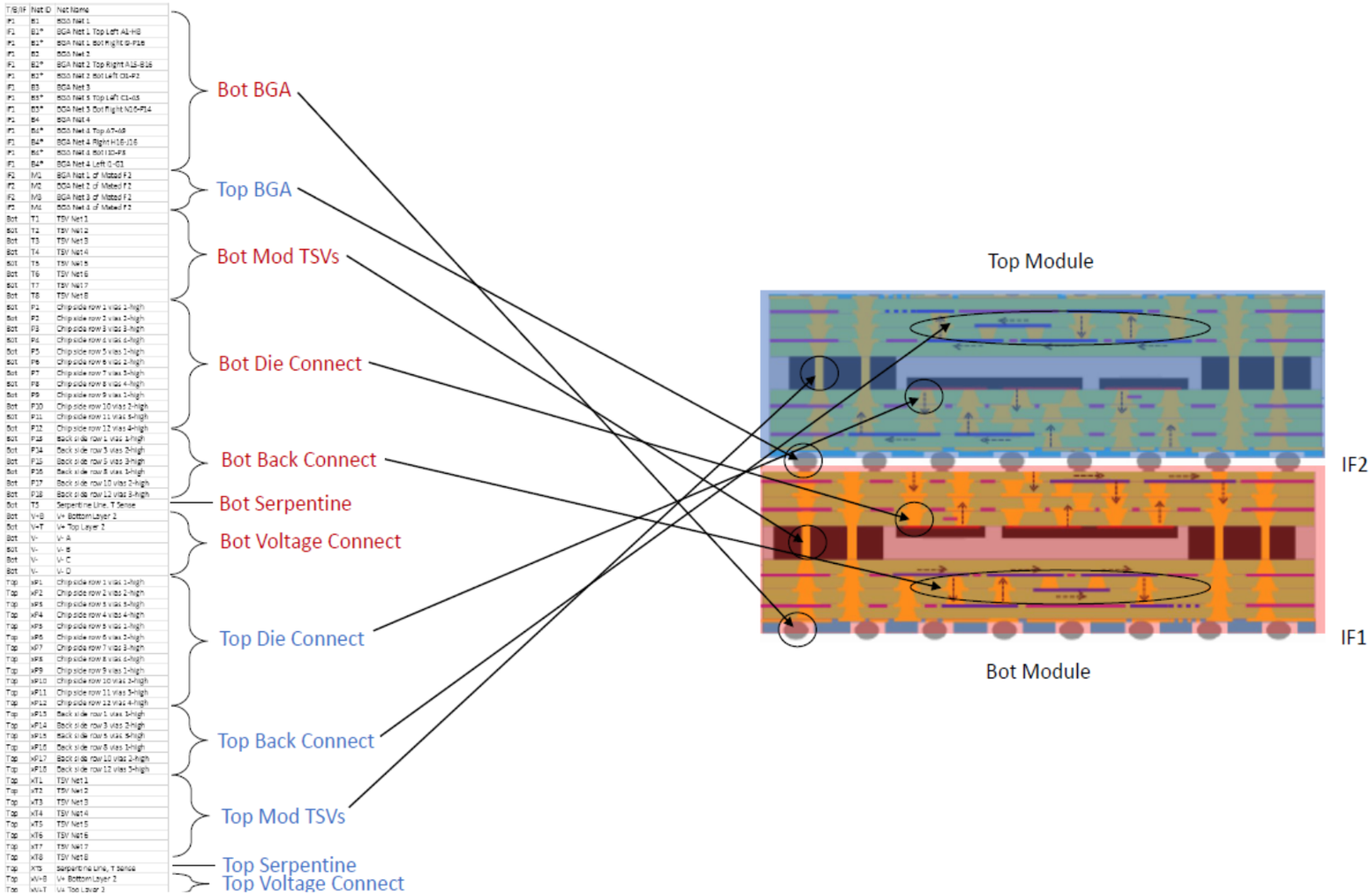
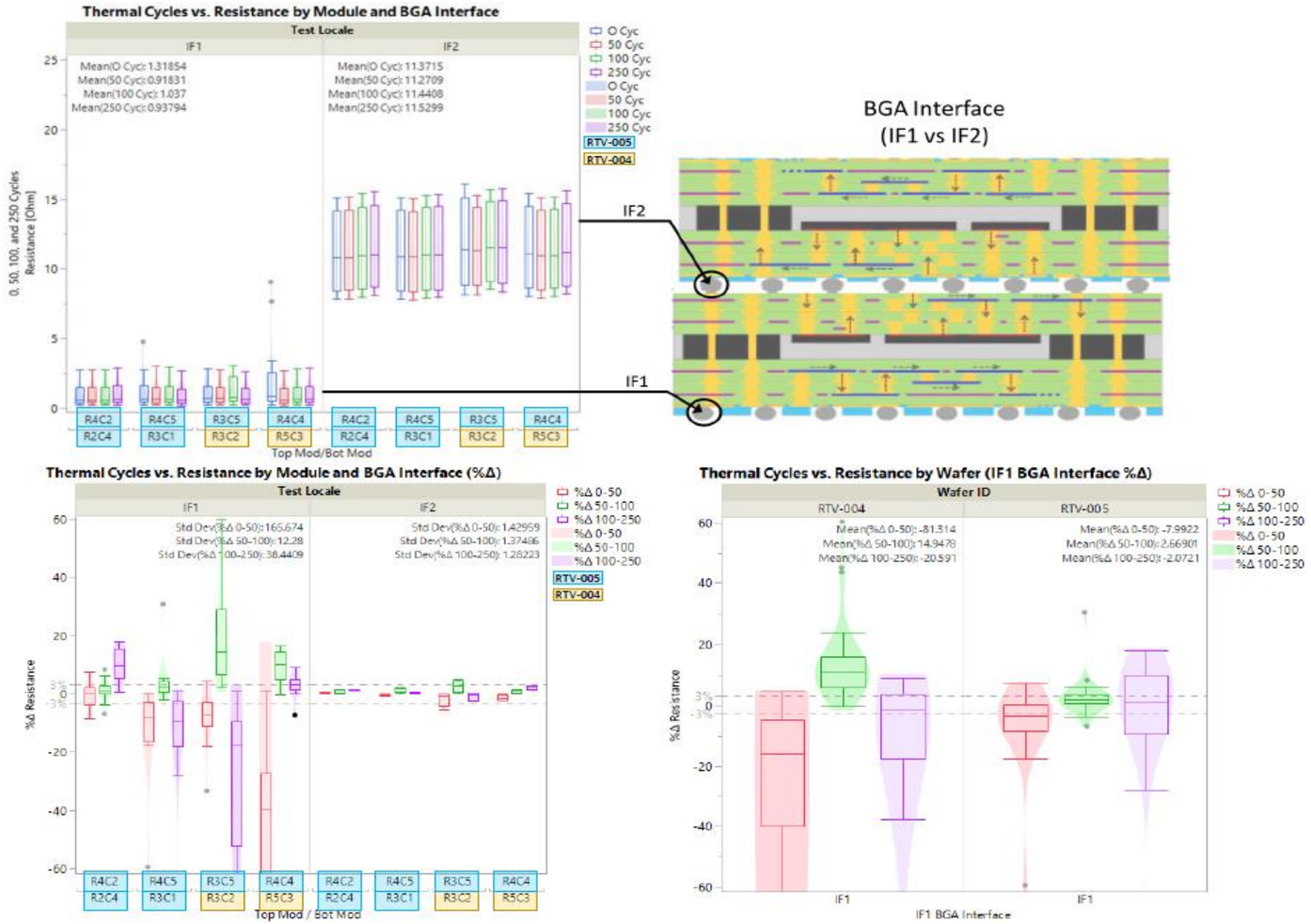
Test Vehicle Test Nets Grouping



4 Conditions for Reliability Testing

- BGA Interface (IF1 vs. IF2)
- TSV Interface (Top Module vs. Bottom Module)
- Internal Module Via Resistance (Top Mod Die Side Interconnects vs. Bottom Mod Die Side Interconnects)
- Internal Module Via Resistance (Top Mod Backside Interconnects vs. Bottom Mod Backside Interconnects)

Reliability data for BGA Interface (IF1 vs. IF2)



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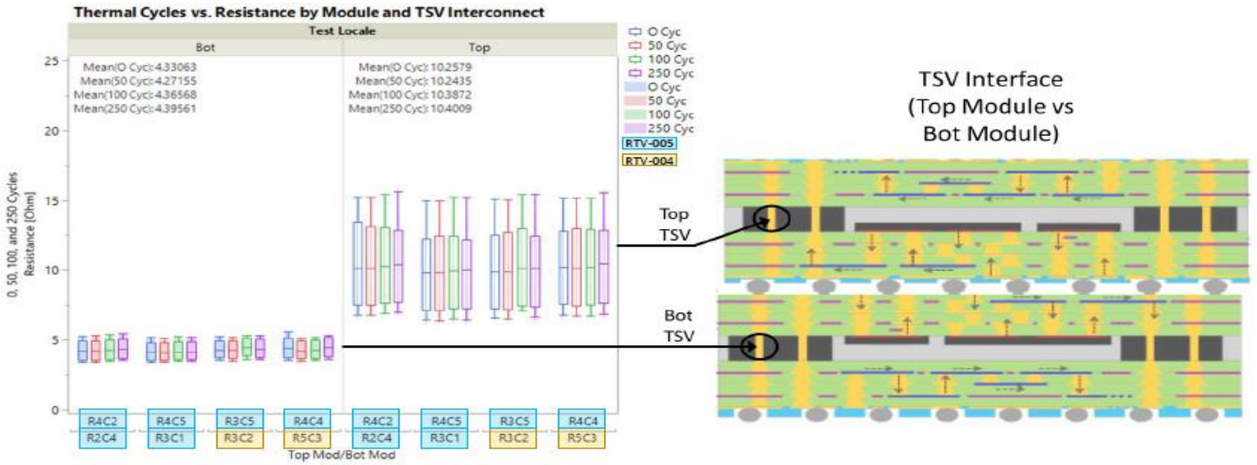
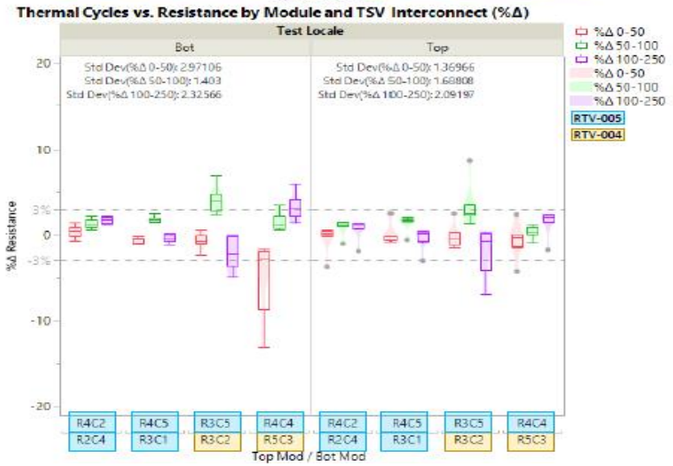
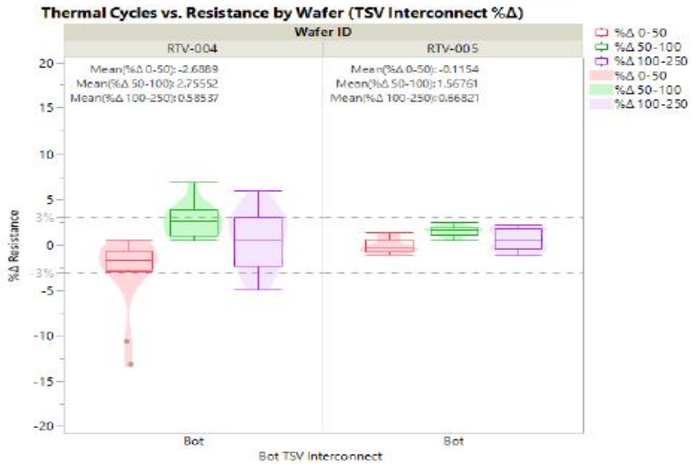
Reliability data for TSV Interface (Top Module vs. Bottom Module)







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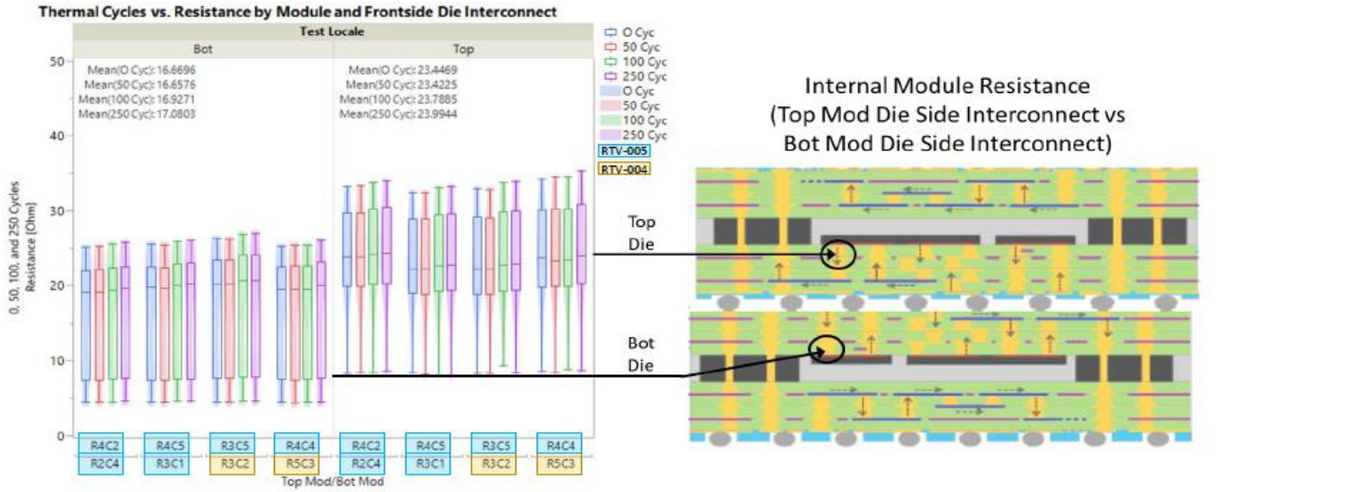
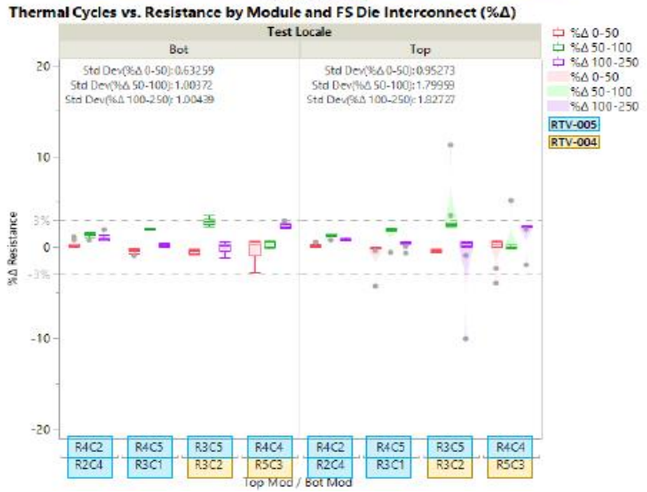
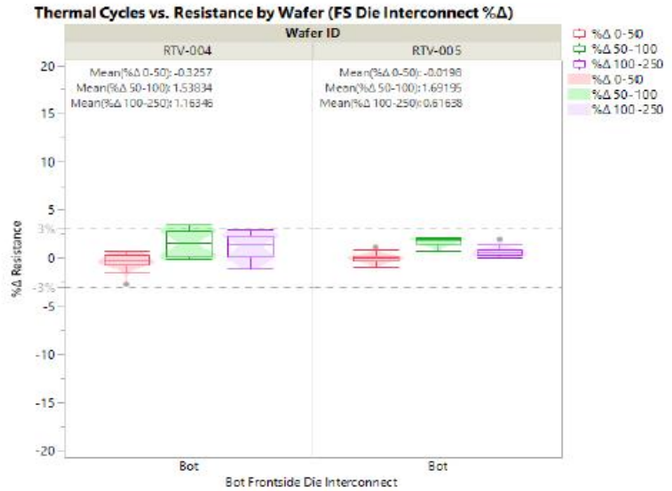
Reliability data for Internal Module Resistance (Top Module Die Side Interconnect vs. Bottom Module Die Side Interconnect)







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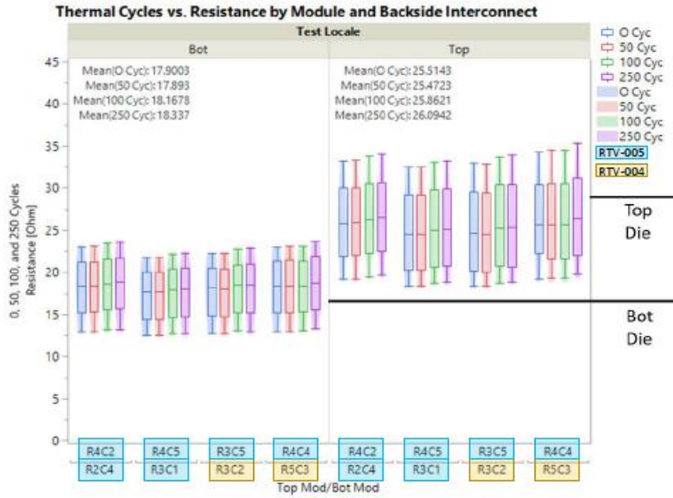
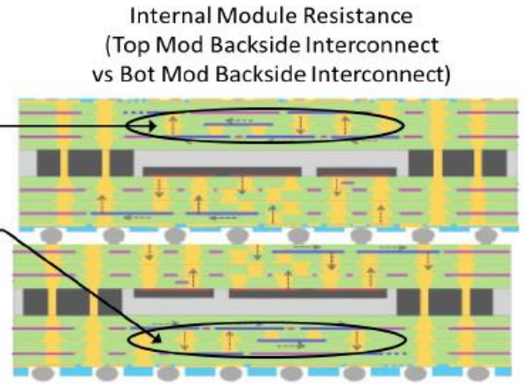
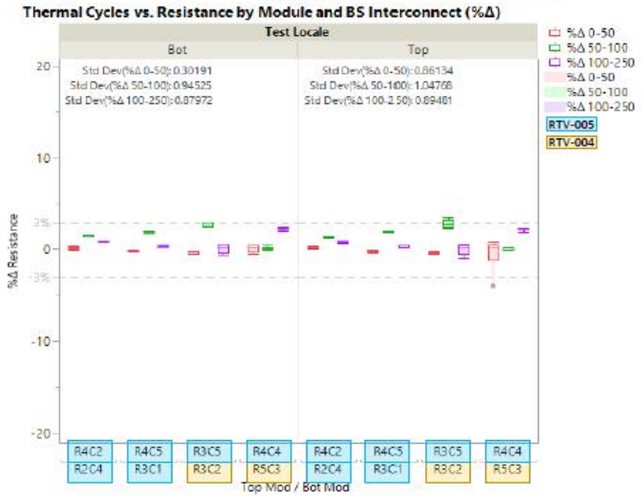
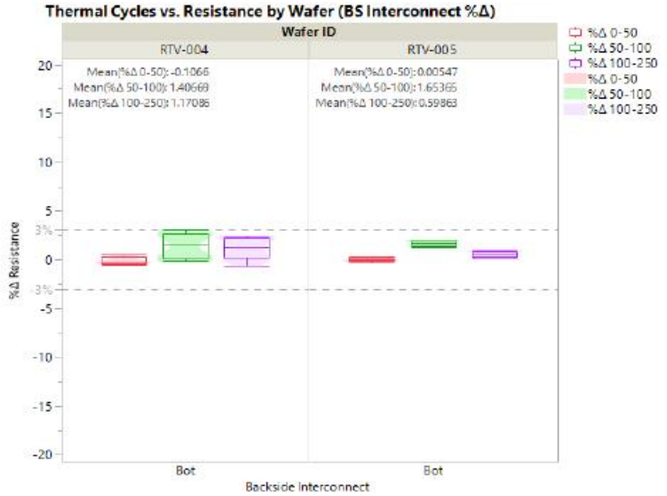
Reliability data for Internal Module Resistance (Top Module Backside Interconnect vs. Bottom Module Backside Interconnect)









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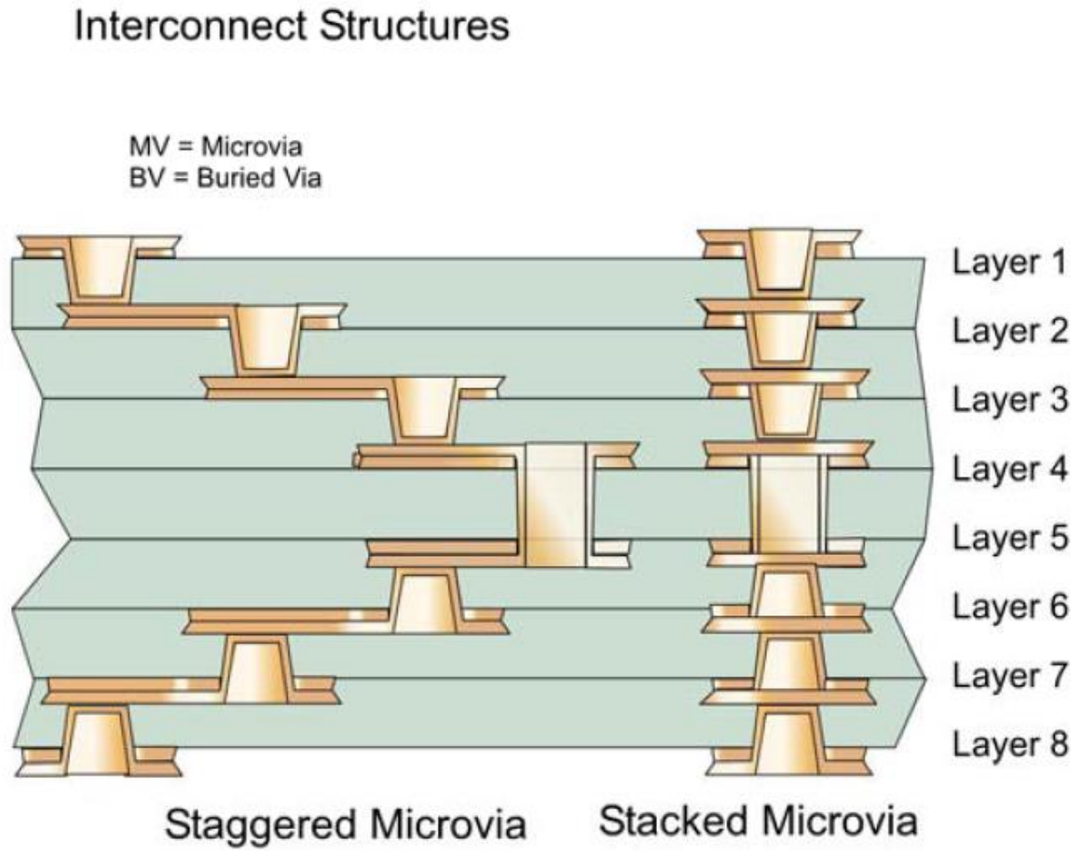
Microvia Structure



Discussion Highlights

- The TSV resistance variation of the TSVs in the top is less than that of the bottom module.
- The staggered via design buildup structures on both top sides of the module are very reliable.
- The reliability reveals that the soldered interconnected between the top module and the bottom module IF2, is much more reliable than then BGA IF1.
- Modules built using the RTV-04 process have a much larger resistance variation than those using the RTV-05 process.

Conclusions

- HSIP technology offers tremendous flexibility to accommodate different die types, sizes to produce a high performance high density multi-chip package using FOWLP.
- Process capable to produce a flat HSIP with good electrical circuit when using RTV-05 conditions (higher cure temperatures and shorter bake times on a new equipment set).
- Thermal cycling -29 to 85C, 2 cycles per hour, shows that modules subjected to a qualified BGA attach process are showing good reliability up to 250 cycles. Testing will continue to 1000 cycles and beyond.
- Future work will concentrate on stacking modules and further testing under standard JEDEC conditions (T/C 0 to 100C and -40 to 125C).

Acknowledgements

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- Larry Black, Program Mgr.
- Chuck Baab, Process Engr.
- Kevin Knadle, TTM Reliability Engr.

Thank You!

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