UNIVERSAL IOT SENSOR PLATFORM BASED ON A FOWLP RDLFIRST APPROACH

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Outline

- Motivation
- Package Concept
- Process Flow & Process Development
- Process Challenge: Warpage
- Demonstrator Manufacturing
- Evaluation & Test
- Summary & Outlook

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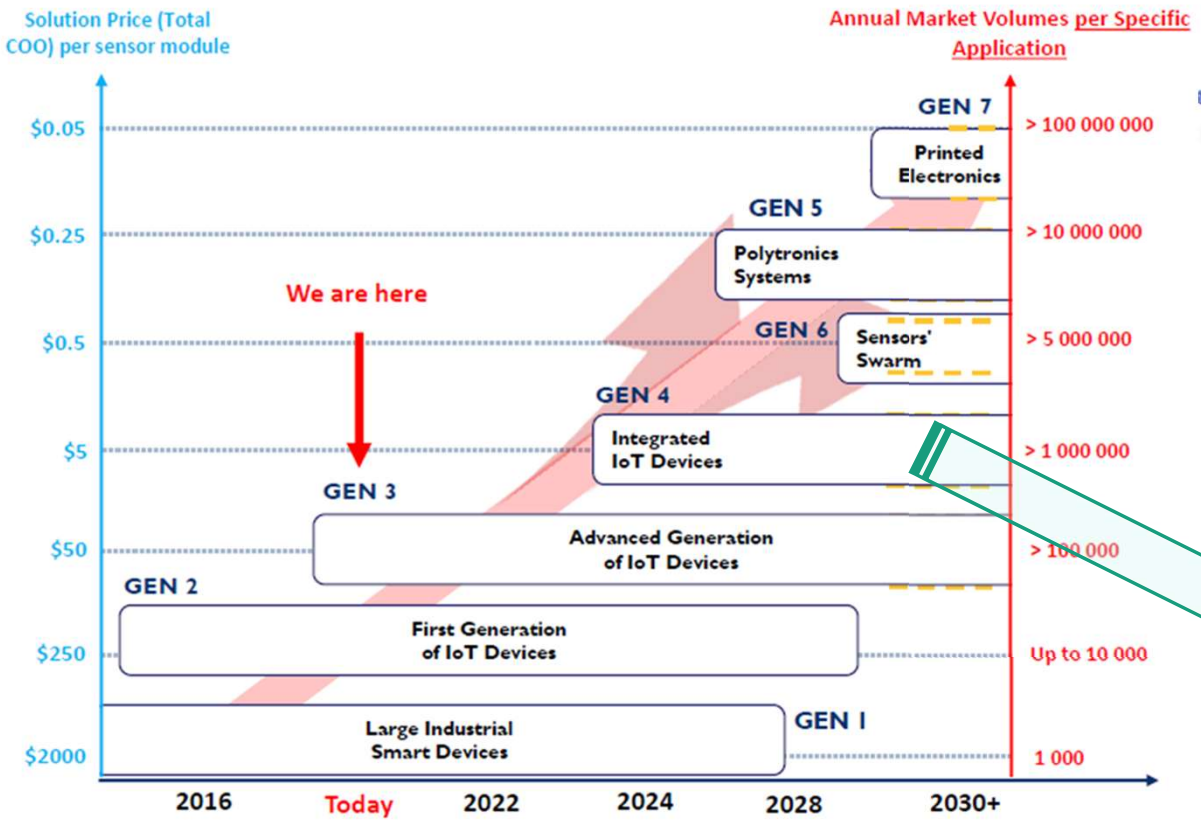
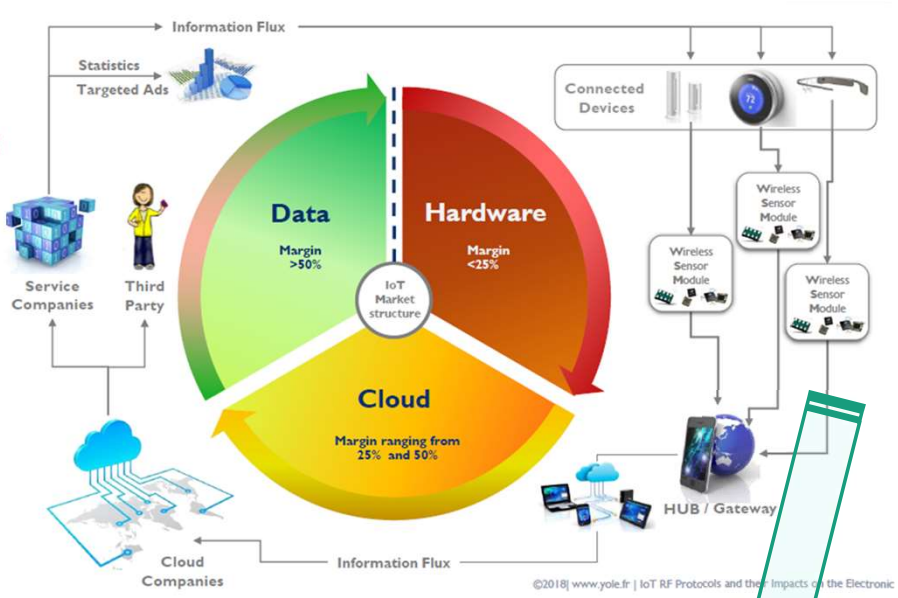
Motivation Universal Sensor Platform for IOT





GEN 4 needs higher integration level

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PACKAGE CONCEPT

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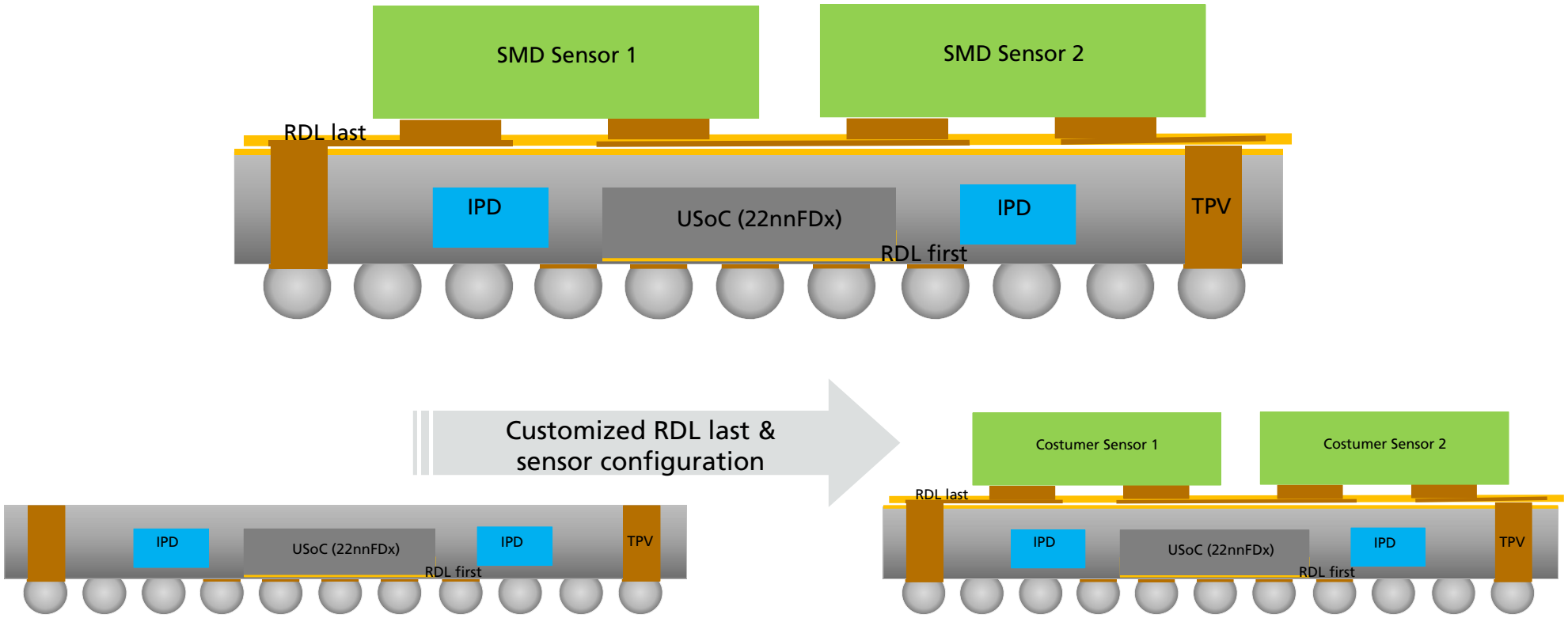
Universal Sensor Platform (USeP) – Package Concept



Standard USoC Package (RDL first)

Customized USiP Package (RDL last)

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PROCESS FLOW

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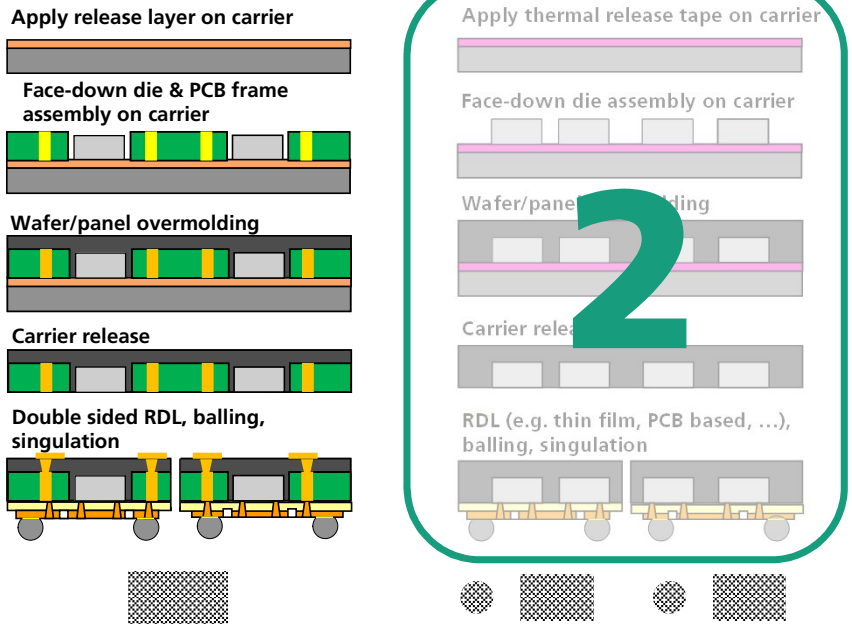
FOWLP & PLP Process Flow Options

RDL last

face-down

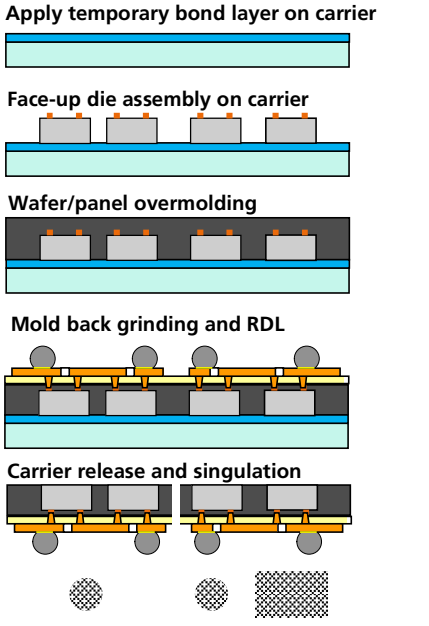


„eWLB“ „RCP“

SAMSUNG ELECTRO-MECHANICS

Infineon, Panel Level Packaging Consortium, nepes, Amkor Technology, JCET STATSChipPAC, Powertech Technology Inc.

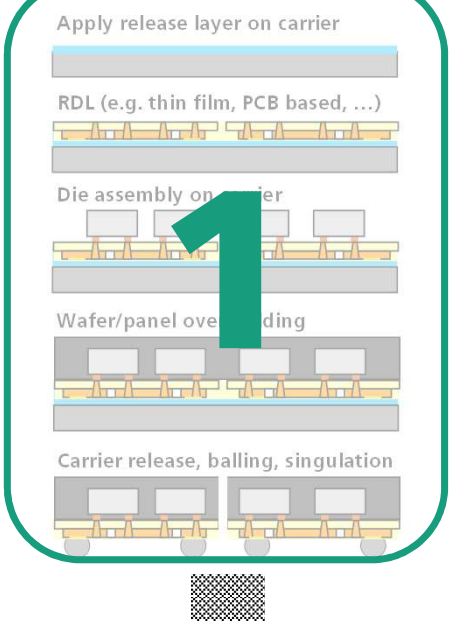
face-up



„InFo“ „M-Series“

tsmc, Deca Technologies, SPIL, ASE GROUP

RDL first



Unimicron 欣興電子

SAMSUNG ELECTRO-MECHANICS

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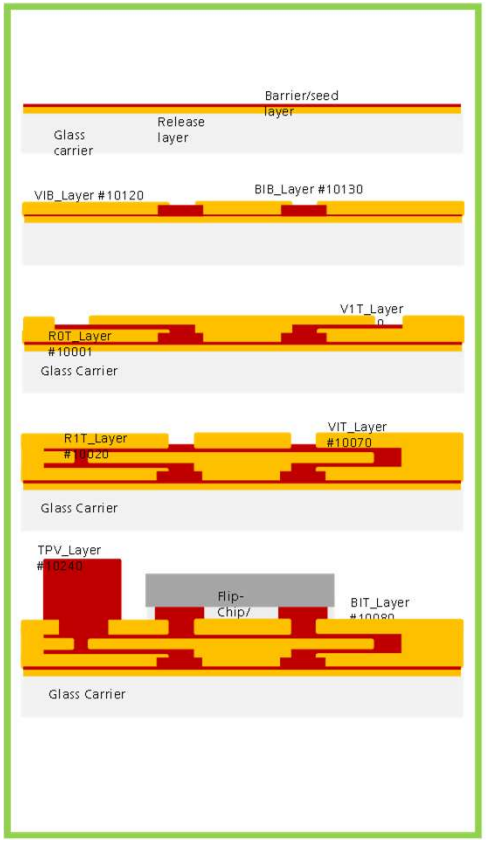
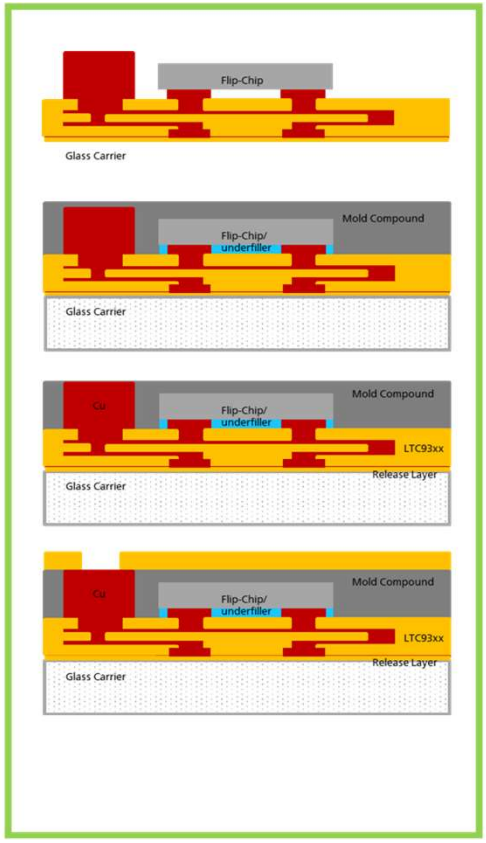
USiP Process Flow

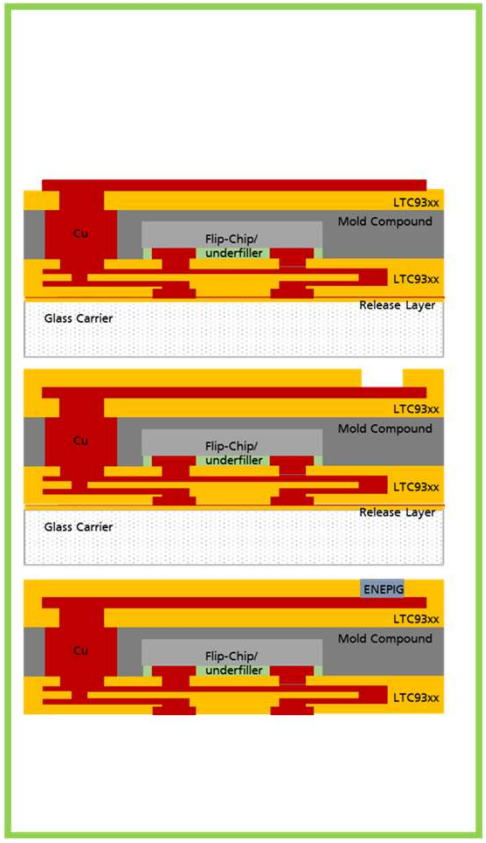
RDL-1st Process/ D2W-Bonding



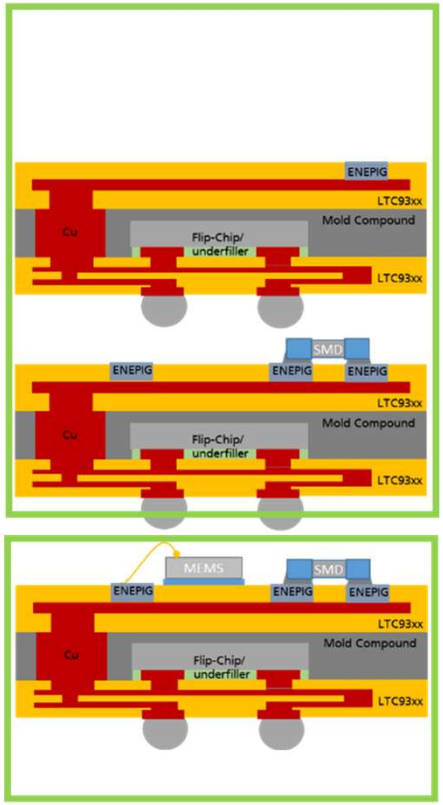
IPD/ Wafer Mold/ TPV open



Top Side RDL/ Laser Release + Clean



SBA/ Dicing/ SMD-Assembly



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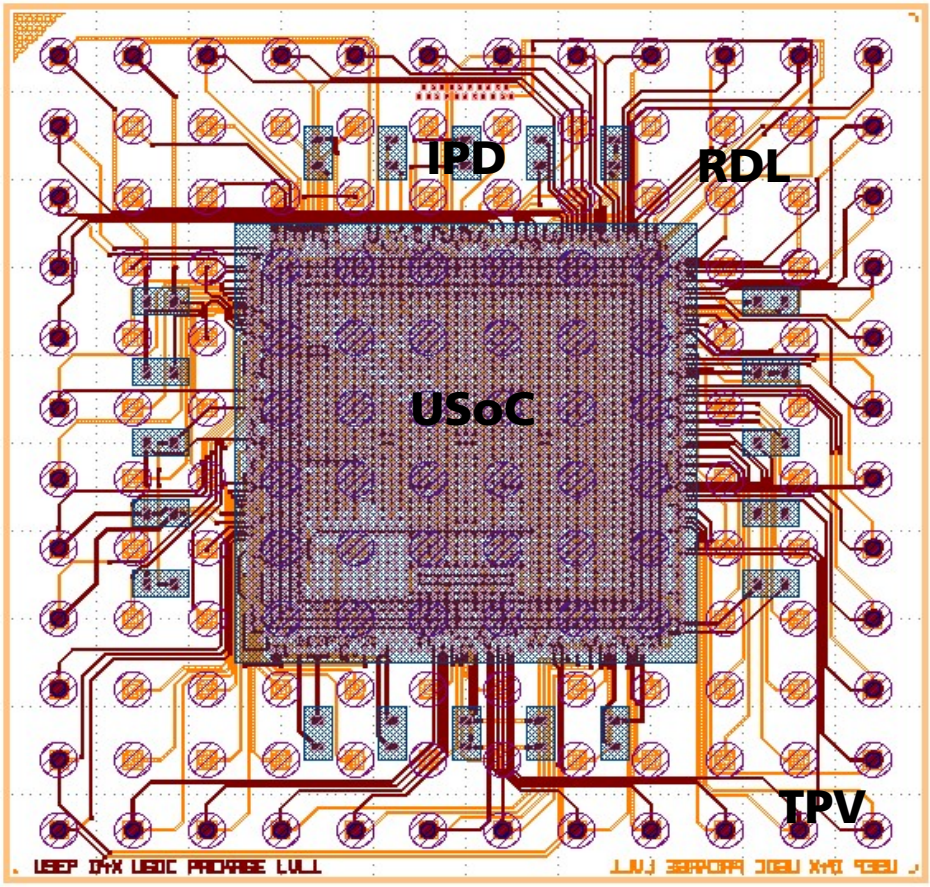
Demonstrator Design

Design Parameter

- Flip Chip (USoC)
  - Die size/ outline 5000 µm x 5000 µm
  - Die thickness 100 µm
  - µ-pillar diameter/ pitch 60 µm/ 100 µm
  - I/O-# per die ~2200
- RDL first
  - Package size/ outline 10000 µm x 10000 µm
  - Package thickness ~200 µm
  - RDL-stack 2 RDL-layer
  - FC-land diameter/ pitch 60 µm/ 100 µm
  - TPV-diameter/ pitch 150 µm/ 800 µm
  - SBA-Land diameter/ pitch 400 µm/ 800 µm
  - Solder ball diameter 500 µm
  - Package I/O-# to (L2/L3) 44/ 144



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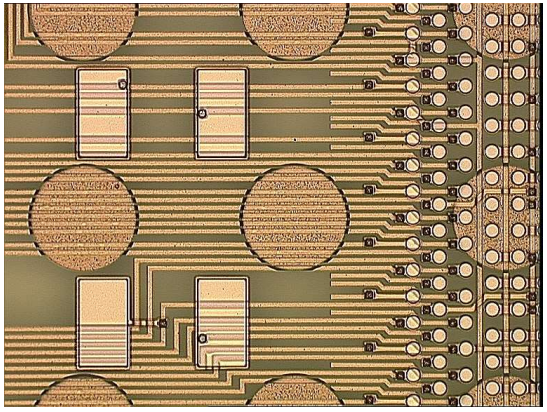
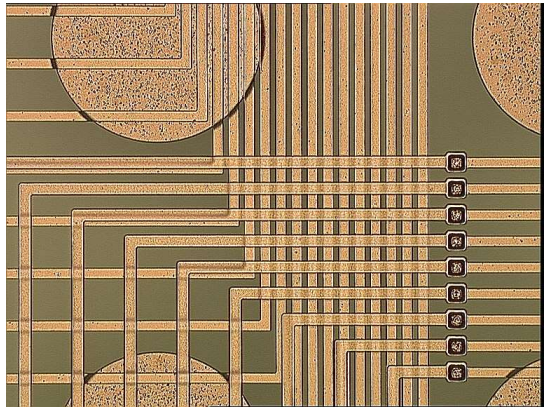
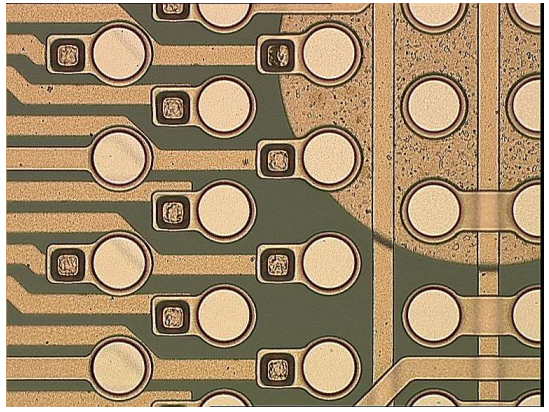
Multi-Layer Polymer RDL first

Process development/ modification/ evaluation of multi-layer polymer RDL

- Spin on coating of release layer material
- Sputter of UBM layer/ layer variation on glass carrier coated with polymer materials
- Evaluation of via in via designs for vertical connection
- Application of advanced resist material for well defined Cu-pattern
- Variation and adjustment of FC-land pad construction
- Integration of dryfilm 2x lamination/ exposure/ development for large Cu pillar (TPV)
- Improvement of Cu-pillar plating process
- Improvement/ adjustment of final wet clean steps (BS and FS)







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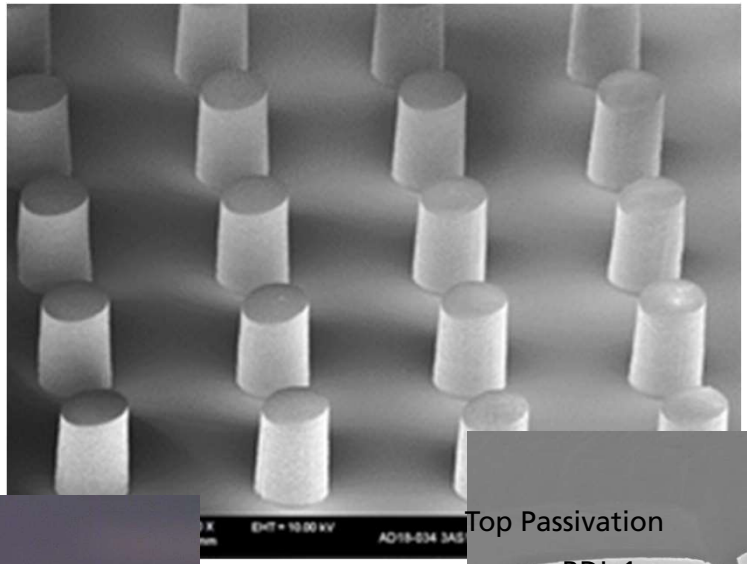
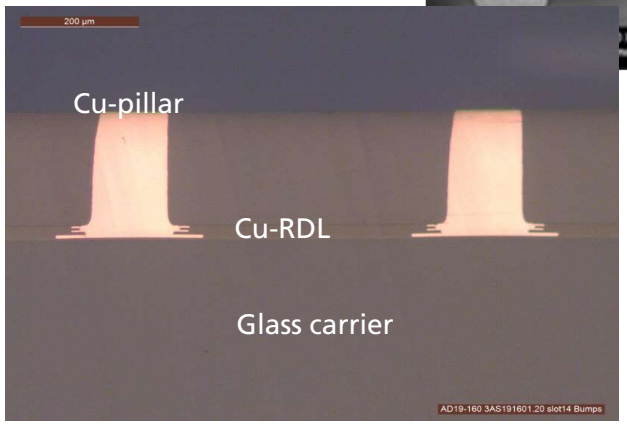
Tall Cu-Pillar Process for Through Package Vias (TPV)

Process flow "Tall Cu-Pillar"

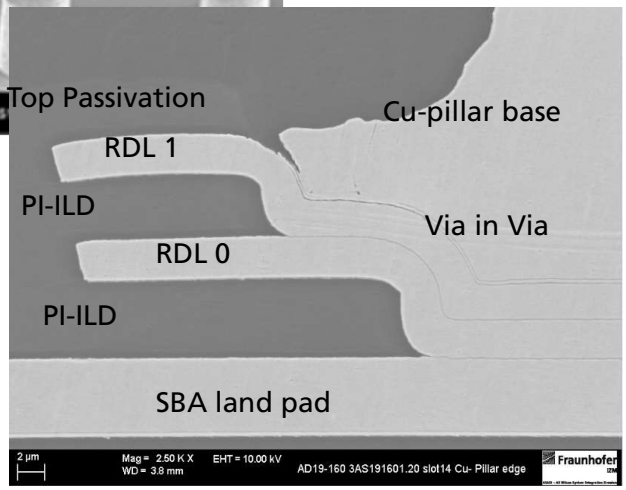
- Application of adjusted UBM layer stack for Cu-Pillar plating
- 2x dryfilm lamination to achieve resist thickness of > 200 µm
- Modification of Cu-pillar plating process
- Implementation of flycut after plating
- Modification of resist strip and UBM wet etch steps to secure clean surface of RDL-1st substrate



Cu-Pillar array
Pitch: 800 µm
Height: 200 µm
Diameter: 150 µm



X-section through Cu-Pillar post UBM wet etch



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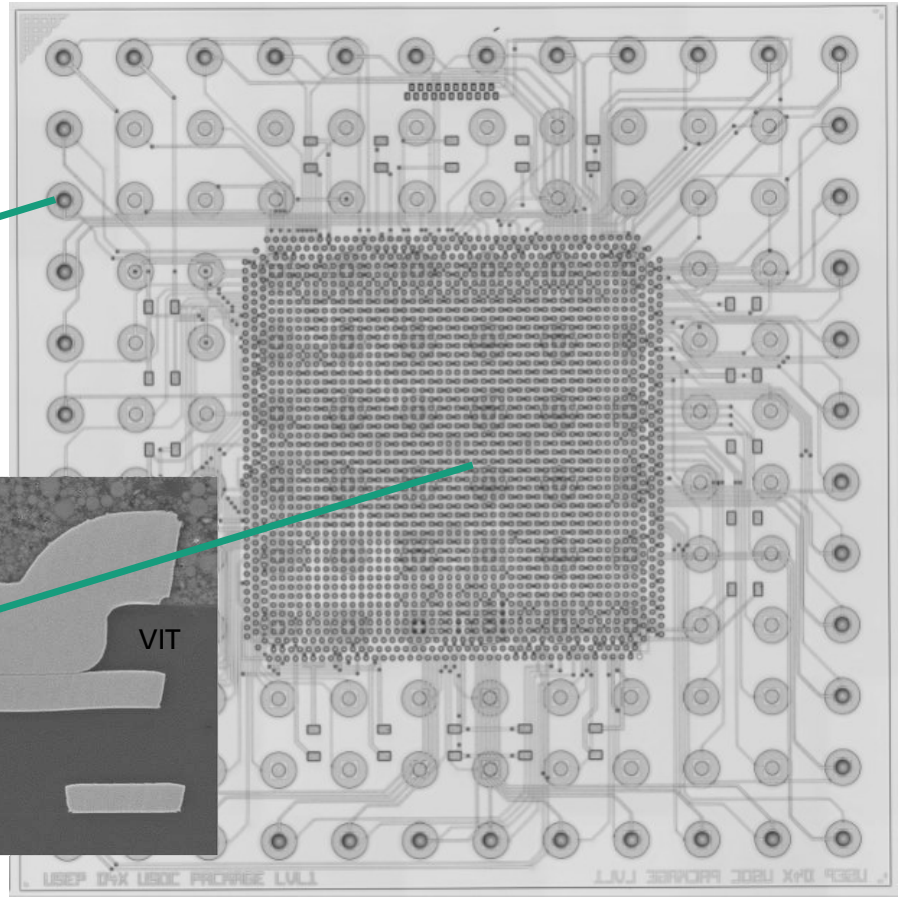
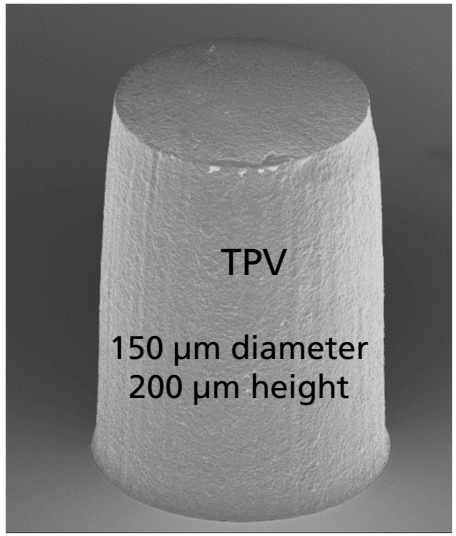
RDL first Substrate

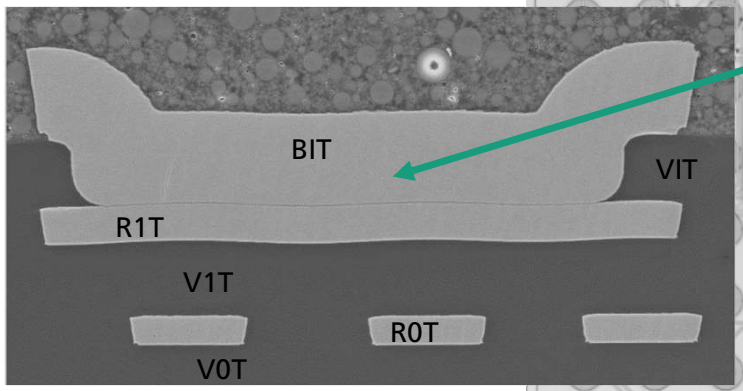
High resolution image (AOI) of final RDL first substrate for USEP demonstrator



SEM: Large Cu-Pillar as through package via



X-section: RDL first stack FC pad, 2nd RDL-layer



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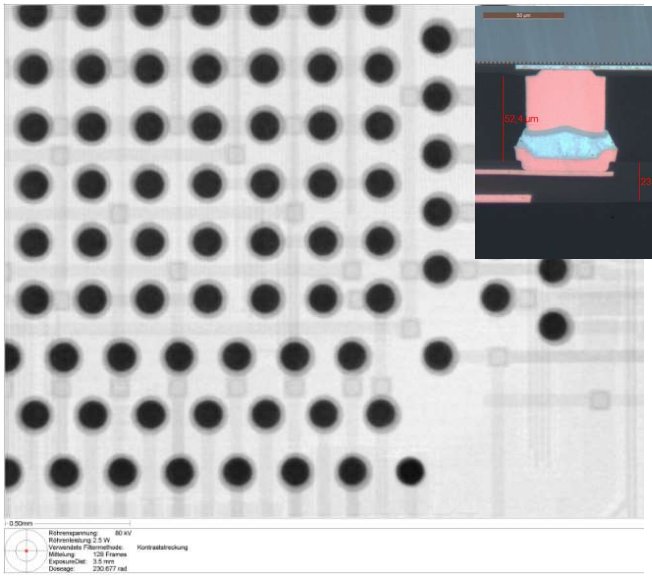
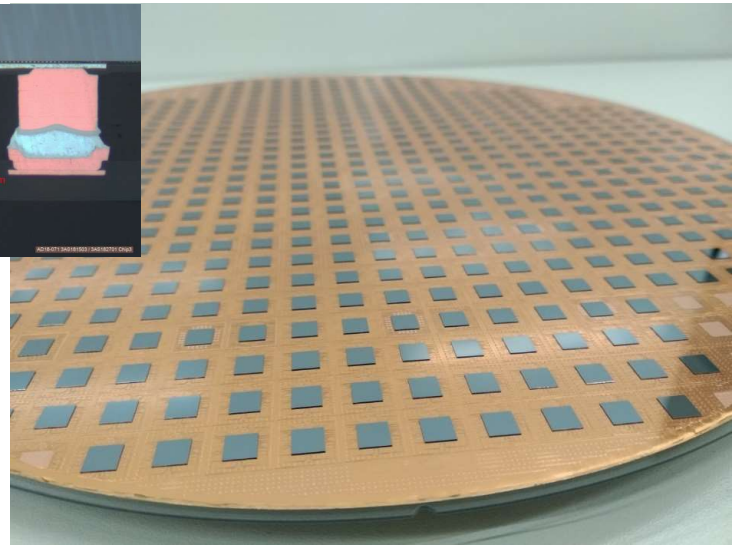
USoC and IPD Assembly on RDL first Substrate

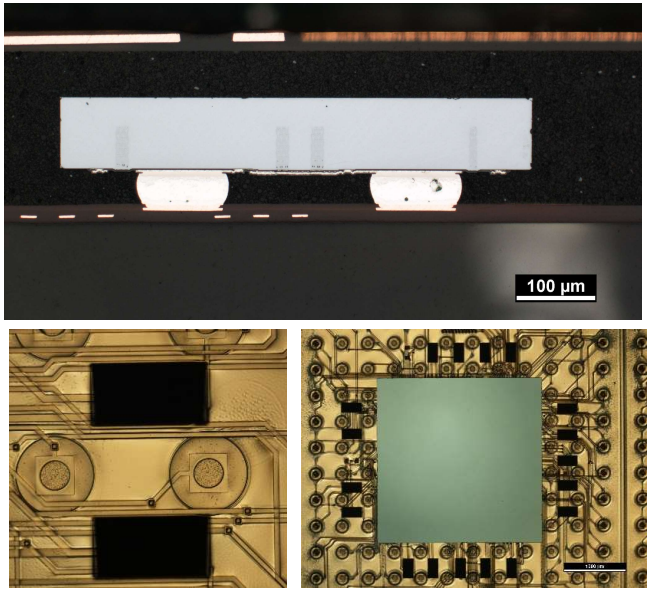
- FC assembly of USoC and IPDs on RDL first substrate
- Bumped IPD capacities selected due to small form factor for extreme thin package (~200 µm)



X-Ray image of RDL first substrate and FC interconnects, flip-chip interconnects 100 µm pitch/ 50 µm diameter/ 50µm height



300 mm RDL first substrate assembled with SOC. The substrate contains the pattern for about 630 packages



IPD assembly on RDL first substrate, selection of pre-bumped IPD components

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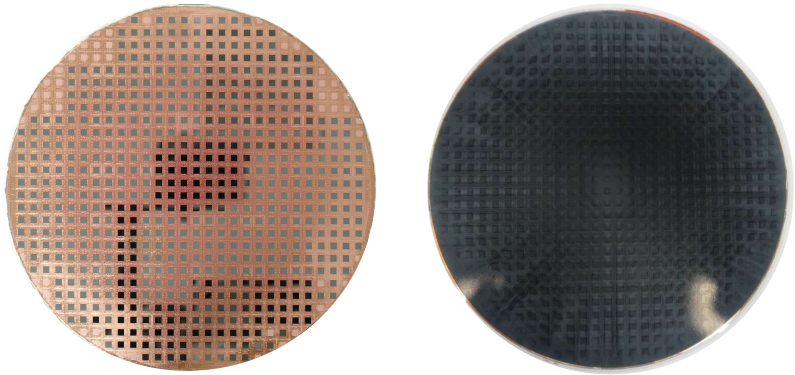
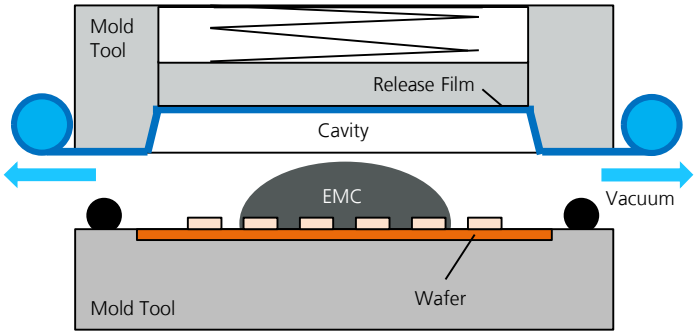
Compression Molding for Wafer Encapsulation

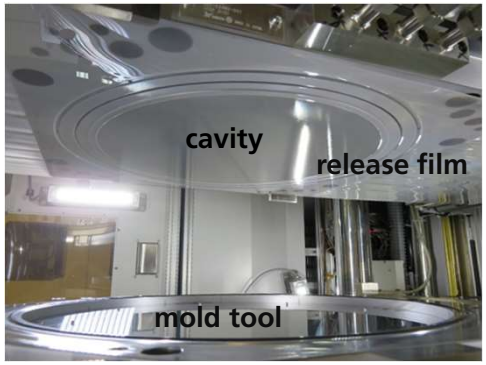
- Wafer encapsulation by compression molding
- 293.5 mm mold cap on 300 mm wafer size
- Use of liquid epoxy molding compound (EMC)
- Evaluation of molded underfill (MUF) – underfilling and overmolding in one process step



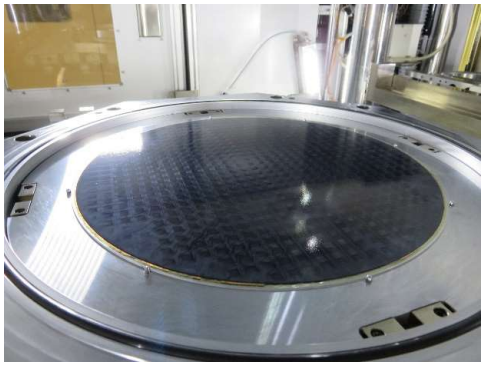
RDL first wafer before and after compression molding



compression mold principle



300 mm compression mold tool



molded RDL first wafer in compression mold tool

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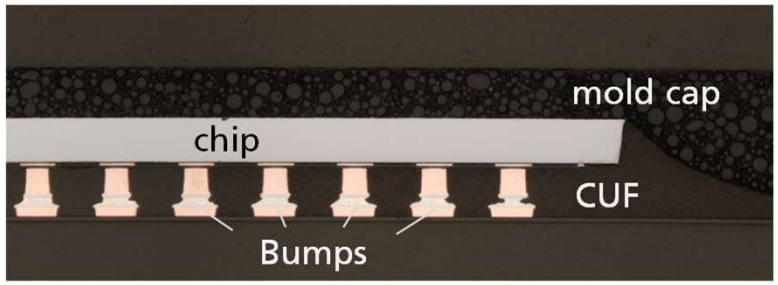
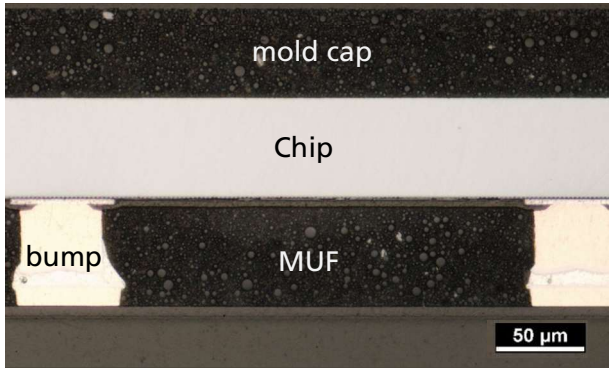
Compression Molding for Wafer Encapsulation

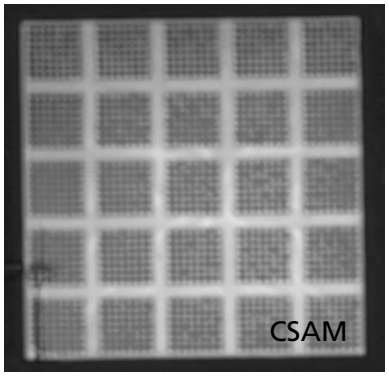
Capillary Underfill (CUF)



- Capillary underfill applied and cured before compression molding
- Additional process step
- Allows overmolding with EMCs with larger filler particles

Molded Underfill (MUF)





- Underfilling and overmolding in one process step
- Need for EMC with fine filler particles
- Void free underfilling and overmolding could be successfully demonstrated

➢ **Selected for demonstrator manufacturing**

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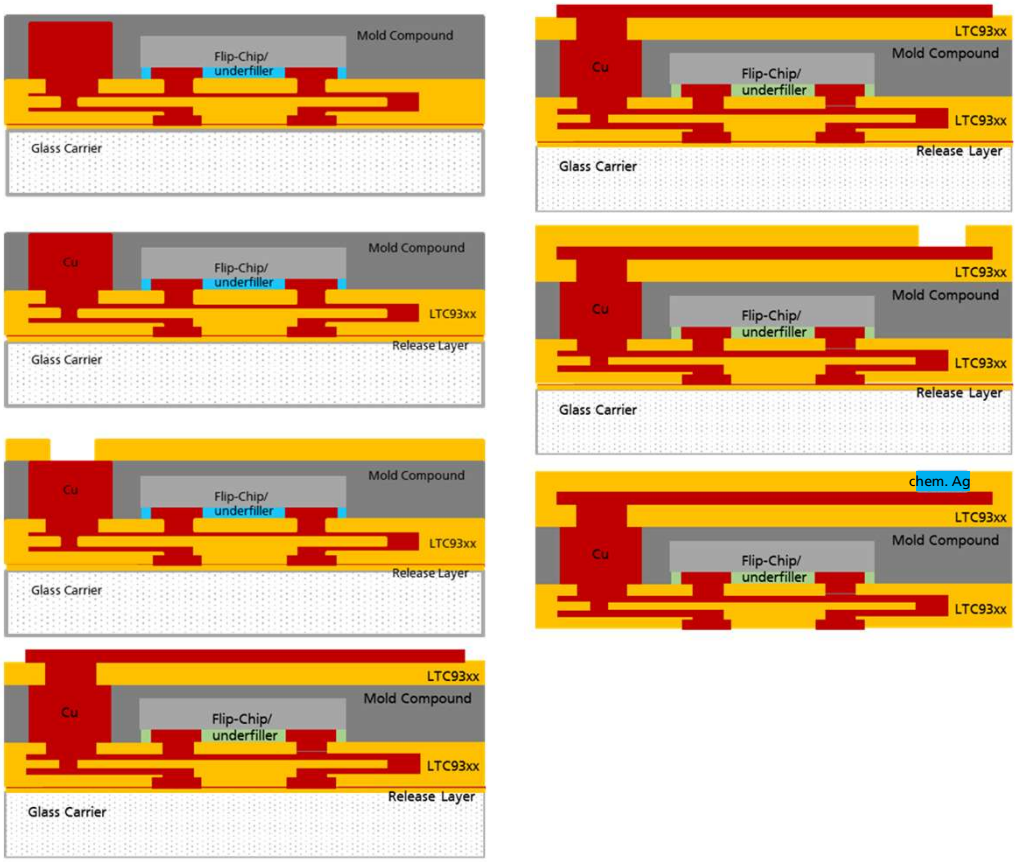
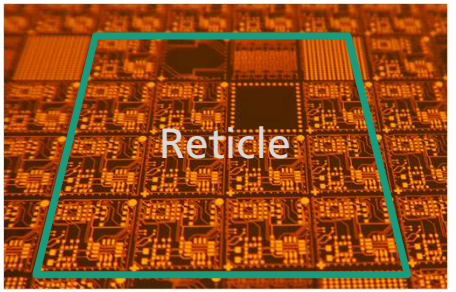
Process Sequence for RDL last and release of balling pads

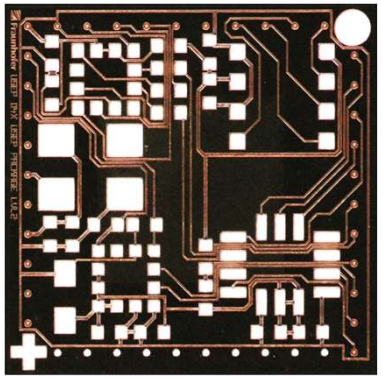


Process Flow

- Mold grinding
- PI-application, lithography mask, PI-cure
- Deposition of TiW/Cu (Barrier/Seed)
- Dry resist application, lithography mask
- Copper-ECD (8µm) and resist strip & plasma clean
- PI-application, lithography mask, PI-cure
- Electroless Ag deposition
- Laser release of glass carrier clean of laser release residue
- Wet etch of Ti/Cu seed layer on back side to release the balling pads

Top RDL





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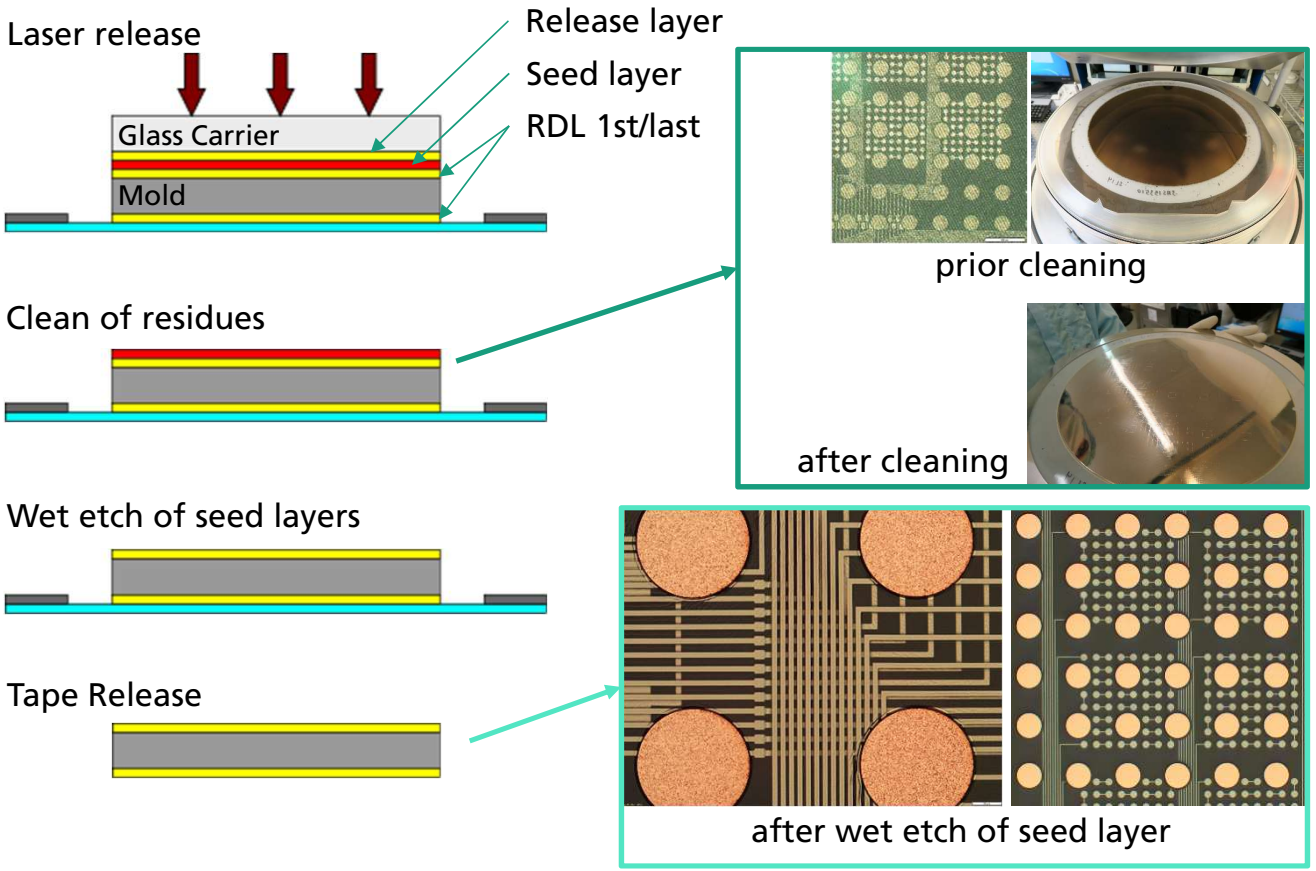
Carrier Release and Cleaning (Handling on Film Frame)



- After the wafer is released by laser debonding, the residues are cleaned by a combination of wet and dry etch chemistry (all processing is done on film frame to protect the top RDL); the process sequence is the following:
  - Laser debond
  - Wet and dry etch clean of release layer residues
  - Wet etch of seed layers
  - Tape release by UV irradiation
- For better handling on film frame, the mold wafer should exhibit a very low warpage which realized by the right amount of mold vs. Si and a symmetrical RDL layer setup

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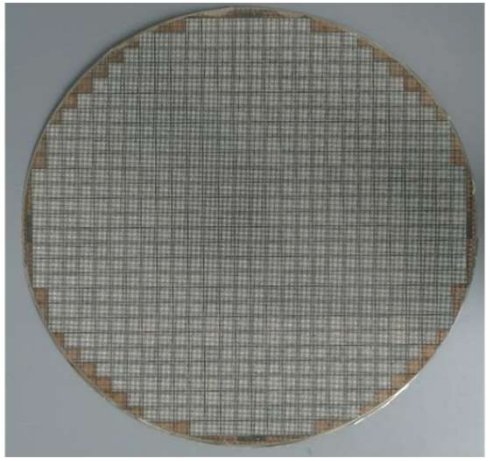
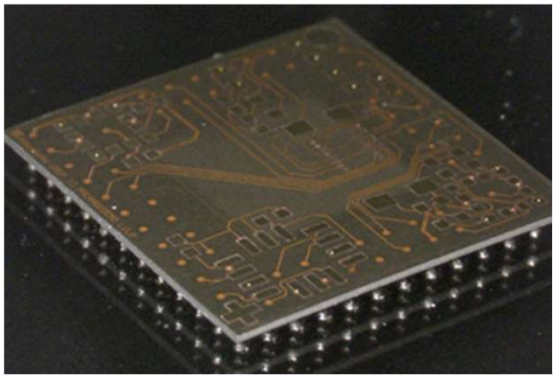
Wafer Balling & Dicing

- Wafer Balling on 300 mm wafer size and 200 µm wafer thickness
- Balls: SnAgCu, d = 500 µm
- Process flow:
  - Printing of tacky flux
  - Ball drop through stencil
  - Reflow
- Main Challenge:
  - Wafer warpage and warpage change during reflow
  - Wafer fixation during processing
- ➢ With optimized process nearly 100% yield could be achieved

- For packaging singulation standard wafer blade dicing as well as cutting by laser was successful evaluated



300 mm wafer after solder ball attach



Singulated USiP package

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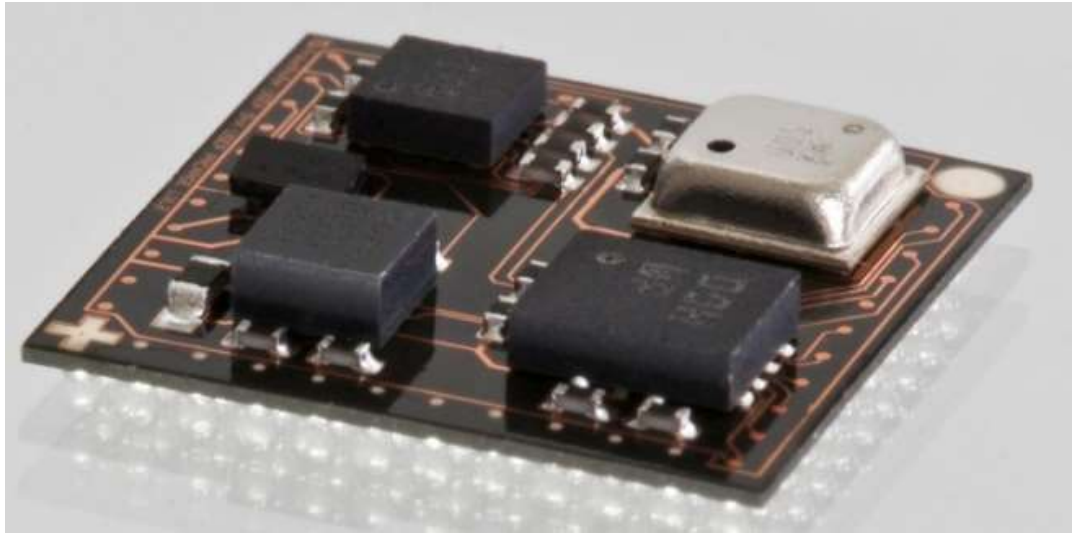
Sensor Assembly on RDL last

- Assembly of passive components and SMD sensors on RDL last
- Process demonstrated on singulated packages
  -> transfer to assembly on wafer level possible



Process flow:

- Placement in package specific workpiece holder
- Maskless solder place jetting
- Automatic pick and place
- Reflow soldering

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Process Challenge

WARPAGE

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Warpage Evaluation during RDL first Processing

Wafer Level on Carrier

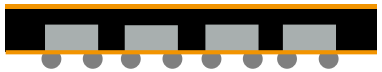
- Carrier thickness & CTE
  - Release layer
    - RDL stack
- Si area density & thickness
- EMC properties & thickness
  - Grinding process
    - Backside RDL

Wafer Level without Carrier

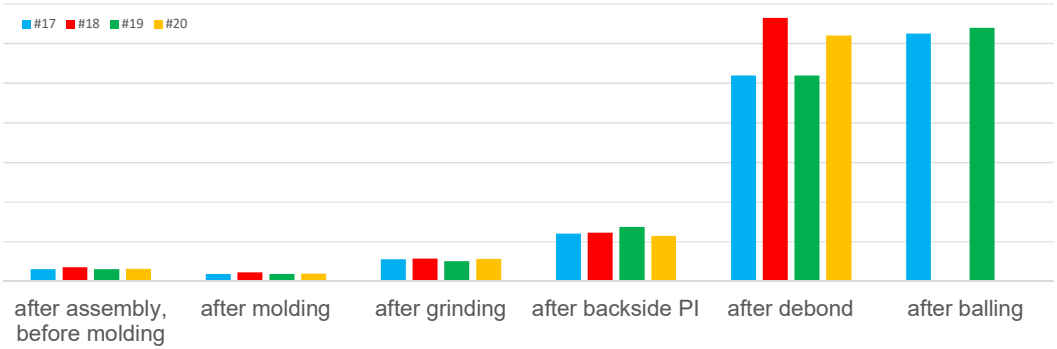
- Carrier release
  - Release layer clean
    - Seed layer etch
    - Balling / reflow

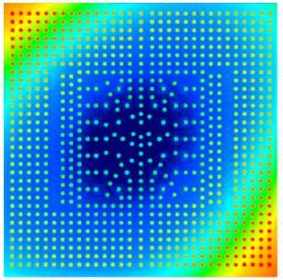
Package Level

- Package singulation



~ 200 process steps





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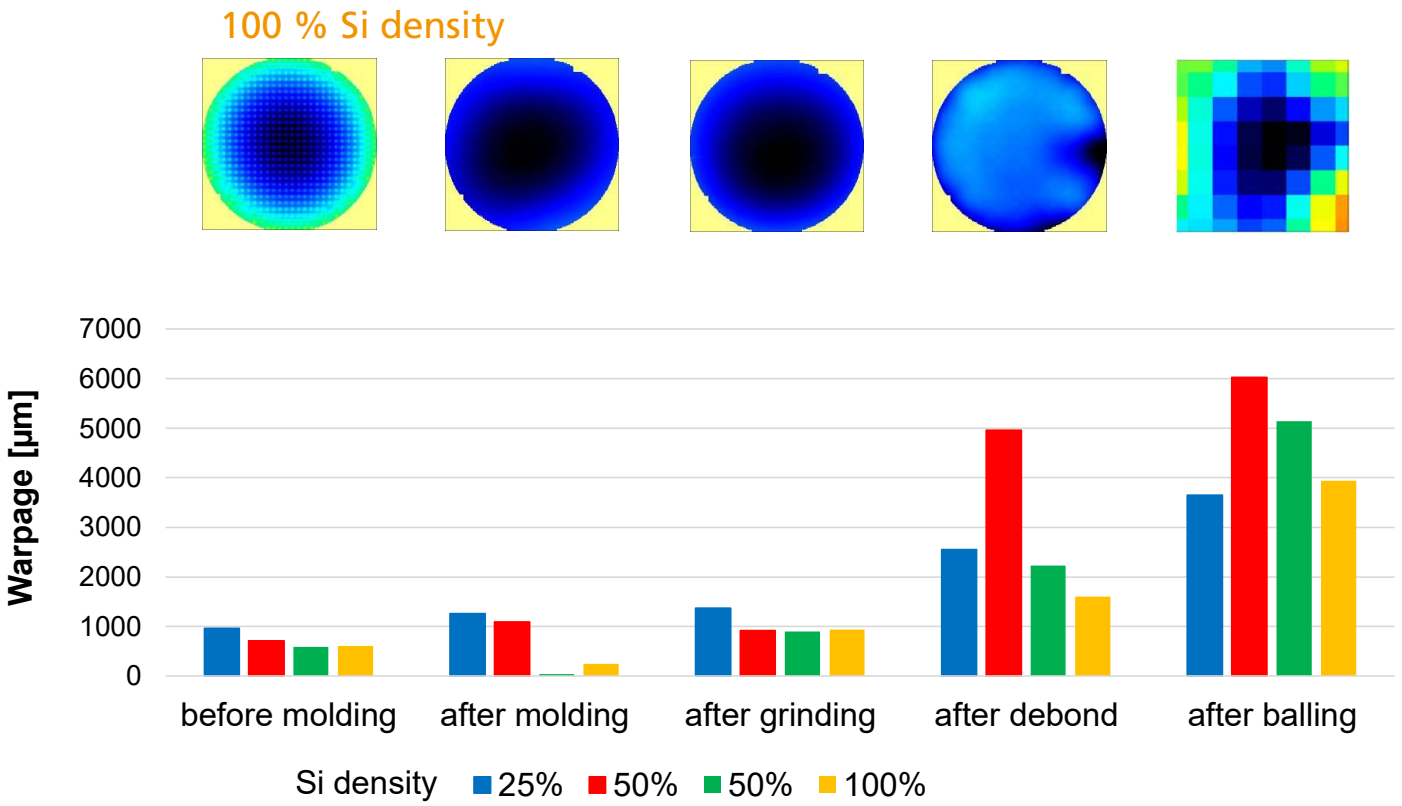
Warpage Evaluation during USiP Processing



- Warpage changes significantly during processing due to different process conditions (e.g. temperature, vacuum, CTE mismatch)
- Significant increase in warpage after debond and reflow
- 3D warped/bended wafer after debond and reflow
- The ratio of mold vs. Si density plays an important

100 %: all dies assembled in reticle

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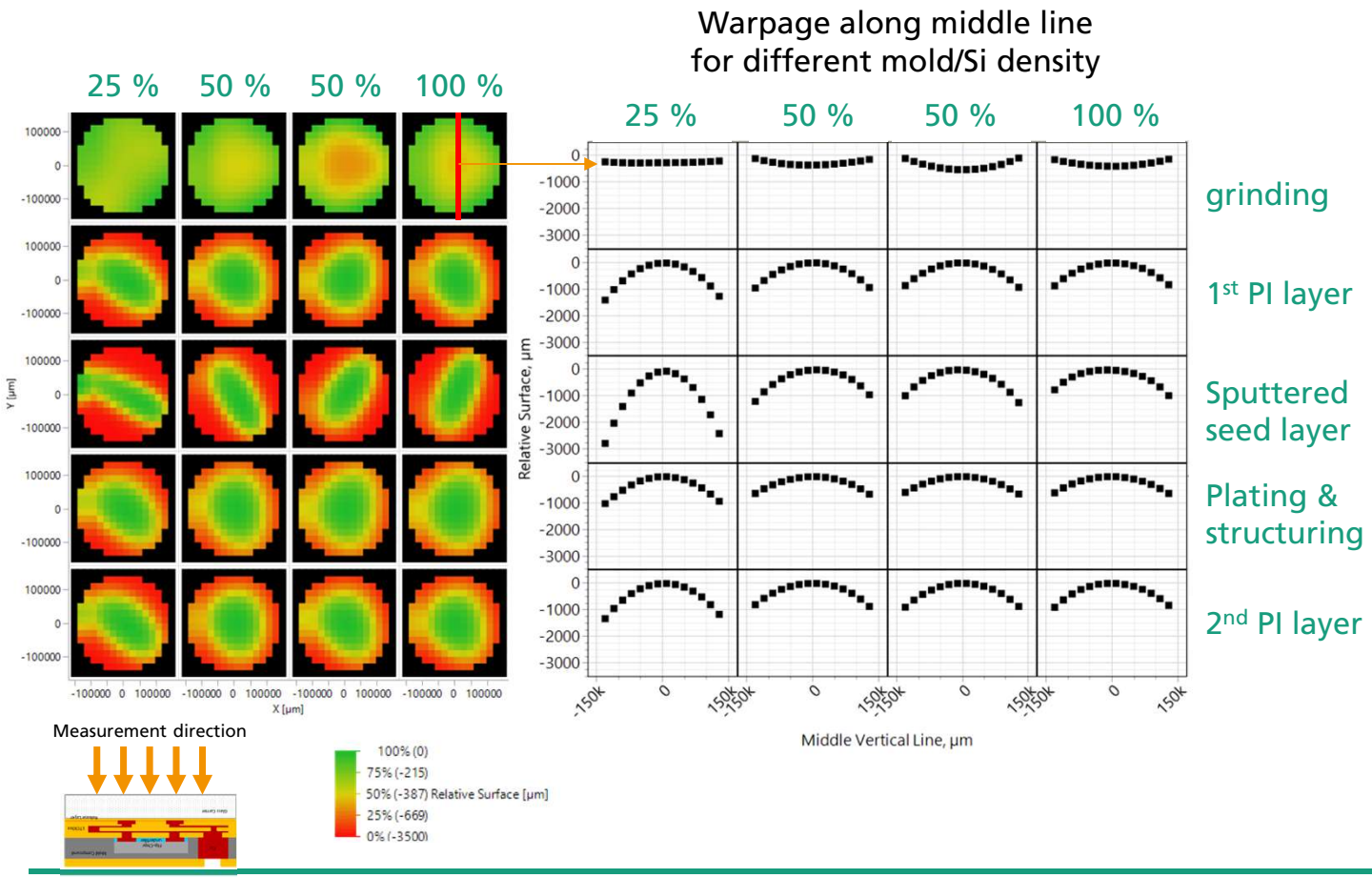
Warpage after each Process Step – RDL last Process (on carrier)



- Warpage changes during processing due to different process conditions (e.g. temperature, vacuum, CTE mismatch)
- The ratio of mold vs. Si density plays an important role as well (25% Si density has the highest warpage)
- A symmetrical RDL setup helps to minimize the warpage and enables handling on film frame after glass carrier release

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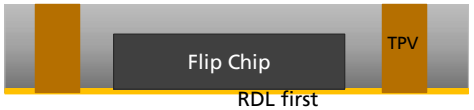
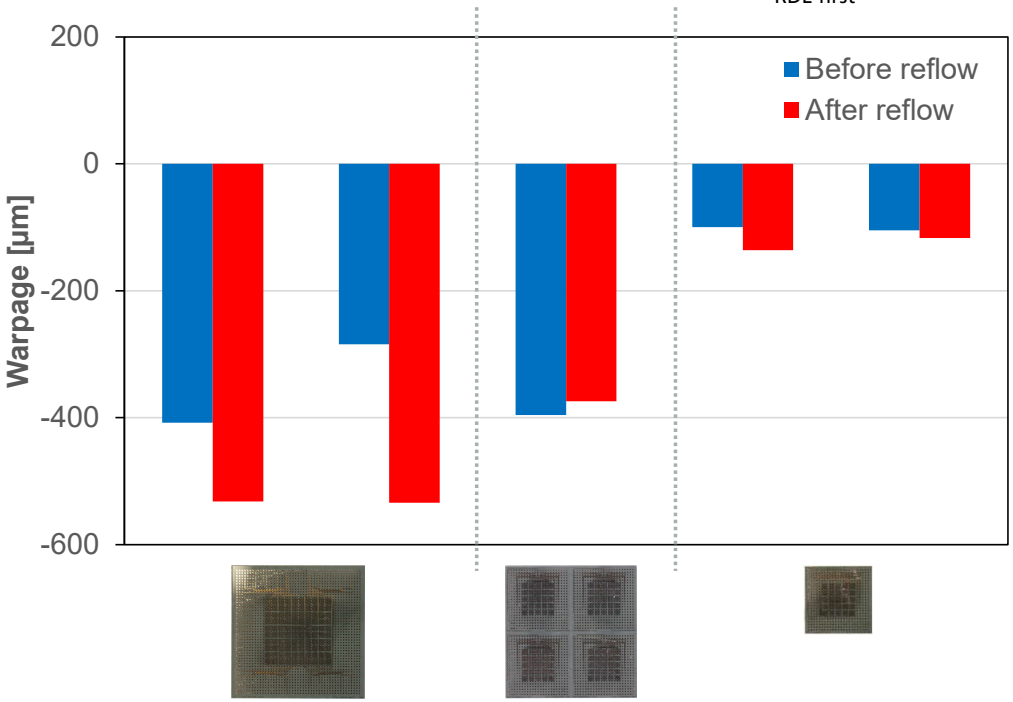
Study Influence Warpage on Package Level

Without RDL last



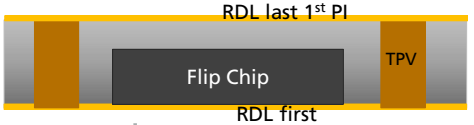


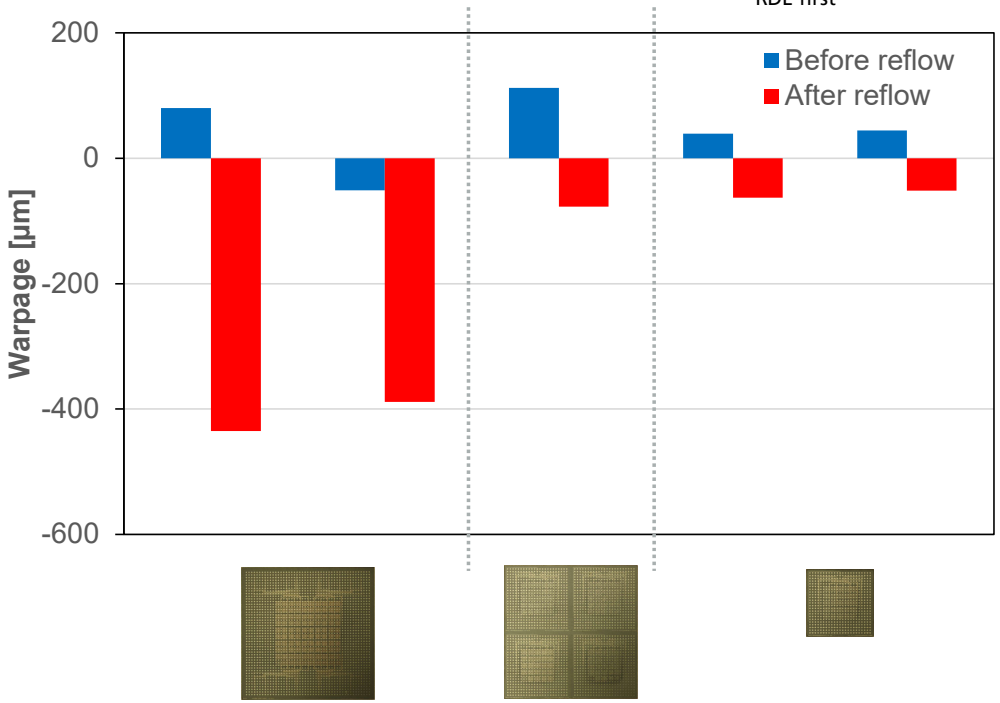
P: 20x20 mm²
D: 10x10 mm²

P: 20x20 mm²
D: 4x 5x5 mm²

P: 10x10 mm²
D: 5x5 mm²

With 1st RDL last PI layer





P: 20x20 mm²
D: 10x10 mm²

P: 20x20 mm²
D: 4x 5x5 mm²

P: 10x10 mm²
D: 5x5 mm²

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DEMONSTRATOR

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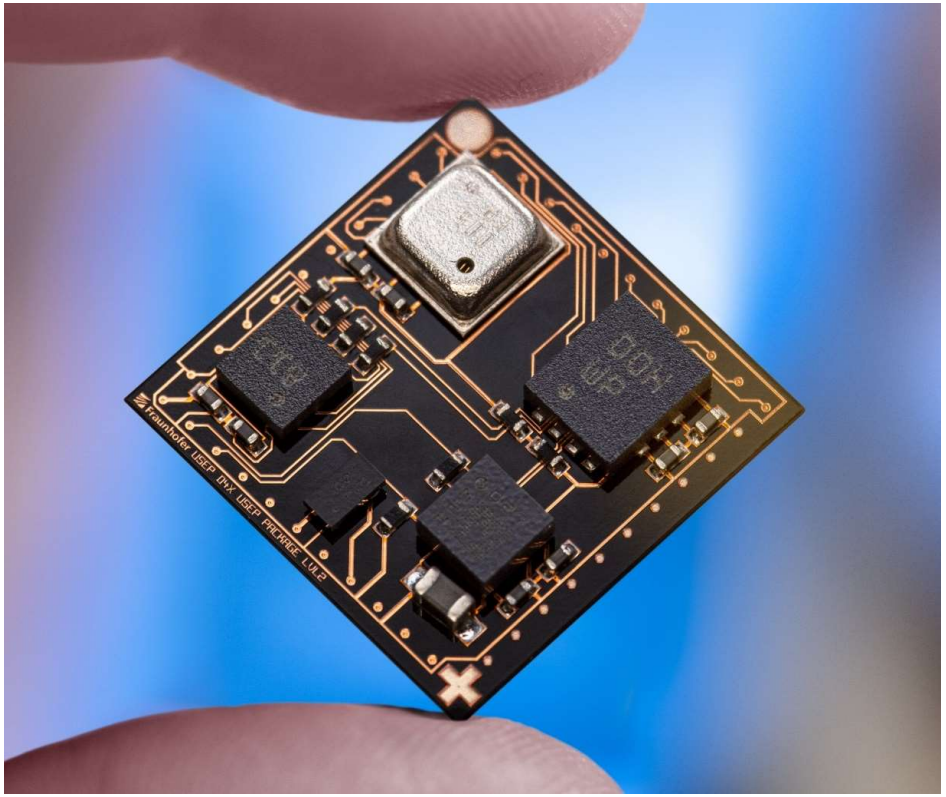
USiP Demonstrator Manufacturing



- Optimized processes applied to manufacture functional demonstrator
- RDL first package includes USoC and 12 x 1 nF and 6 x 10 nF as FC IPDs
- Sensors assembled on RDL last:
  - Bosch BME680 (temperature, humidity, pressure)
  - Bosch BMA456 (acceleration, inclination)
  - Bosch BMG250 (triaxial gyroscope)
  - ST Microelectronics MIS2DH (vibration, acceleration)

➢ **Package concept successfully demonstrated**

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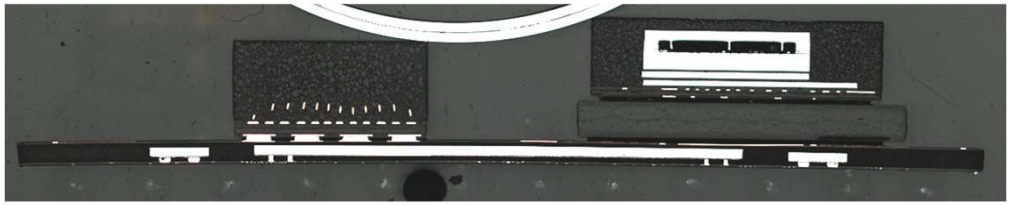
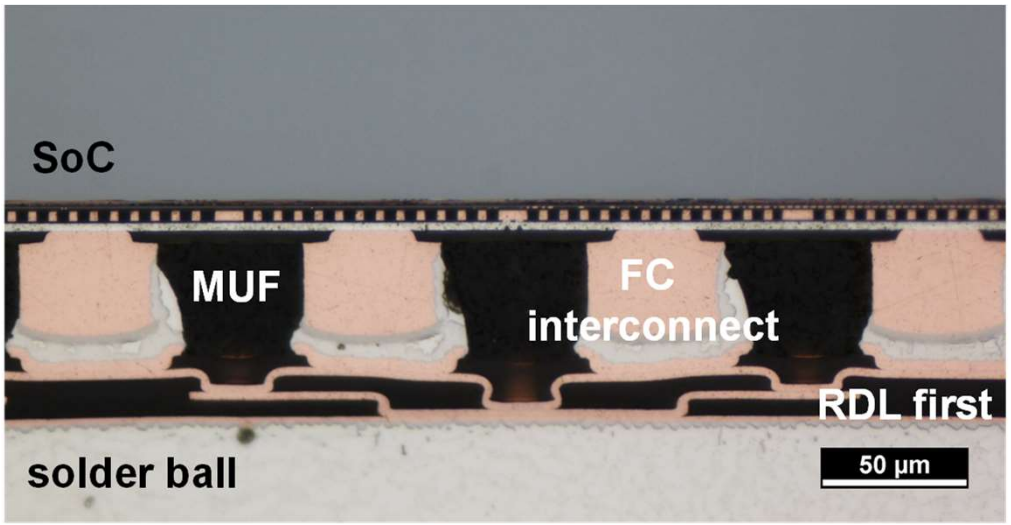
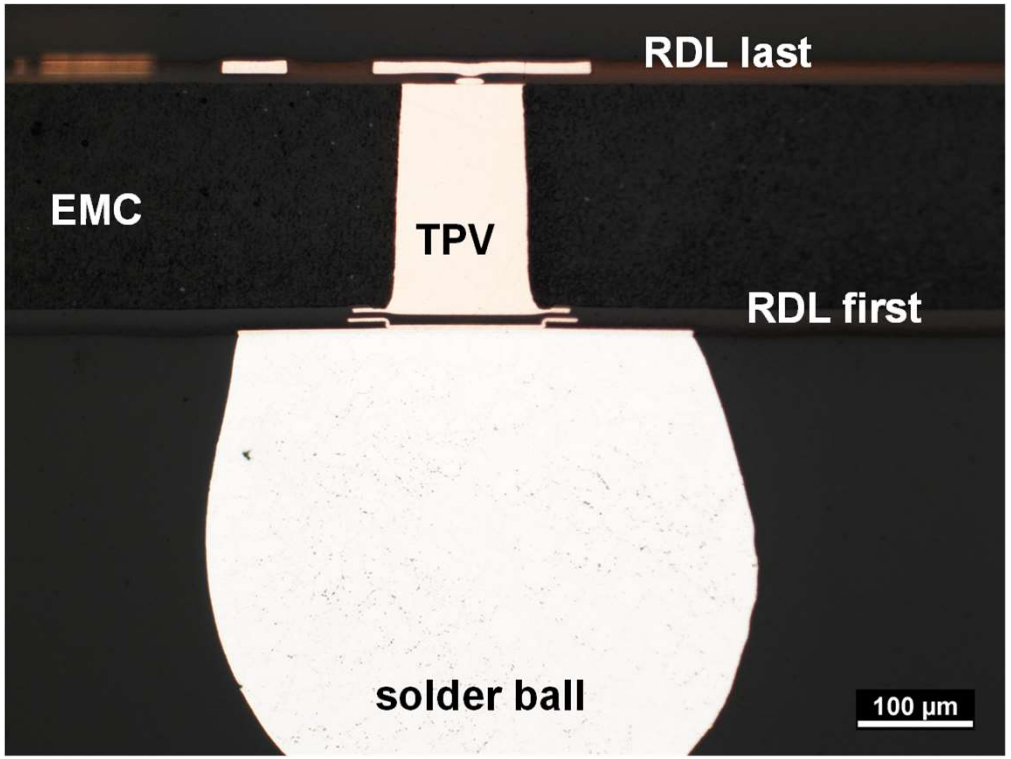
USiP Demonstrator Manufacturing

➢ **Package concept successfully demonstrated**







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TEST & EVALUATION

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Architecture of Development, Test and Validation Infrastructure

- The concept of the infrastructure is based on a highly modularized approach, which means that for every design task and field of electrical and functional validation of the package a dedicated test module is available and can be added to the evaluation board
- The evaluation board represents the basic architecture with all necessary peripheral components and building blocks such as energy supply, digital and analogue interfaces, and probing and debugging capabilities
- Based on high density multi-pole connectors and test socket with BGA Footprint the dedicated hardware modules can be stacked on the evaluation board
- The test sockets itself allow non soldering connection between PCB and electrical interface
- The BGA footprint of the socket can be later used for soldering of the known good SiP modules

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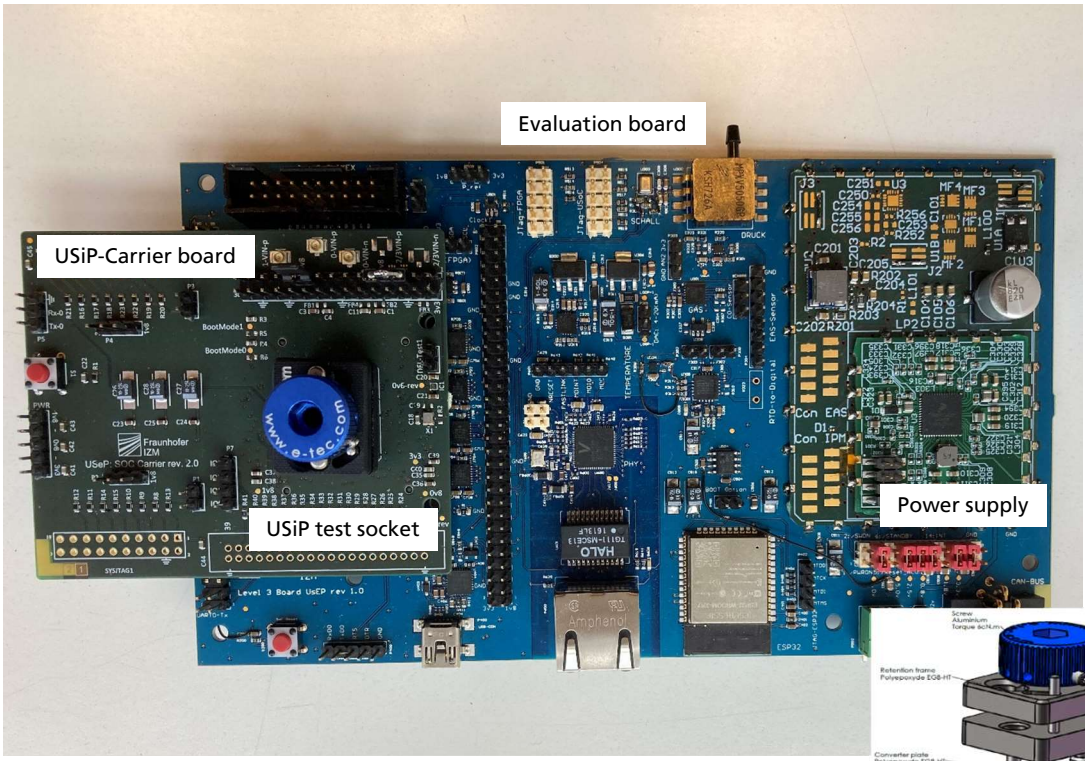
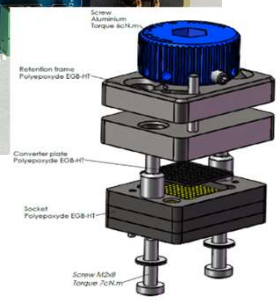
USoC final Package Testing

- Final 3D package design could be tested and evaluated by an additional adapted socket and USiP-carrier board which are also connected to the evaluation board
- In this step the additional sensor layer on top of the package could be tested
- ➢ **Furthermore the package concept and manufacturing process could be validated**



Evaluation board with all mounted test modules



Technical drawing by e-tec

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Summary & Outlook

- An Universal IoT Sensor Platform based on a FOWLP approach
- Standard SOC core package (RDL first) with a customized RDL last on top for sensor assembly
- Scalable approach from low to high volume needs
- Developments include
  - SOC design and manufacturing (FHG IIS-EAS & Globalfoundries)
  - Package concept and design
  - FOWLP process development based on a RDL first approach with a RDL last on top on 300 mm wafer size
  - Test and validation
  - Reliability Testing (ongoing)
- Dedicated design rules und process of record (POR) are defined and used for successful demonstrator manufacturing
- Main challenge: warpage – has to be considered and optimized from design on through the entire process

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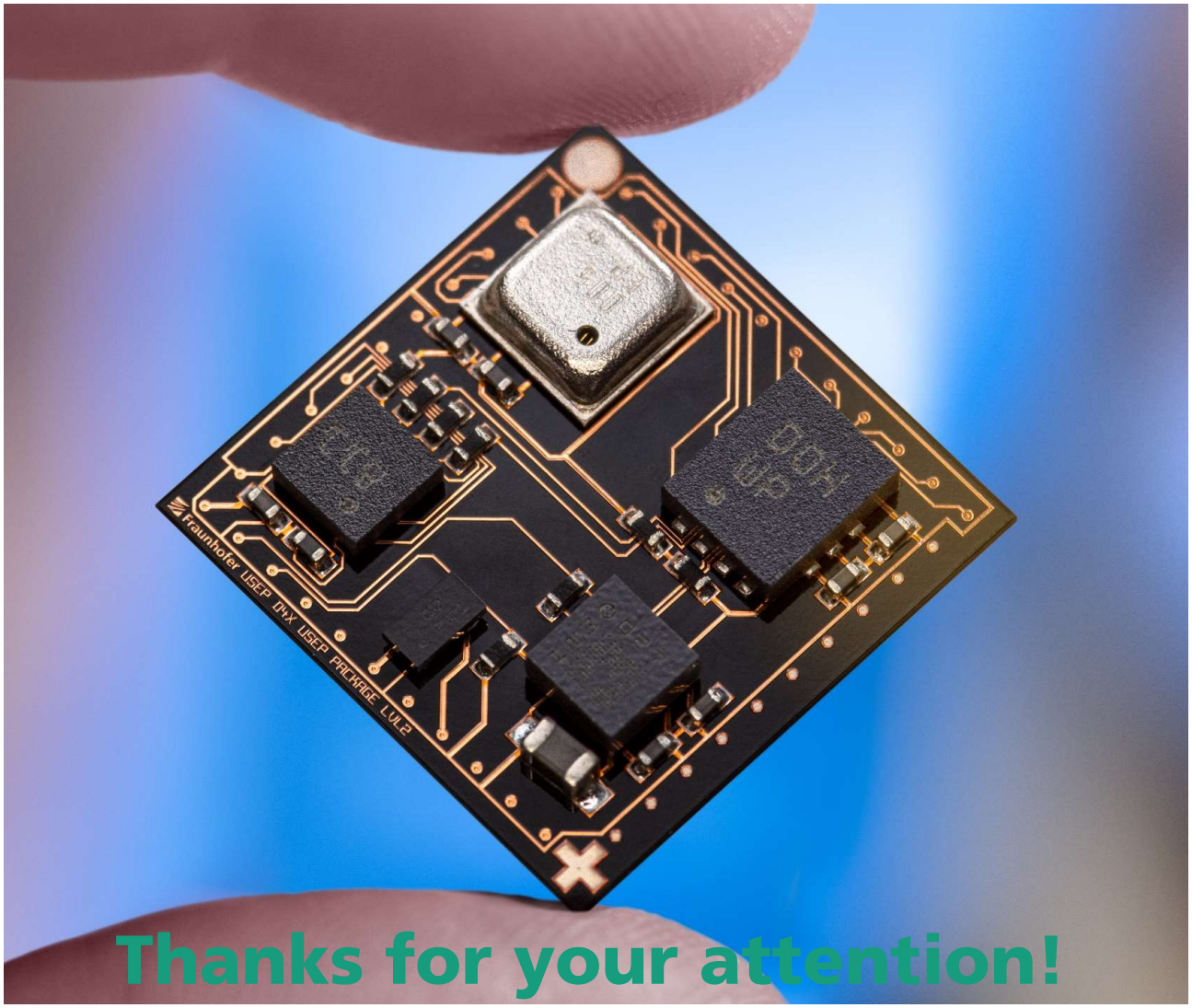

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