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SIEMENS

Advanced Semiconductor Engineering, Inc.

Using Deca's Adaptive Patterning™ to win the Chiplet Integration race with Siemens EDA and ASE

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Agenda

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1. Introductions
2. Background
3. Technology overview
   1. Silicon Interposer
   2. Embedded Bridge
   3. Fan-Out
4. Adaptive Patterning™ Introduction
5. Design Study
6. Follow Up Work

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1 Introductions

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Robin Gabriel – Solutions Architect, AP Studio

Jan Kellar – Sr. Director of Applications & Design

SIEMENS

Keith Felton – Product Marketing Manager, High Density Advanced IC Packaging

Ian Gabbitas – Applications Engineer, IC Packaging

ASE GROUP

John Hunt – Sr. Director of Engineering, Marketing & Technical Promotion

Lihong Cao – Director, Corporate Technology Development

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2 Background

Adoption Life Cycle

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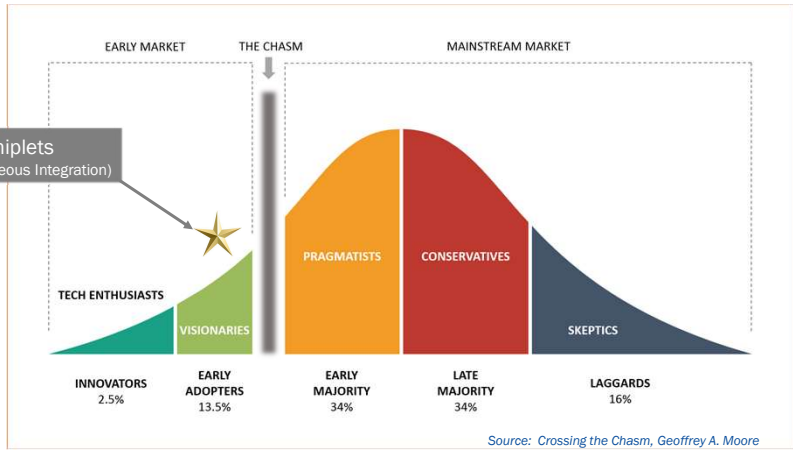

- Chiplets are close to crossing the chasm
- Achieving cost-effective high-density integration is key

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The Chiplet Integration Race

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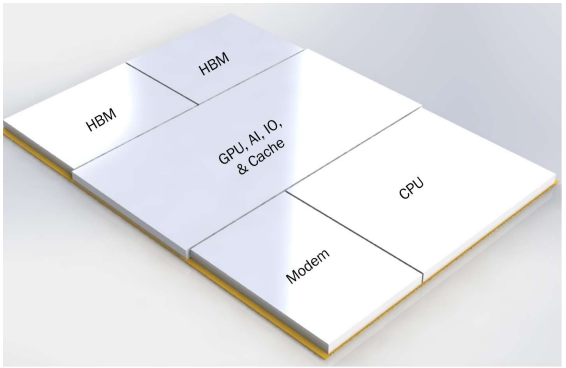
Key Competition Factors

1. Cost
2. Yield
3. Scalability



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3 *Technology Overview and Comparison*

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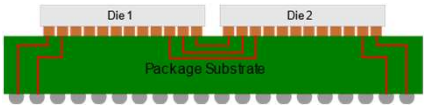
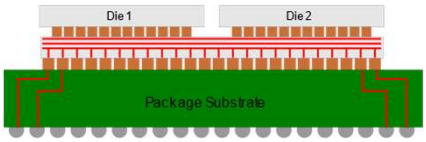
Competitors

Heterogenous Integration Solutions

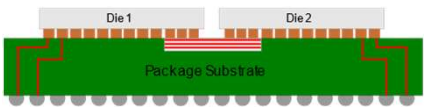
Traditional Multi-die Flip-Chip



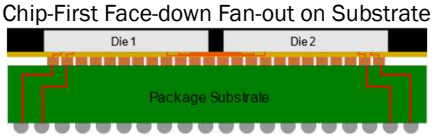
Silicon Interposer



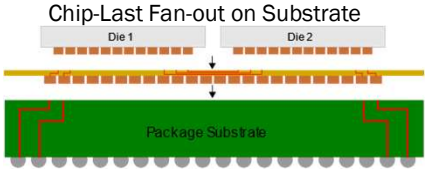
Embedded Bridge



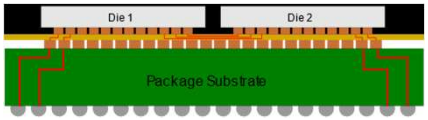
Chip-First Face-down Fan-out on Substrate



Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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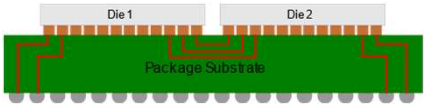

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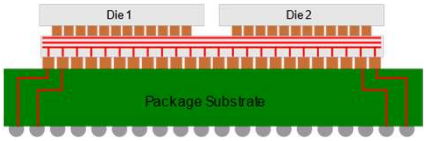

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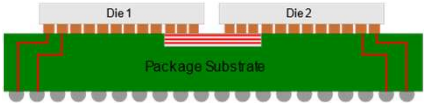

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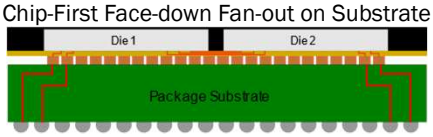

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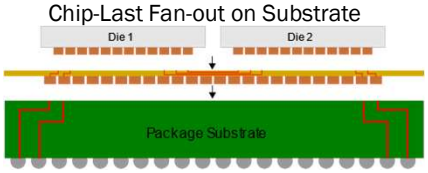

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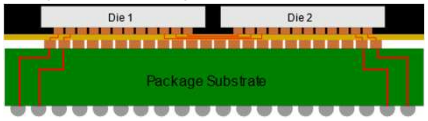

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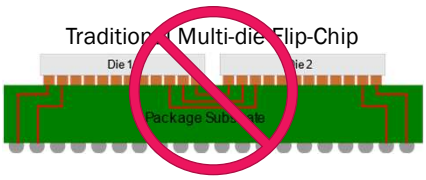

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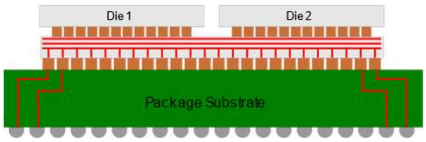

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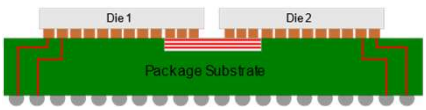

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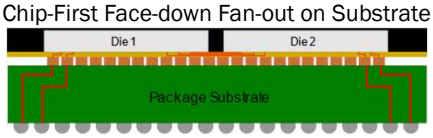

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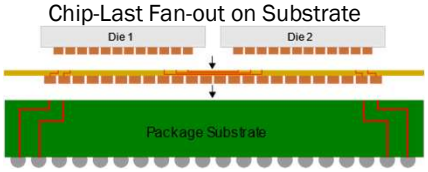
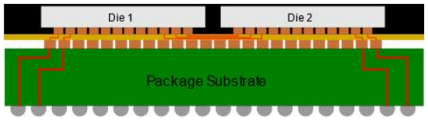


Chip-First Face-up Fan-out on Substrate



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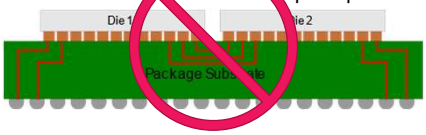
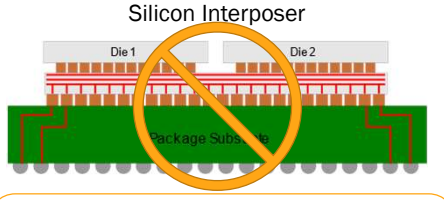


Silicon Interposer



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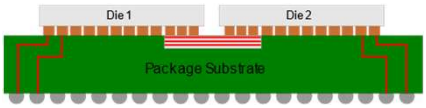
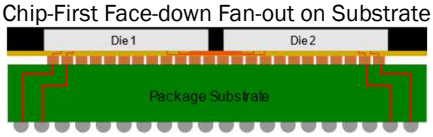


Chip-First Face-down Fan-out on Substrate



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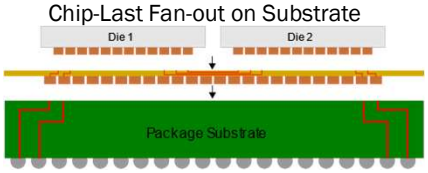

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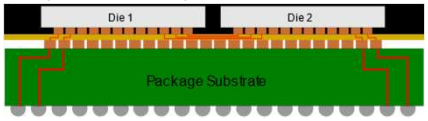

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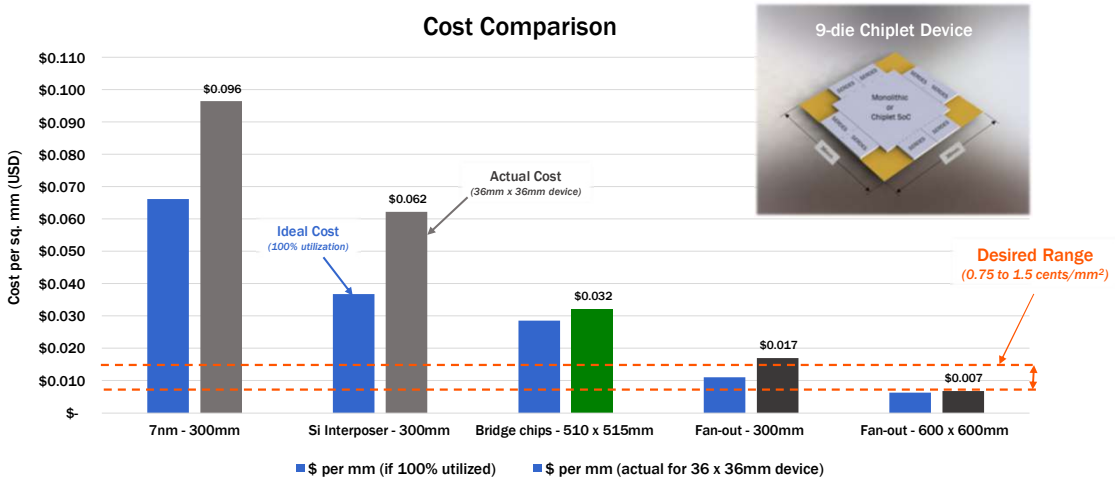
Cost

Normalized in $ per mm²



One cent ($0.01) per mm² key target for mainstream (mass market) chiplet adoption

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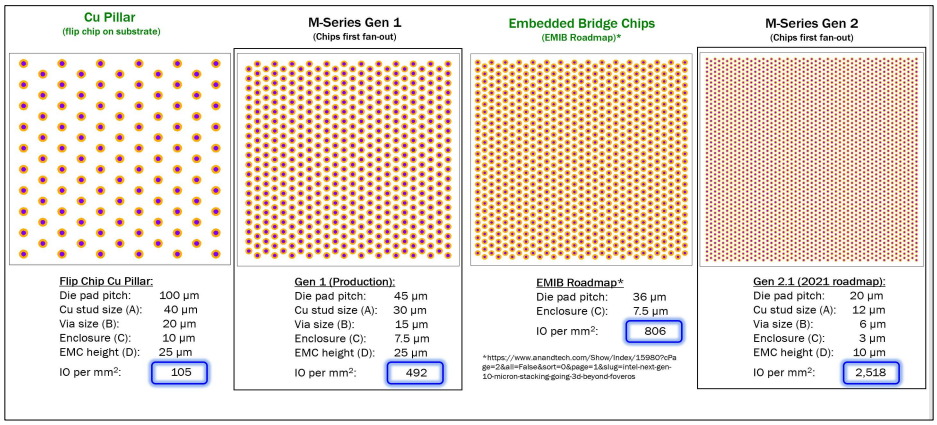
Scalability

Minimum Die Pad Pitch Supported



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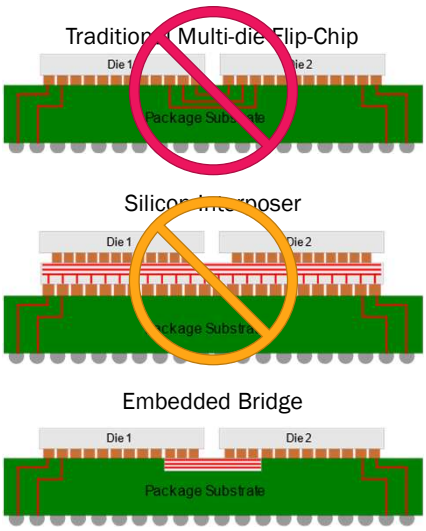
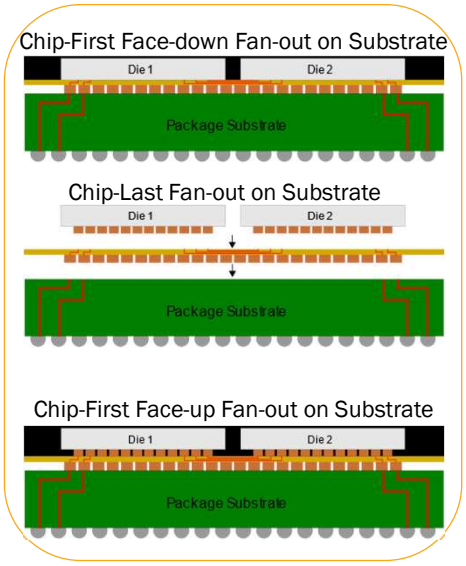
Competitors

Heterogenous Integration Solutions





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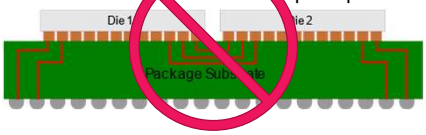
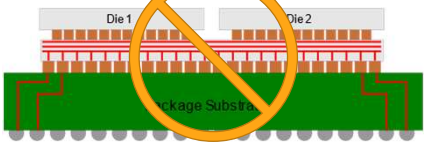
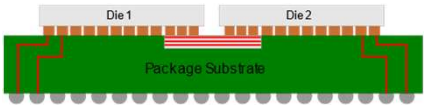


Silicon Interposer



Embedded Bridge



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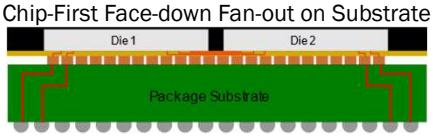
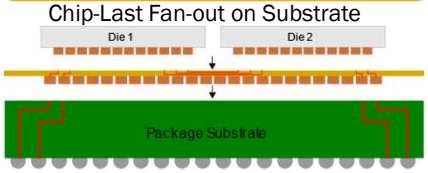
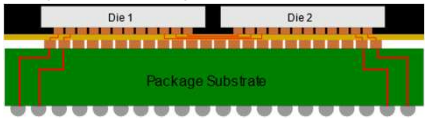


Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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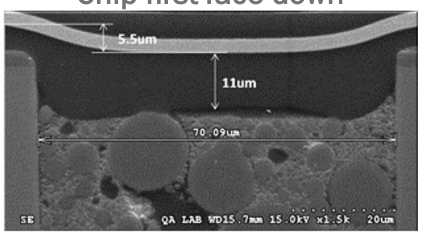
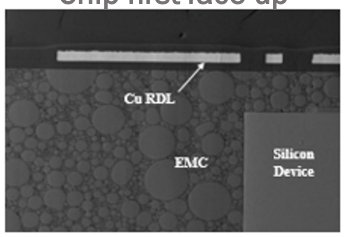
Chip-First Face-down Fan-out on Substrate

Yield - Planarity

Chip-first face-down



Chip-first face-up



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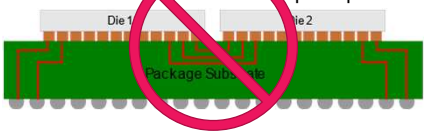

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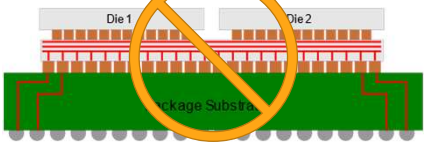
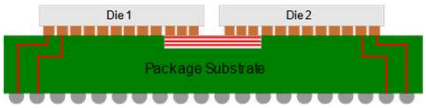


Embedded Bridge



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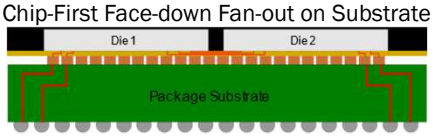
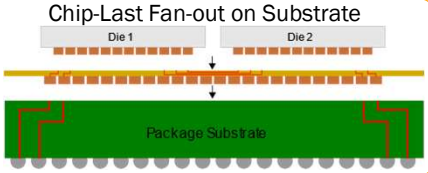


Chip-Last Fan-out on Substrate



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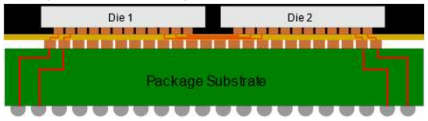

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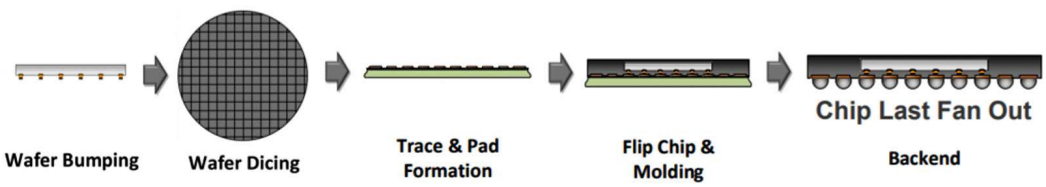
Chip-Last Fan-out on Substrate

- Provides an opportunity to integrate known-good die (KGD) onto a known-good substrate
- Viewed as a simple extension of traditional substrate technology using solder chip-attach
- In practice, significantly more complicated than the traditional flip-chip laminate process with addition of a temporary carrier, RDL build-up, chip attach, molding, and carrier removal
- Additionally, high precision low-throughput thermo-compression die attach is typically required
- The solder-metal interface required for flip-chip bumping adds electrical discontinuities in the signal path



*Courtesy of ASE

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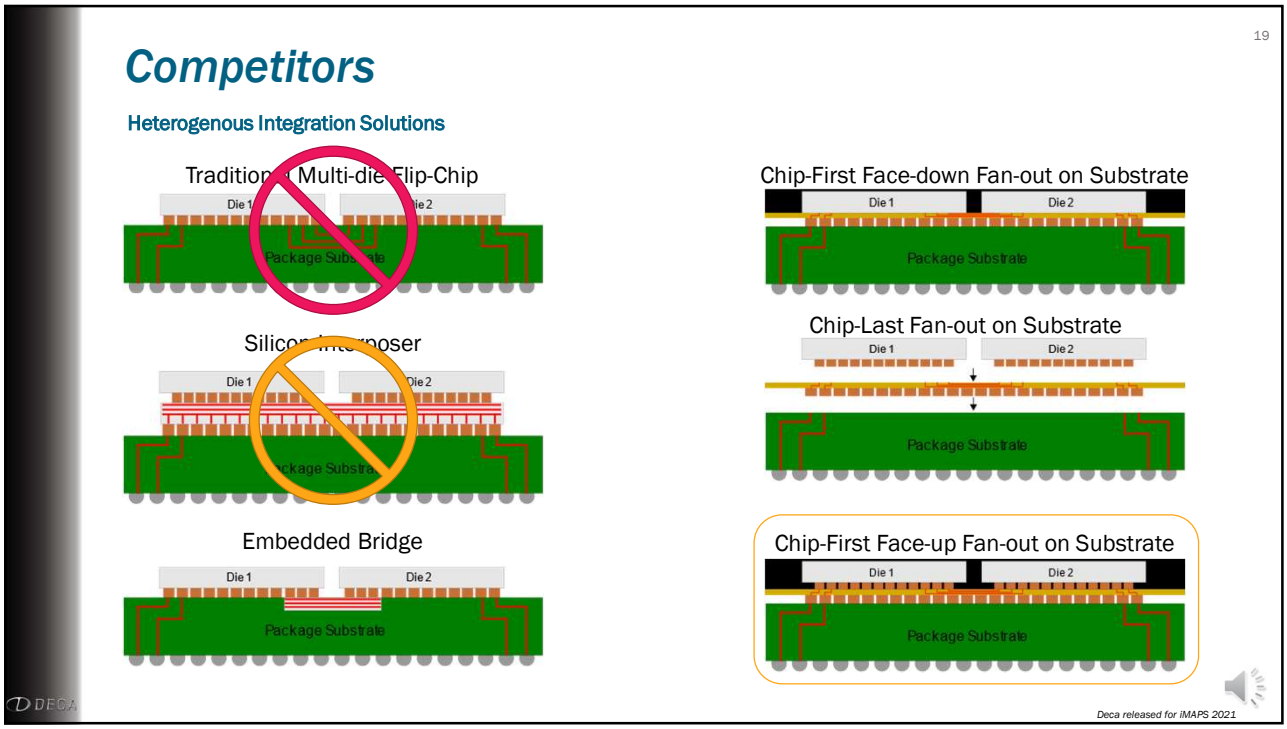
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Competitors
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Traditional Multi-die Flip-Chip
Die 1
Die 2
Package Substrate
Silicon Interposer
Embedded Bridge
Chip-First Face-down Fan-out on Substrate
Chip-Last Fan-out on Substrate
Chip-First Face-up Fan-out on Substrate
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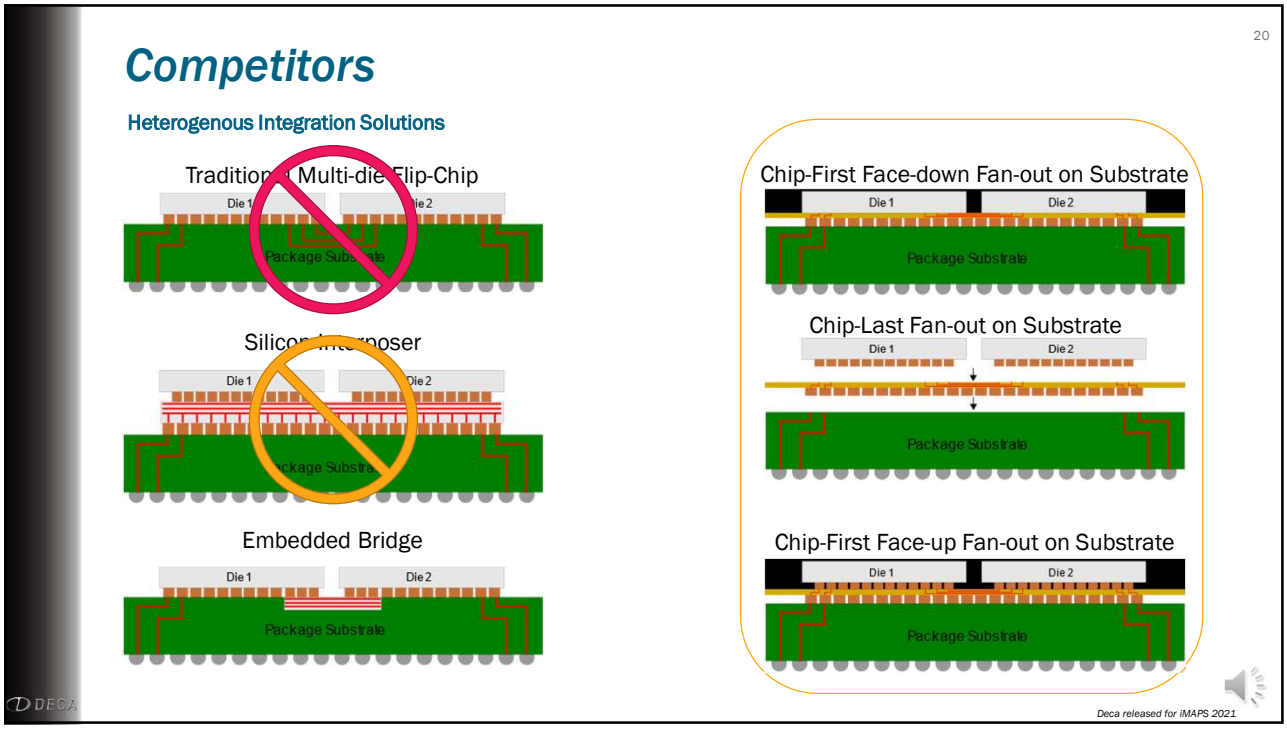
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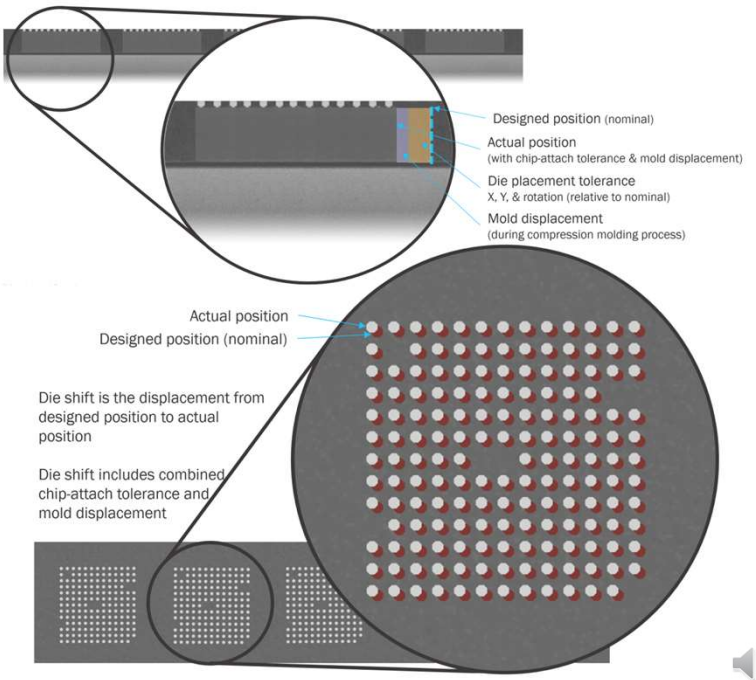
Yield

The Die Shift Problem - #1 Concern

1. Die placement offset

2. Displacement during molding



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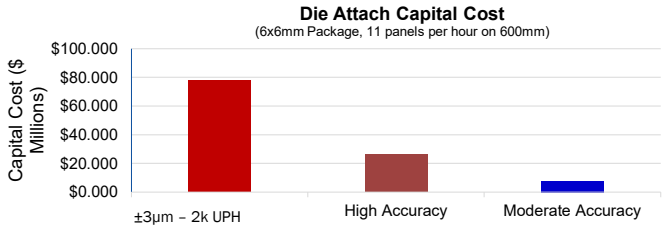
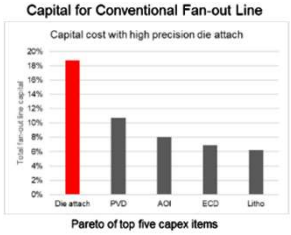
Cost



Production Capacity
3 k panels per month
35 million units per month

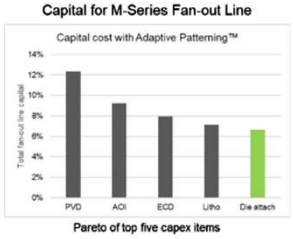
With
Adaptive Patterning

Capital for Conventional Fan-out Line



Pareto of top five capex items

Capital for M-Series Fan-out Line



Pareto of top five capex items

Chip Attach Equipment Options

Very high accuracy	± 3µm @ 3σ	$1.1M	2,000 CPH
High accuracy	± 8µm @ 3σ	$0.9M	5,000 CPH
Moderate accuracy	± 15µm @ 3σ	$1.3M	22,000 CPH

Adaptive Patterning enables an effective ± 3µm @ 3σ performance using the 22,000 CPH machine

10X reduction in highest capex process with Adaptive Patterning

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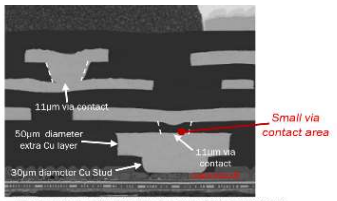
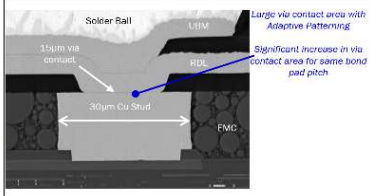
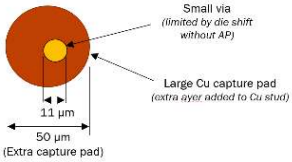
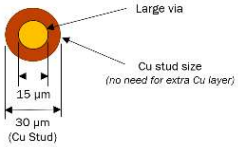
Scalability

InFO bond pad (Latest Gen)	M-Series with Adaptive Patterning (Gen 1)
 *Dimensions estimated by independent consultant	
	

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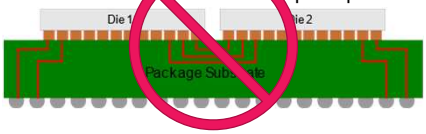
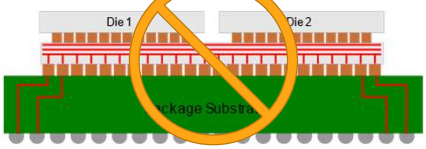
Competitors

Heterogenous Integration Solutions

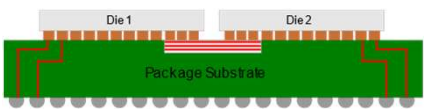
Traditional Multi-die Flip-Chip



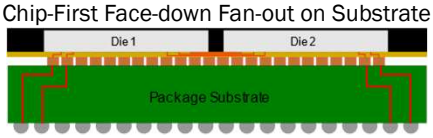
Silicon Interposer



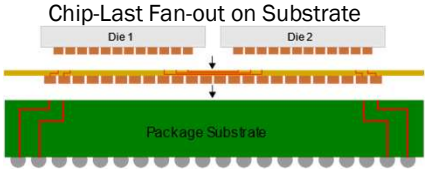
Embedded Bridge



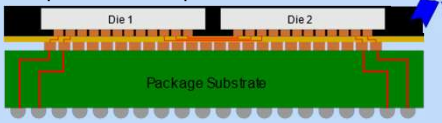
Chip-First Face-down Fan-out on Substrate



Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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6. Follow Up Work

4 *Adaptive Patterning*

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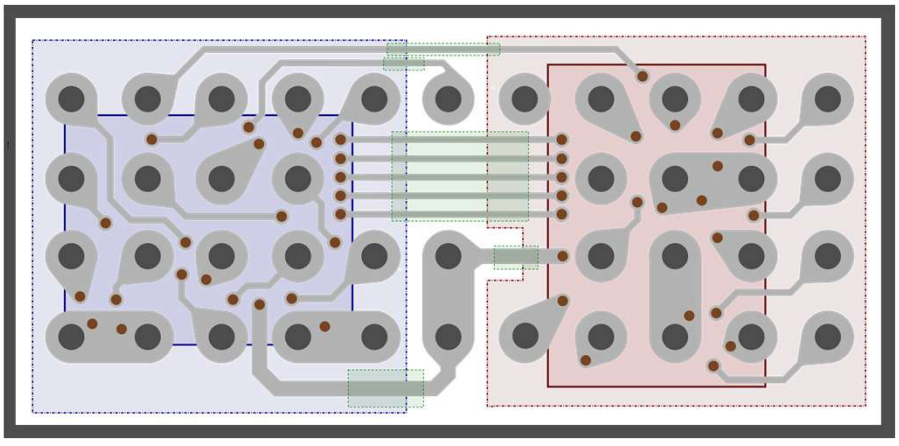
Adaptive Patterning

Design



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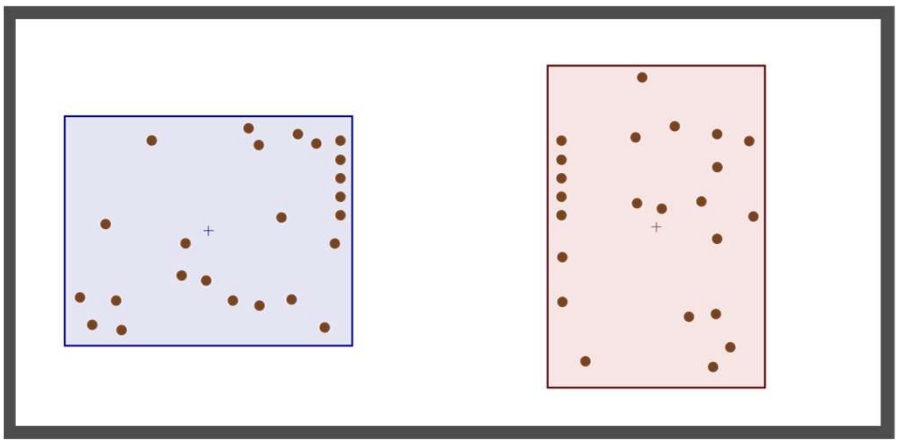
Adaptive Patterning

Die Shift



Die movement

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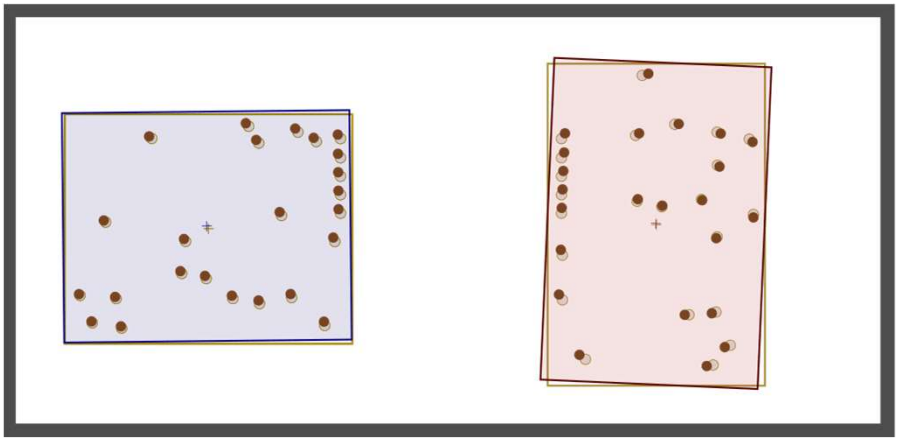
Adaptive Patterning

Die Shift



Die movement

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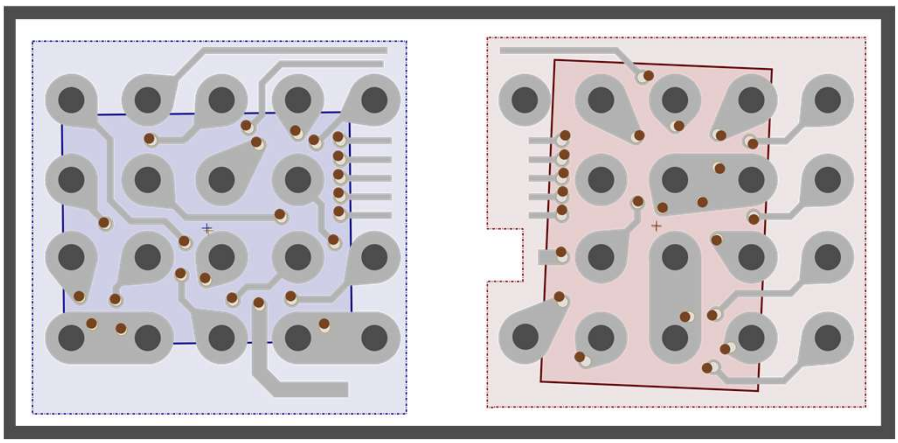
Adaptive Patterning

Adaptive Alignment



Pattern is adaptively aligned to new die position

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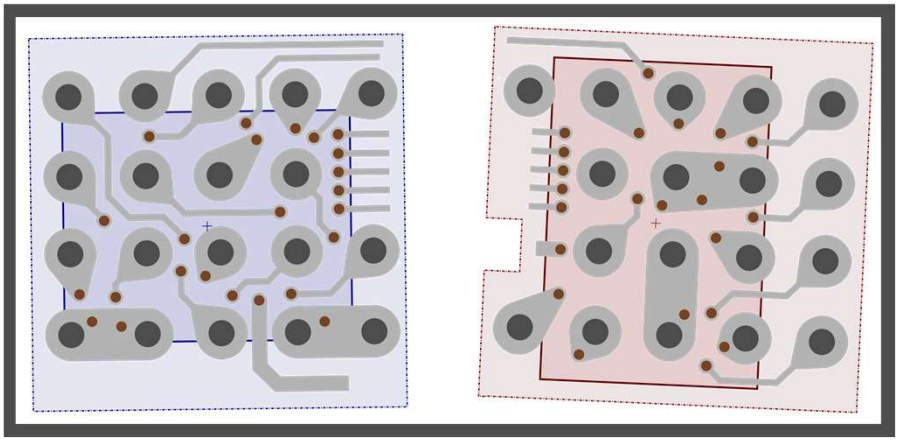
Adaptive Patterning

Adaptive Alignment



Pattern is adaptively aligned to new die position

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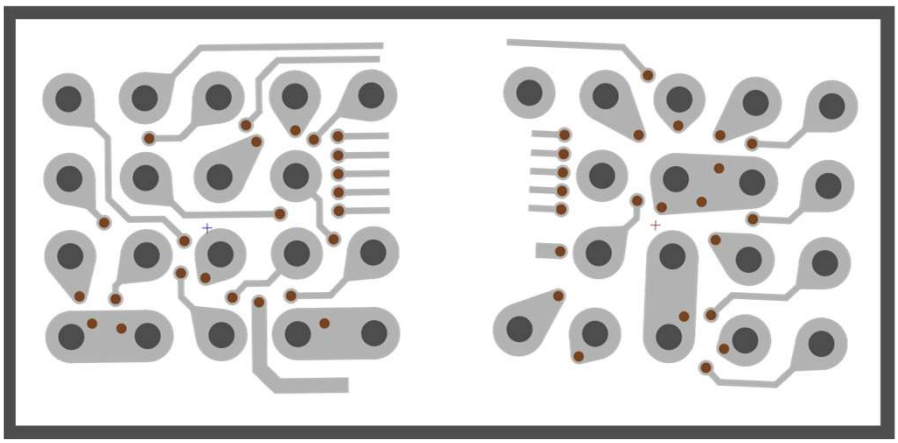
Adaptive Patterning

Adaptive Alignment



Addition of fixed RDL

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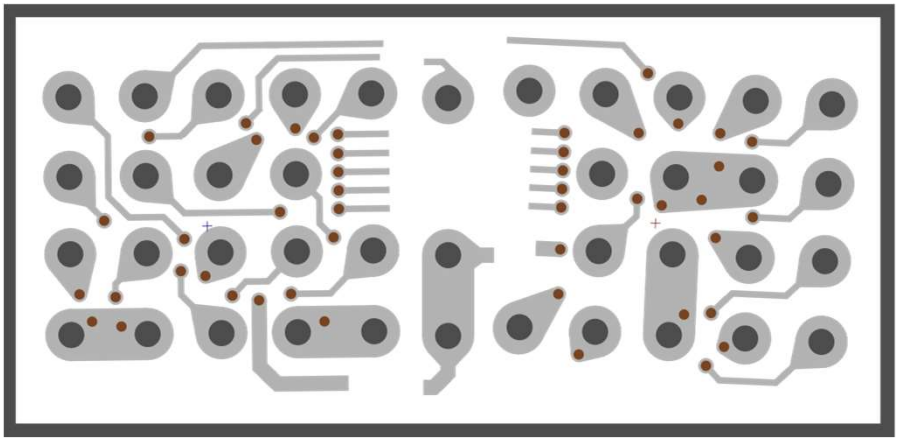
Adaptive Patterning

Adaptive Alignment



Addition of fixed RDL

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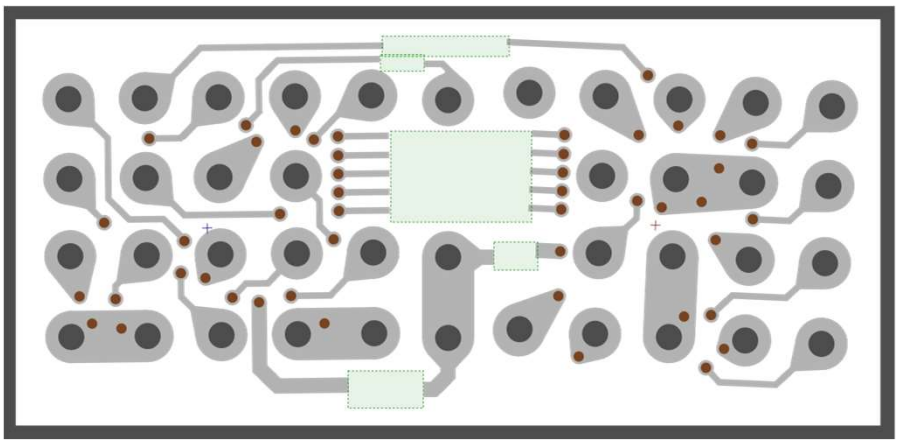
Adaptive Patterning

Adaptive Routing



Adaptive routing is performed to complete connections

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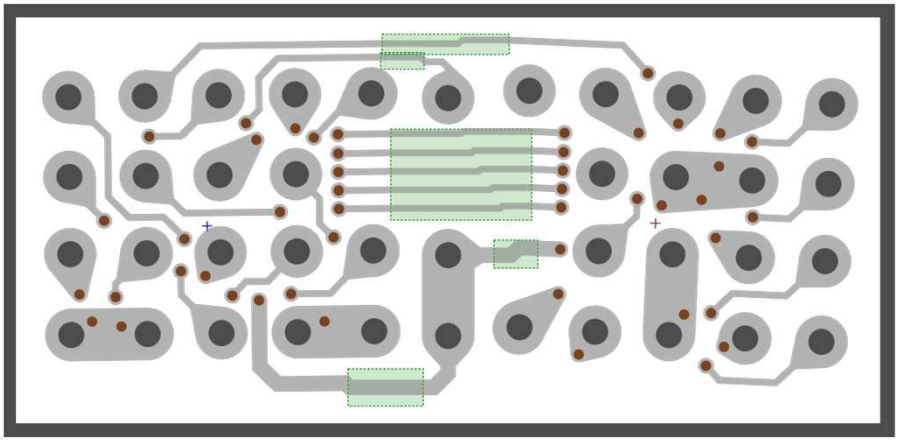
Adaptive Patterning

Adaptive Routing



Adaptive routing is performed to complete connections

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5 *Design Study*

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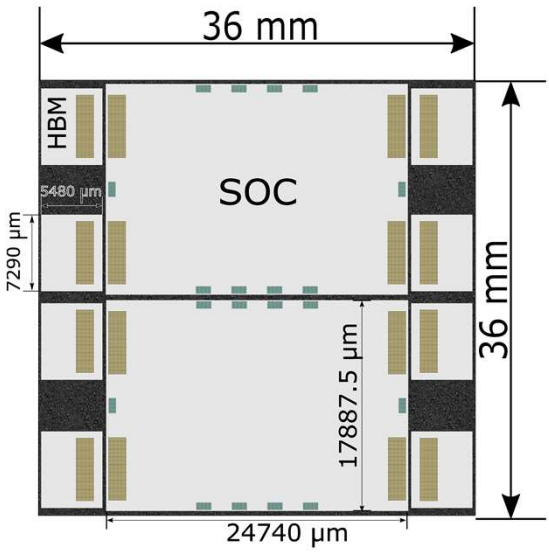
Design Study

Concept



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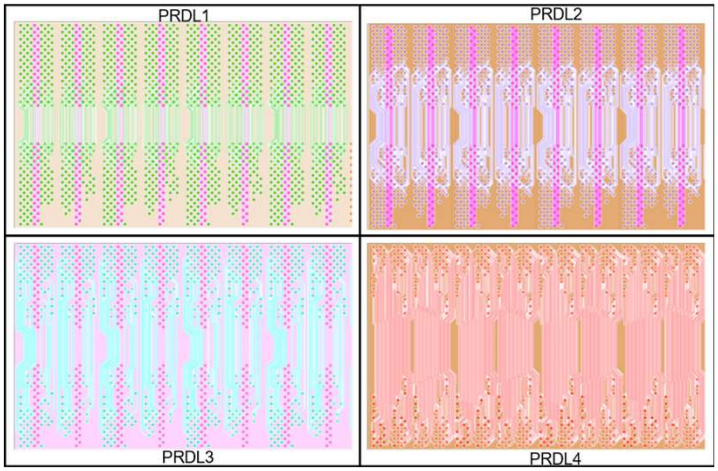
Design Study

20µm Pitch Study



*planned follow up study on layer count reduction using PAA

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Design in Xpedition

Building Interfaces with step and repeat (nCopy)

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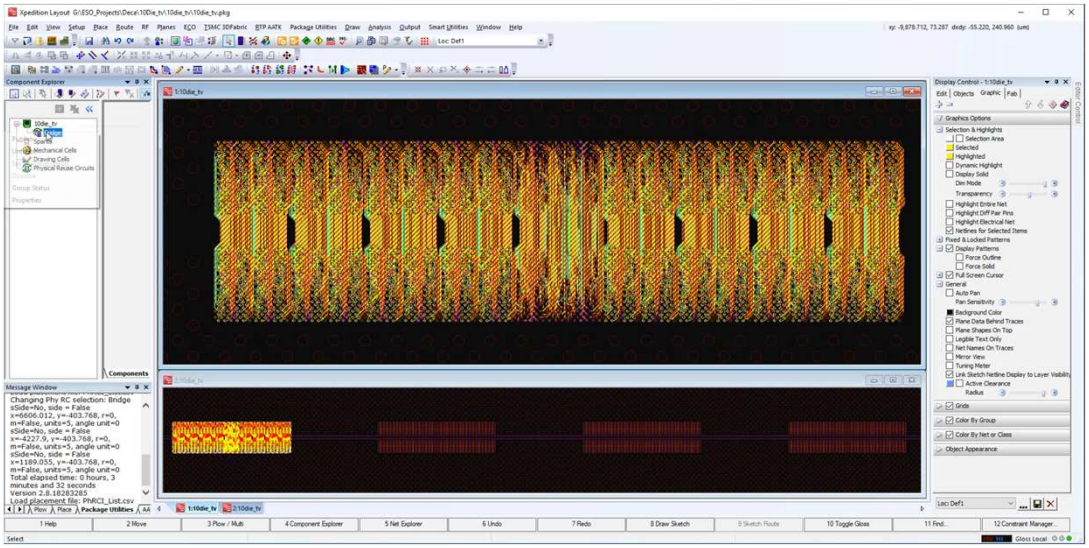
Design in Xpedition – Physical Reuse Blocks

Interface Replication



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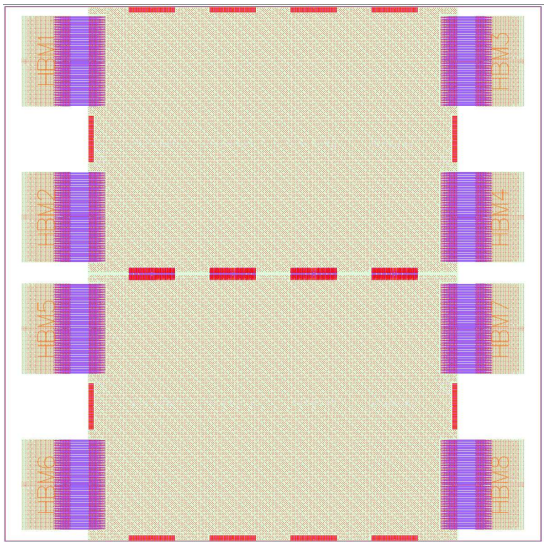
Design Study



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6 *Follow up Work and Conclusions*

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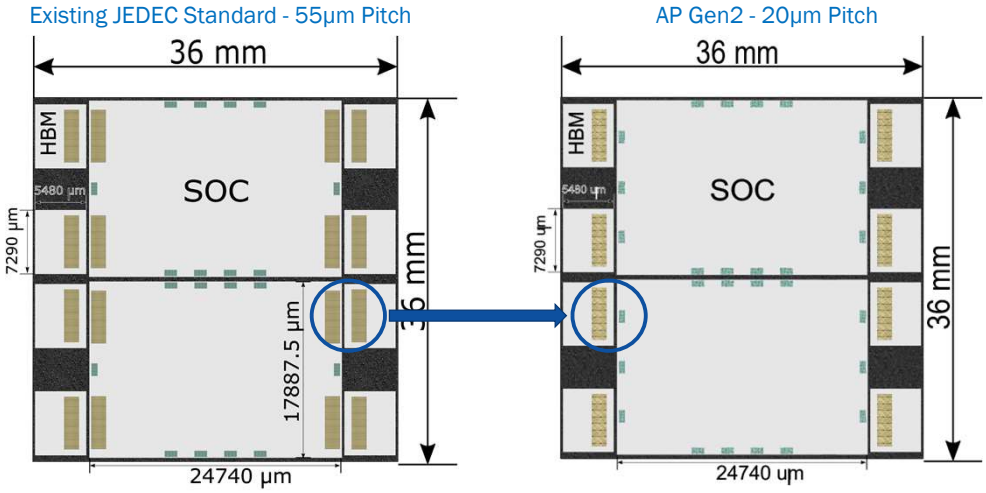
Follow up

Update Design and Build with ASE



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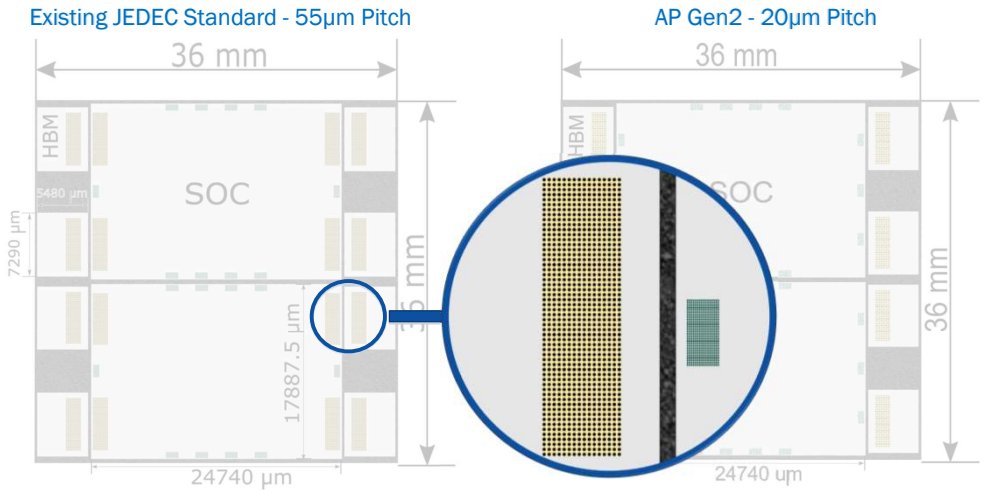
Follow up

Update Design and Build with ASE



86% reduction in required die area

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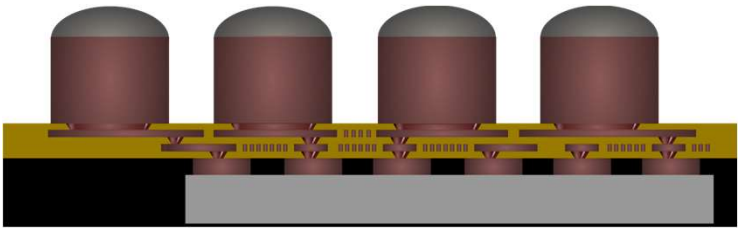
Follow Up Work

Progressive Adaptive Alignment

As Designed



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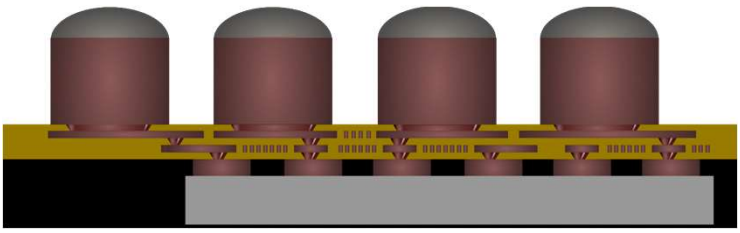
Follow Up Work

Progressive Adaptive Alignment

Adaptive Alignment



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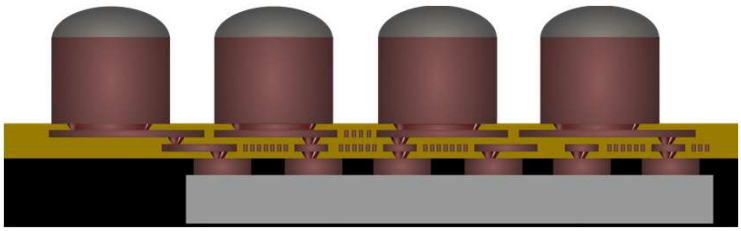
Follow Up Work

Progressive Adaptive Alignment

Progressive Adaptive Alignment



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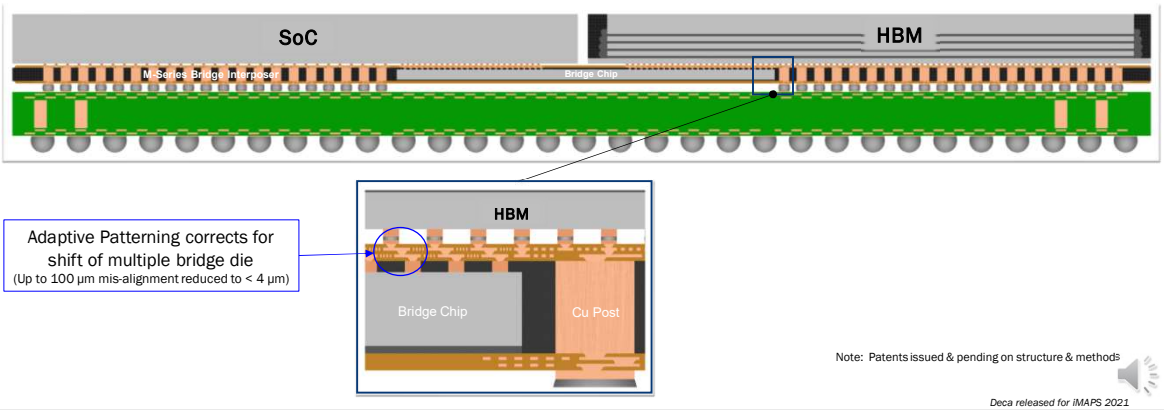
Follow Up

- Opportunity to combine fan-out and bridge chip technologies
  - Integrating silicon bridge into chip-first fanout and using chip-last approach to place SOCs and HBM



Note: Patents issued & pending on structure & methods

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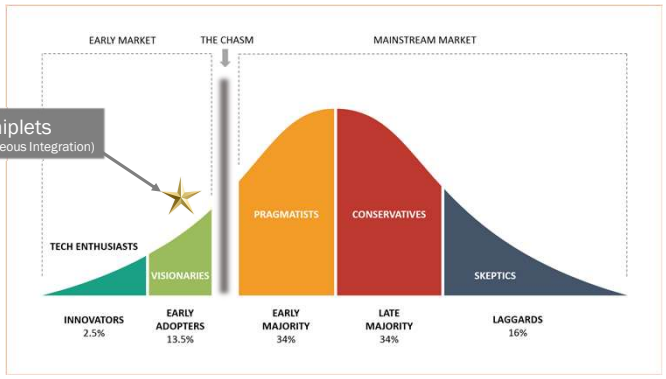
Conclusion



Source: Crossing the Chasm, Geoffrey A. Moore

- Chiplets are close to crossing the chasm to mainstream adoption but cost-effective high-density integration is necessary to do so
- Adaptive Patterning provides a way to break through these barriers and make the transition to mainstream adoption

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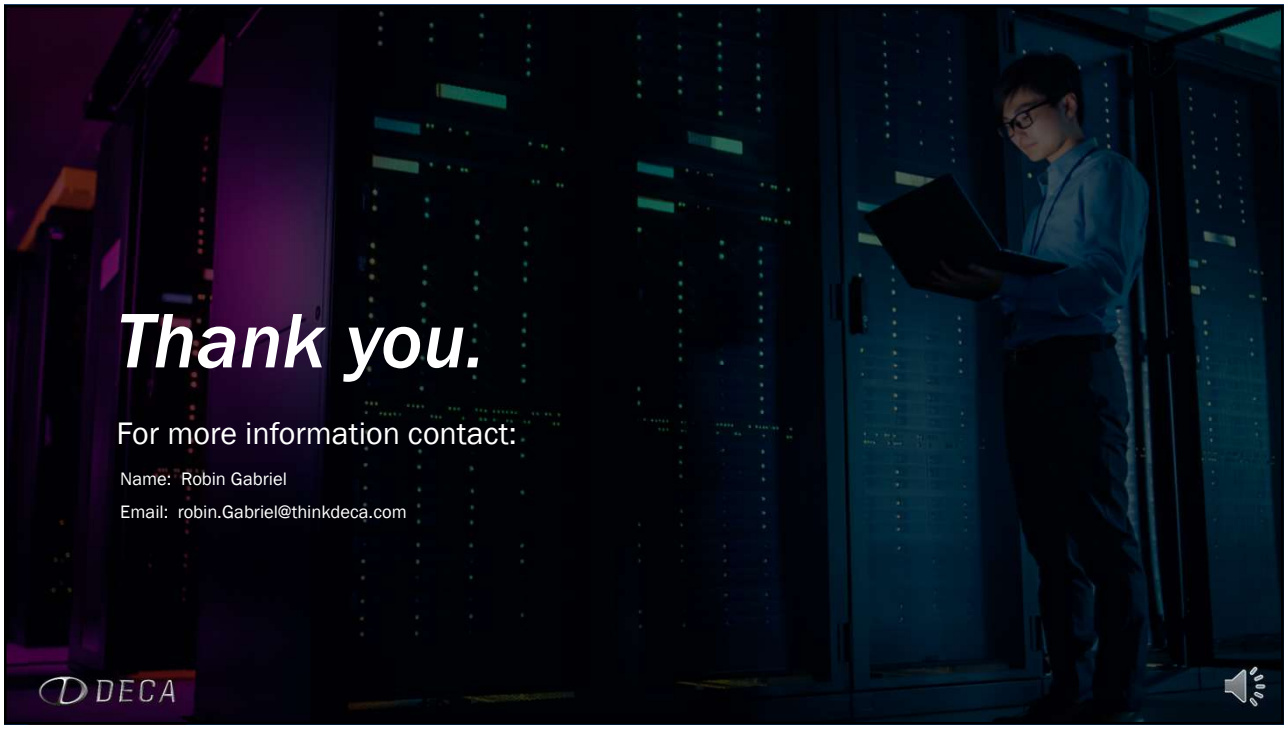
Thank you.
For more information contact:
Name: Robin Gabriel
Email: robin.Gabriel@thinkdeca.com
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