



DECA
SIEMENS



Advanced Semiconductor
Engineering, Inc.

*Using Deca's Adaptive Patterning™ to win the Chiplet Integration race
with Siemens EDA and ASE*



**A GLOBAL
VIRTUAL EVENT**
APRIL 12-15, 2021

**17TH INTERNATIONAL CONFERENCE ON
DEVICE PACKAGING**

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Agenda

1. Introductions
2. Background
3. Technology overview
 1. Silicon Interposer
 2. Embedded Bridge
 3. Fan-Out
4. Adaptive Patterning™
Introduction
5. Design Study
6. Follow Up Work



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1 Introductions



Robin Gabriel – Solutions Architect, AP Studio
Jan Kellar – Sr. Director of Applications & Design



Keith Felton – Product Marketing Manager, High Density Advanced IC Packaging
Ian Gabbitas – Applications Engineer, IC Packaging



ASE GROUP
John Hunt – Sr. Director of Engineering, Marketing & Technical Promotion
Lihong Cao – Director, Corporate Technology Development

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2 Background

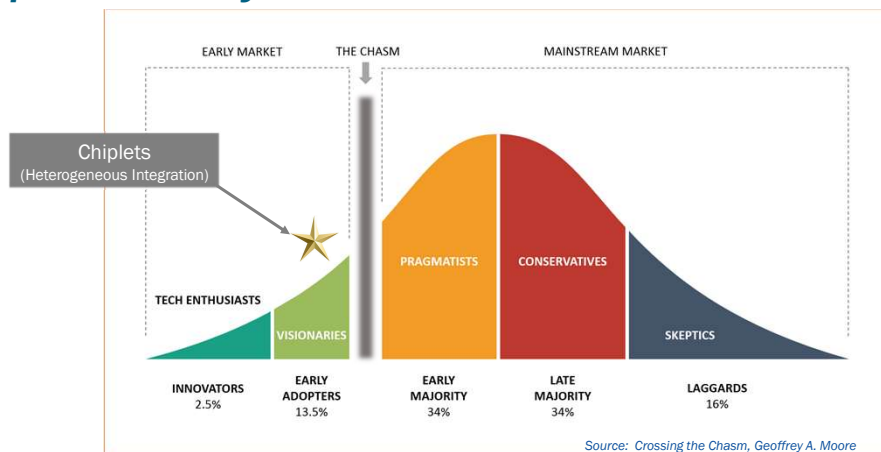
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Adoption Life Cycle



- Chiplets are close to crossing the chasm
- Achieving cost-effective high-density integration is key

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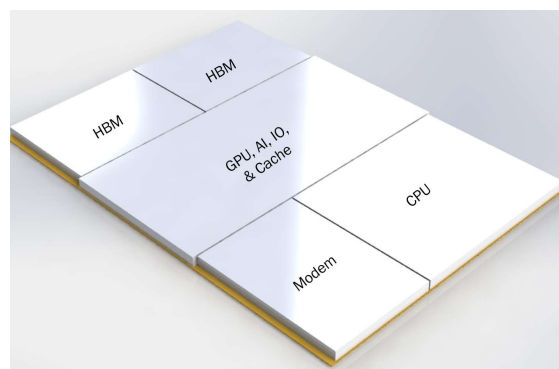
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The Chiplet Integration Race

Key Competition Factors

1. Cost
2. Yield
3. Scalability



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3 Technology Overview and Comparison

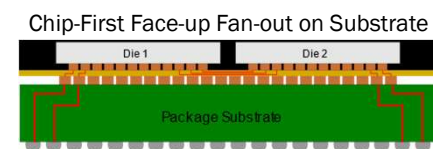
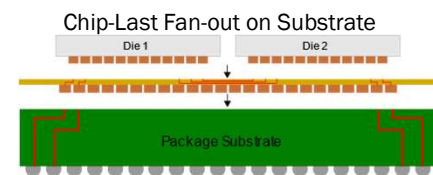
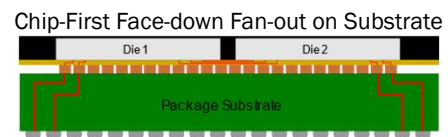
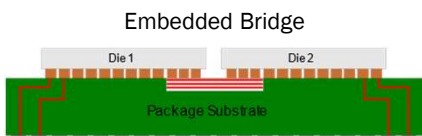
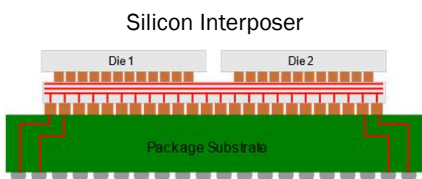
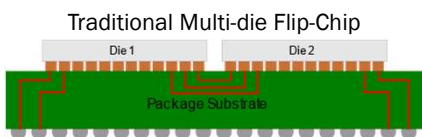
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Competitors

Heterogenous Integration Solutions



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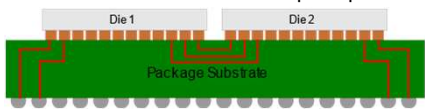
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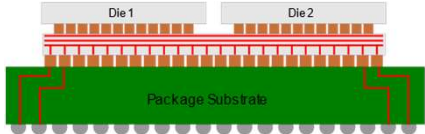
Competitors

Heterogenous Integration Solutions

Traditional Multi-die Flip-Chip



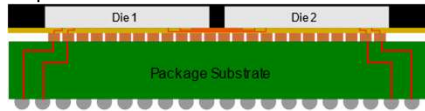
Silicon Interposer



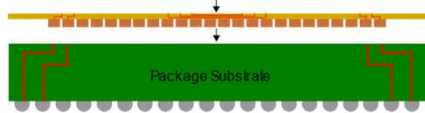
Embedded Bridge



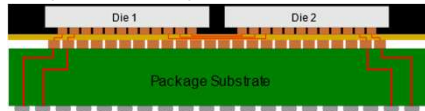
Chip-First Face-down Fan-out on Substrate



Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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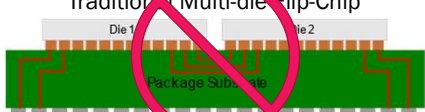
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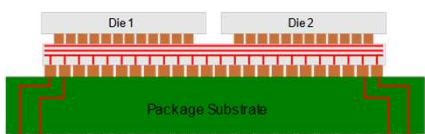
Competitors

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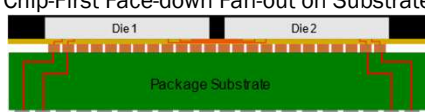
Silicon Interposer



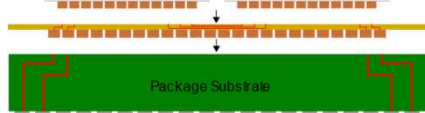
Embedded Bridge



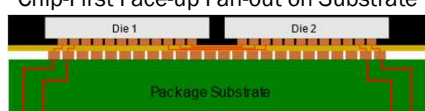
Chip-First Face-down Fan-out on Substrate



Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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Competitors

Heterogenous Integration Solutions

Traditional Multi-die Flip-Chip

Silicon Interposer

Embedded Bridge

Chip-First Face-down Fan-out on Substrate

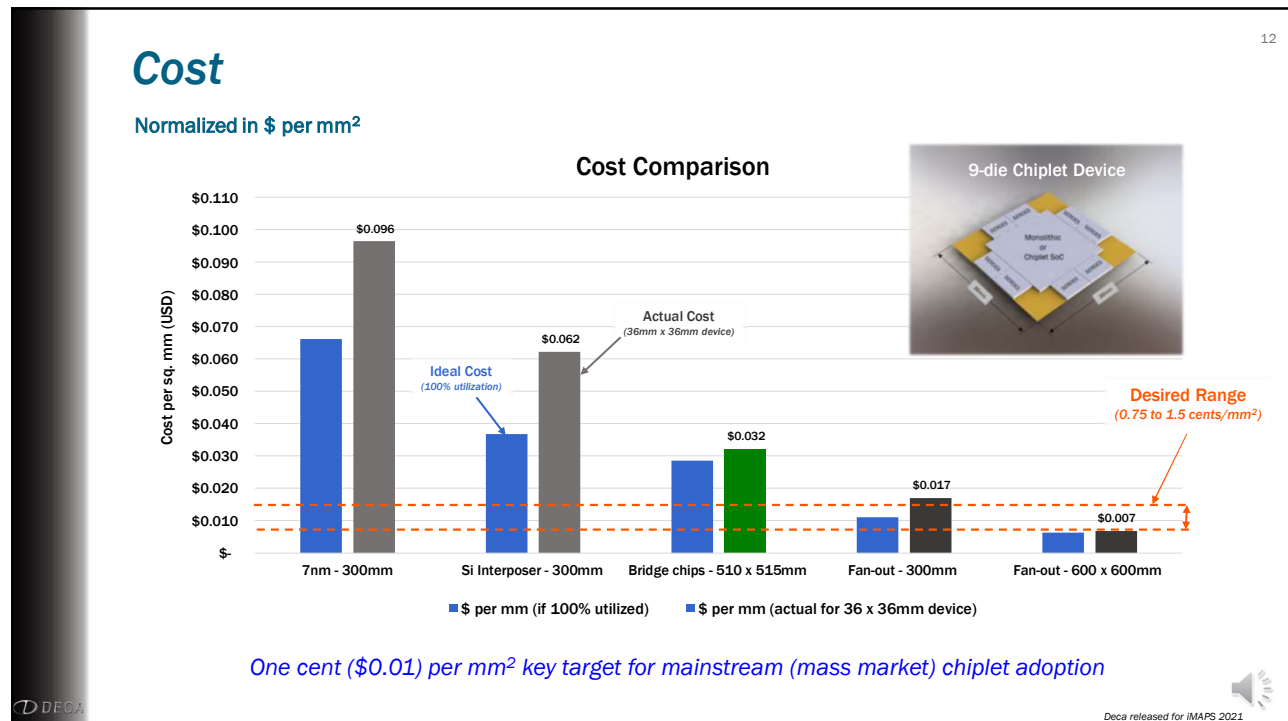
Chip-Last Fan-out on Substrate

Chip-First Face-up Fan-out on Substrate

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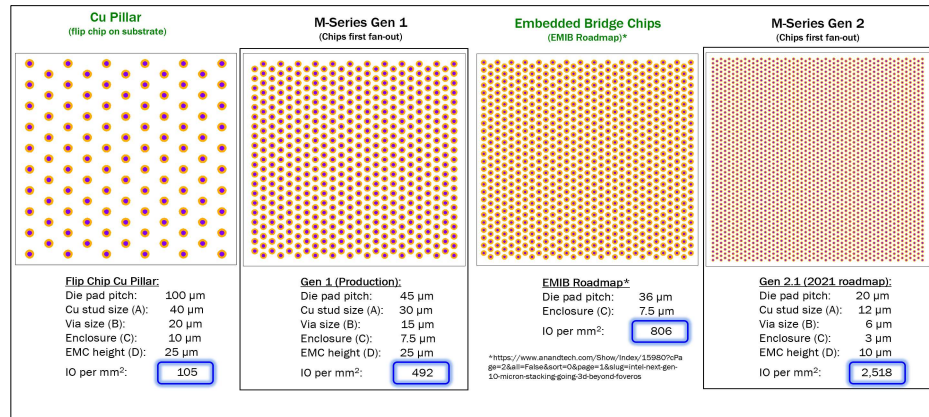
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Scalability

Minimum Die Pad Pitch Supported



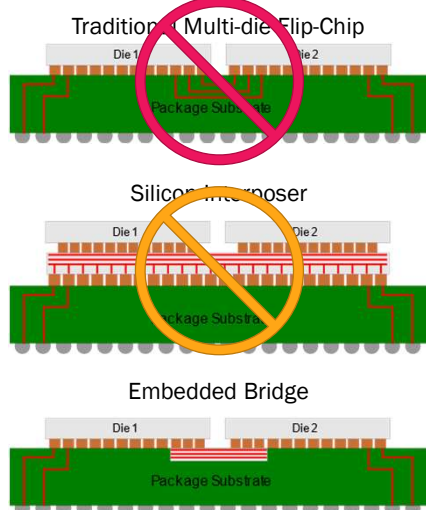
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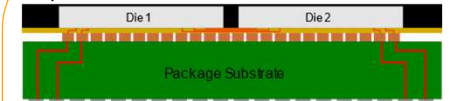
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Competitors

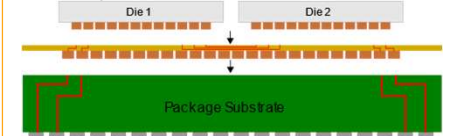
Heterogenous Integration Solutions



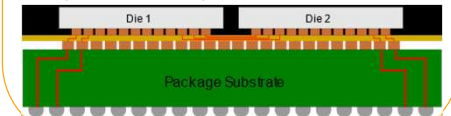
Chip-First Face-down Fan-out on Substrate



Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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Heterogenous Integration Solutions

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Traditional Multi-die Flip-Chip

Chip-First Face-down Fan-out on Substrate

Silicon Interposer

Chip-Last Fan-out on Substrate

Embedded Bridge

Chip-First Face-up Fan-out on Substrate

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Chip-First Face-down Fan-out on Substrate

Yield - Planarity

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Chip-first face-down

Chip-first face-up

5.5um

11um

70.09um

Cu RDL

EMC

Silicon Device

SE QA LAB WD15.7mm 15.0kV x1.5k 20um

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Competitors

Heterogenous Integration Solutions

Traditional Multi-die Flip-Chip

Silicon Interposer

Embedded Bridge

Chip-First Face-down Fan-out on Substrate

Chip-Last Fan-out on Substrate

Chip-First Face-up Fan-out on Substrate

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Chip-Last Fan-out on Substrate

- Provides an opportunity to integrate known-good die (KGD) onto a known-good substrate
- Viewed as a simple extension of traditional substrate technology using solder chip-attach
- In practice, significantly more complicated than the traditional flip-chip laminate process with addition of a temporary carrier, RDL build-up, chip attach, molding, and carrier removal
- Additionally, high precision low-throughput thermo-compression die attach is typically required
- The solder-metal interface required for flip-chip bumping adds electrical discontinuities in the signal path

Wafer Bumping **Wafer Dicing** **Trace & Pad Formation** **Flip Chip & Molding** **Chip Last Fan Out Backend**

*Courtesy of ASE

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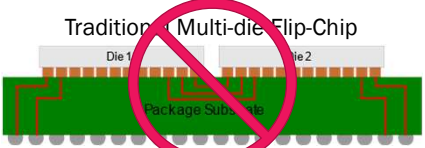
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Competitors

Heterogenous Integration Solutions

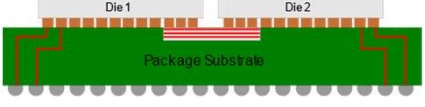
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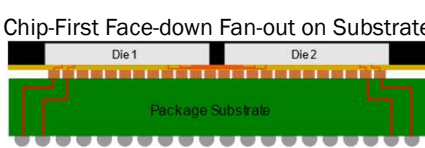
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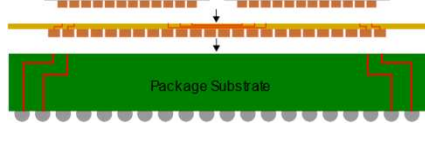
Embedded Bridge



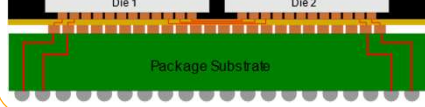
Chip-First Face-down Fan-out on Substrate



Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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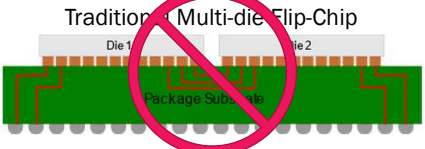
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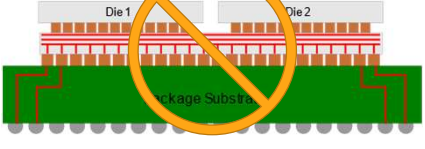
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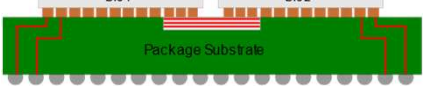
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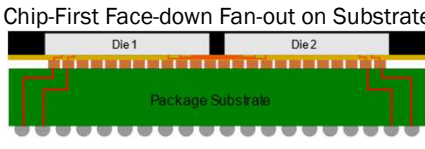
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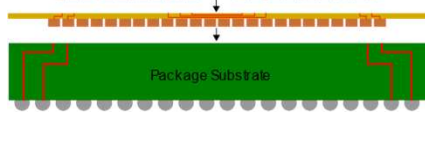
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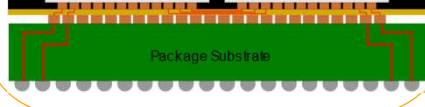
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Chip-First Face-up Fan-out on Substrate



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Yield

The Die Shift Problem - #1 Concern

1. Die placement offset
2. Displacement during molding

Designed position (nominal)

Actual position (with chip-attach tolerance & mold displacement)

Die placement tolerance X, Y, & rotation (relative to nominal)

Mold displacement (during compression molding process)

Actual position

Designed position (nominal)

Die shift is the displacement from designed position to actual position

Die shift includes combined chip-attach tolerance and mold displacement

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Cost

Die Attach Capital Cost

(6x6mm Package, 11 panels per hour on 600mm)

Capital Cost (\$ Millions)

Production Capacity
3 k panels per month
35 million units per month

With Adaptive Patterning

Capital for Conventional Fan-out Line

Capital cost with high precision die attach

Pareto of top five capex items

Capital for M-Series Fan-out Line

Capital cost with Adaptive Patterning™

Pareto of top five capex items

Chip Attach Equipment Options

Very high accuracy	± 3µm @ 3σ	\$1.1M	2,000 CPH
High accuracy	± 8µm @ 3σ	\$0.9M	5,000 CPH
Moderate accuracy	± 15µm @ 3σ	\$1.3M	22,000 CPH

Adaptive Patterning enables an effective ± 3µm @ 3σ performance using the 22,000 CPH machine

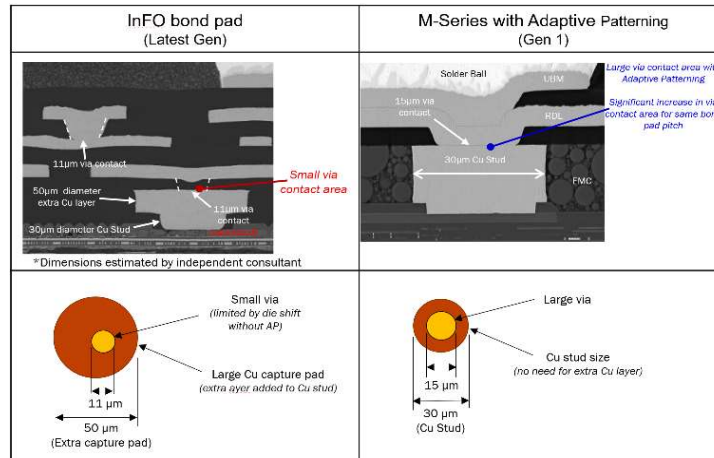
10X reduction in highest capex process with Adaptive Patterning

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Scalability

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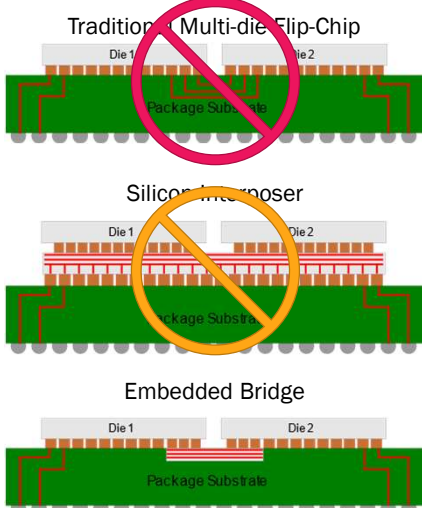
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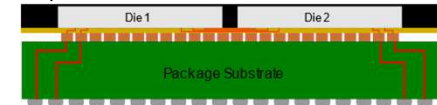
Competitors

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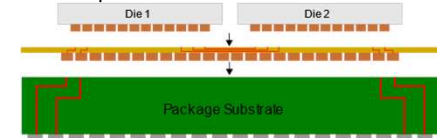
Heterogenous Integration Solutions



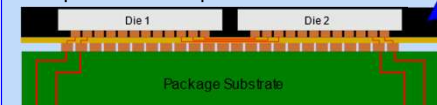
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Chip-Last Fan-out on Substrate



Chip-First Face-up Fan-out on Substrate



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➡ 4 Adaptive Patterning

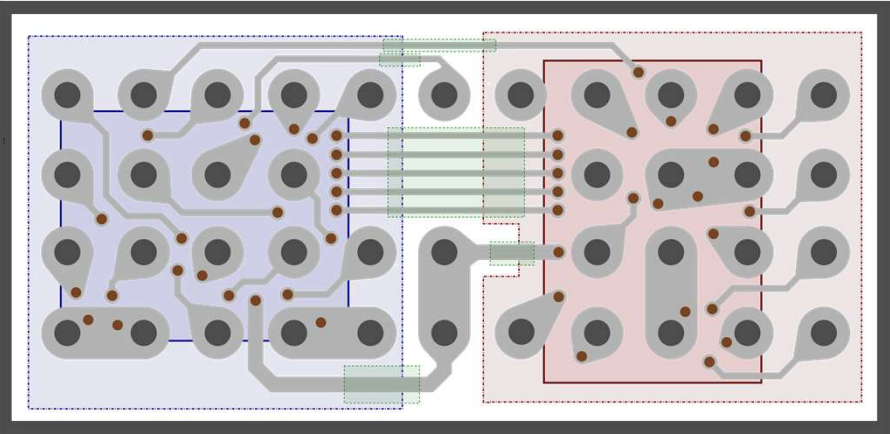

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Adaptive Patterning

Design



The diagram illustrates the design of an Adaptive Patterning interconnect. It shows two die, Die 1 (left, light blue) and Die 2 (right, light red), connected by an Adaptive Route Region (ARR) in the center. The legend identifies the following components:

- PM1 (PVIA1)
- UBM
- CuPPI (PRDL1)
- PM2 (PUBV)
- Die 1 Shadow
- Die 1 Shift Region (SR)
- Die 2 Shadow
- Die 2 Shift Region (SR)
- Adaptive Route Region (ARR)


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Adaptive Patterning

Die Shift

Die movement

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Adaptive Patterning

Die Shift

Die movement

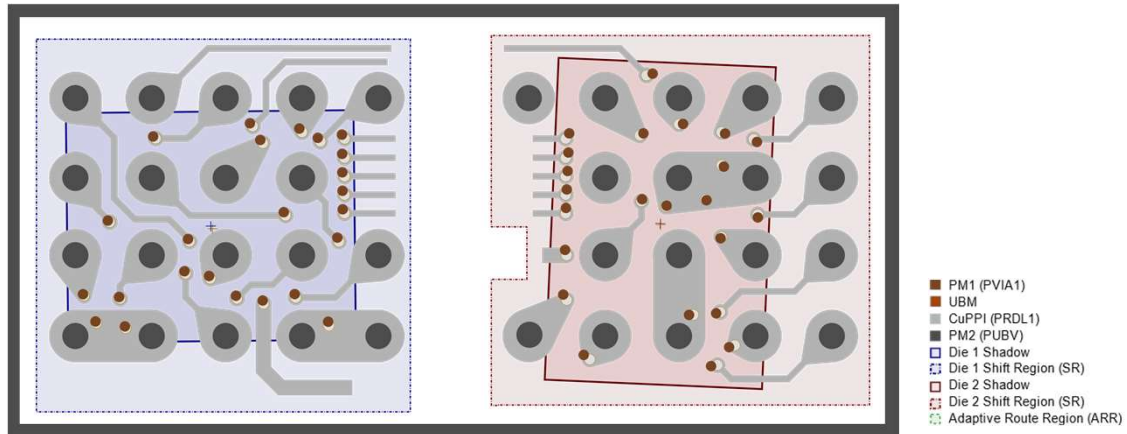
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Adaptive Patterning

Adaptive Alignment



Pattern is adaptively aligned to new die position

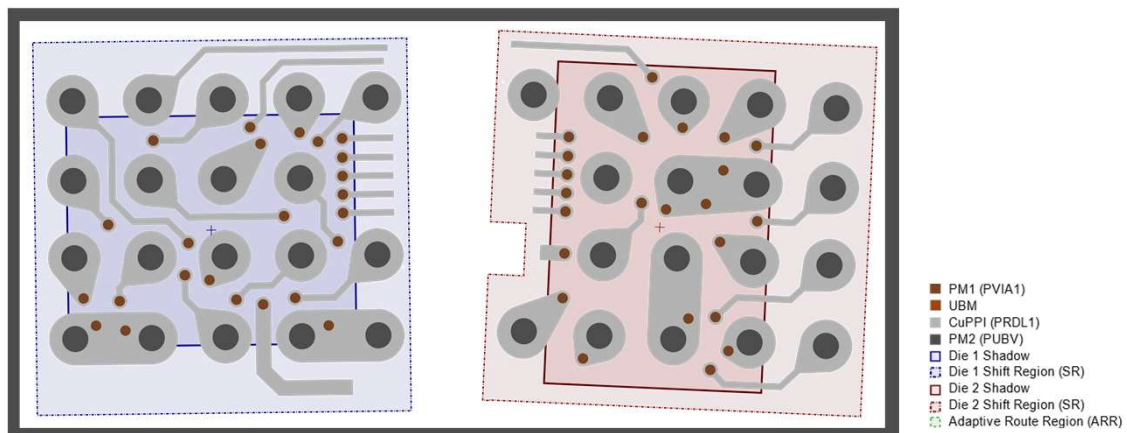
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Adaptive Patterning

Adaptive Alignment



Pattern is adaptively aligned to new die position

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Adaptive Patterning

Adaptive Alignment

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The diagram illustrates the process of adding fixed RDL (Reflowed Die Lead) to a chip layout. It shows two versions of a chip layout: the left version shows the initial layout with various components and regions, and the right version shows the layout after the addition of fixed RDL. The legend identifies the following components:

- PM1 (PVIA1)
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- CuPPI (PRDL1)
- PM2 (PUBV)
- Die 1 Shadow
- Die 1 Shift Region (SR)
- Die 2 Shadow
- Die 2 Shift Region (SR)
- Adaptive Route Region (ARR)

Addition of fixed RDL

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Adaptive Patterning

Adaptive Alignment

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Addition of fixed RDL

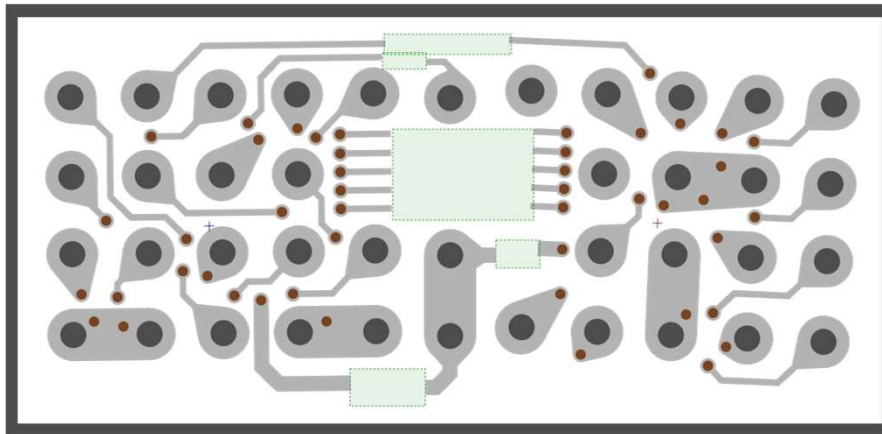
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Adaptive Patterning

Adaptive Routing



Adaptive routing is performed to complete connections

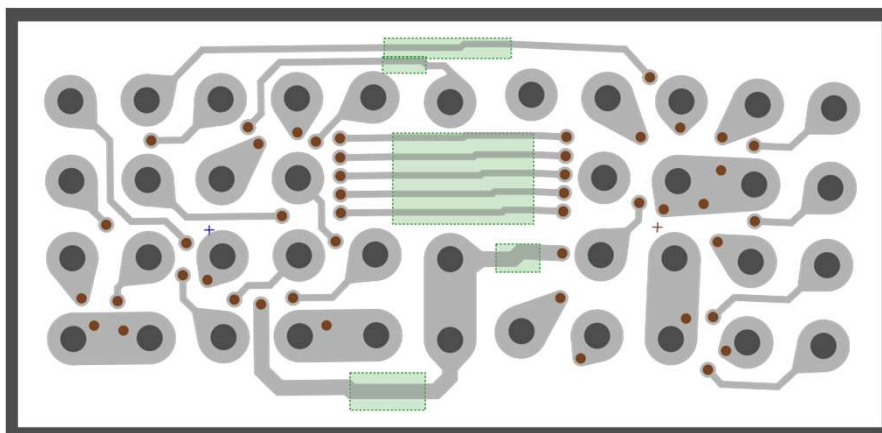
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Adaptive Patterning

Adaptive Routing



Adaptive routing is performed to complete connections

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➤ 5 Design Study

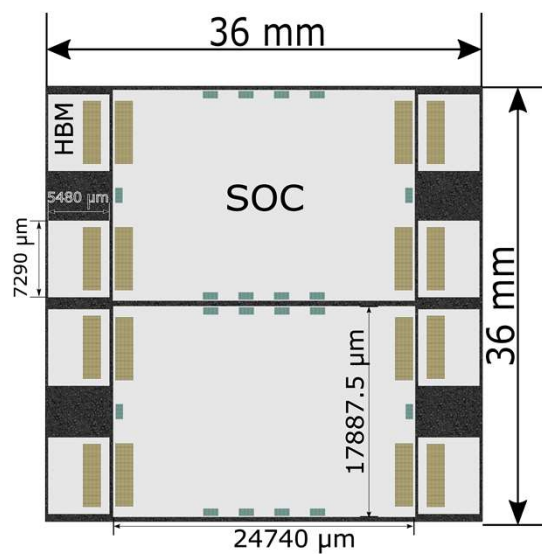
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Design Study

Concept



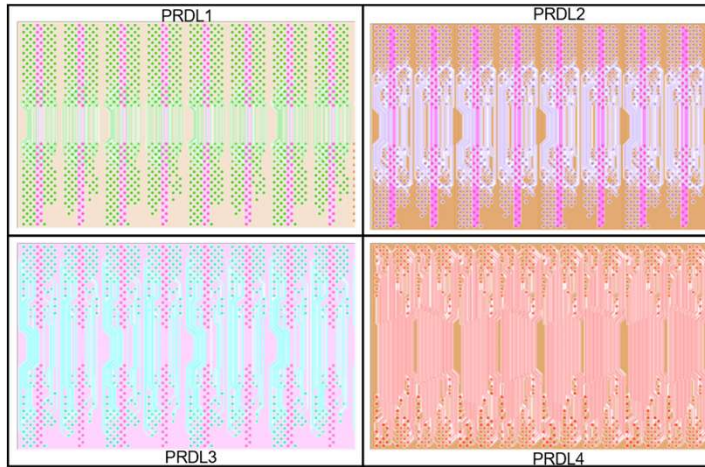
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Design Study

20µm Pitch Study



*planned follow up study on layer count reduction using PAA

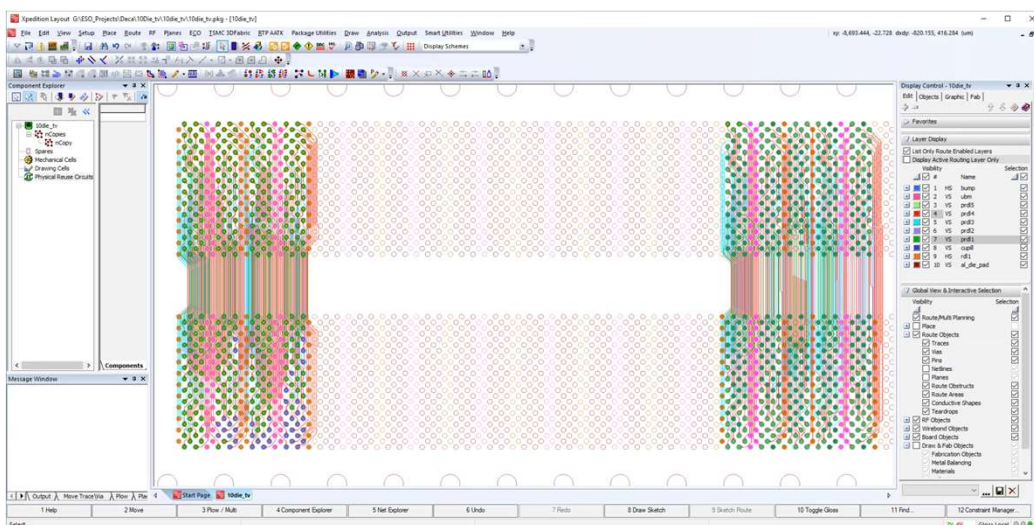
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Design in Xpediton

Building Interfaces with step and repeat (nCopy)



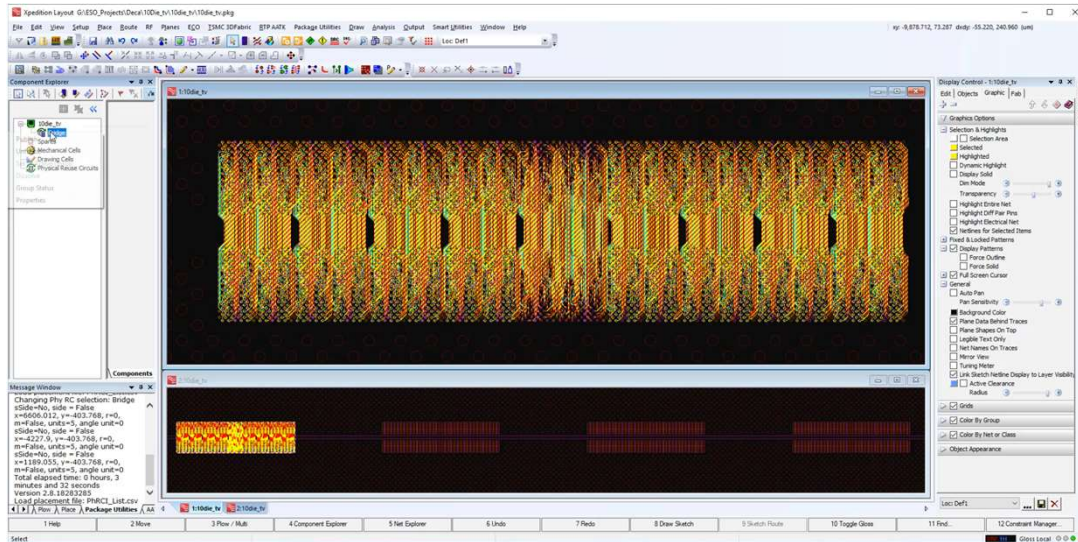
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Design in Xpediton – Physical Reuse Blocks

Interface Replication

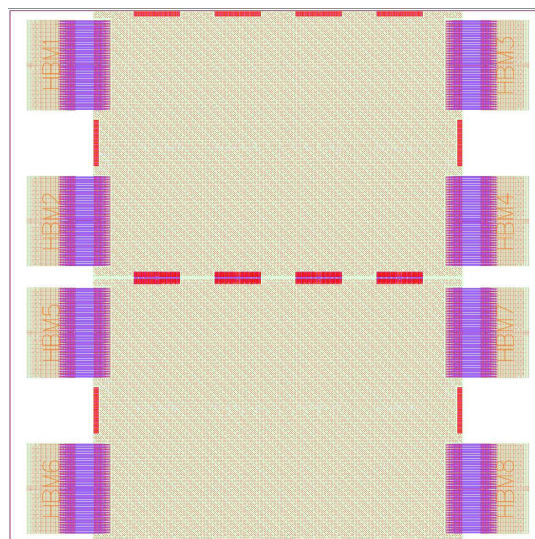


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Design Study



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➤ 6 Follow up Work and Conclusions

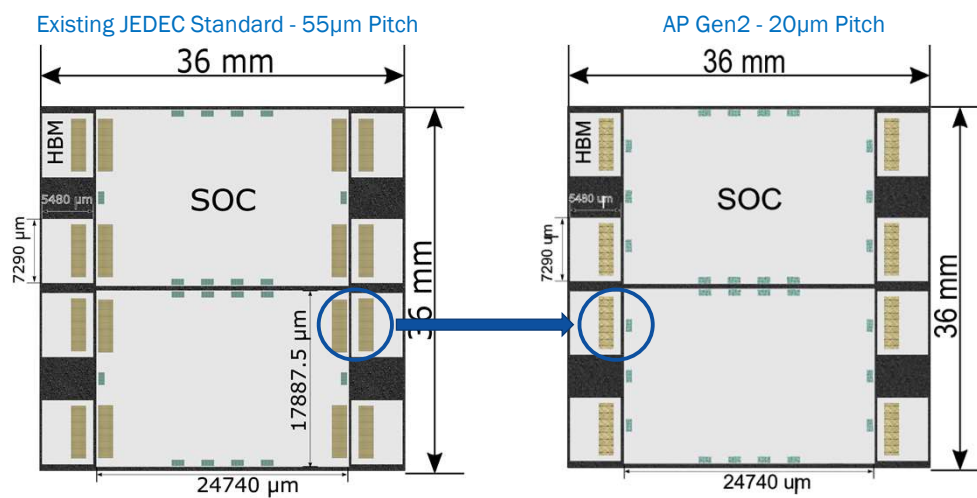
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Follow up

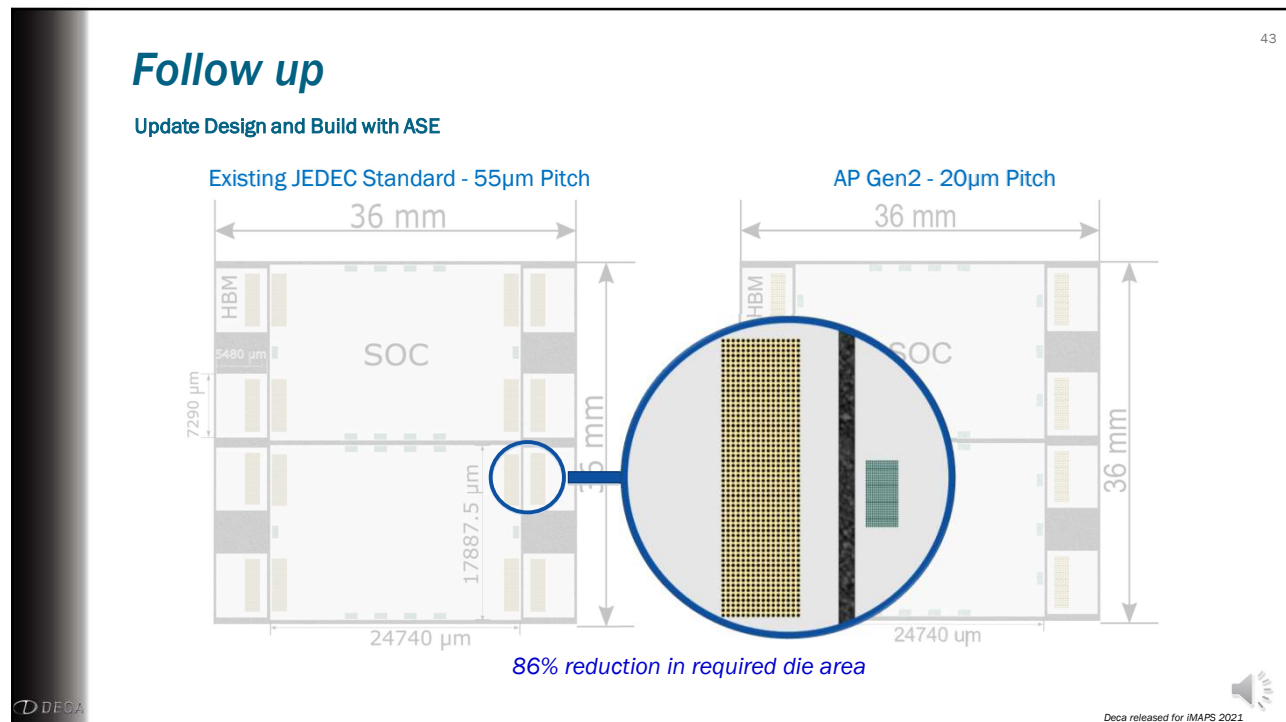
Update Design and Build with ASE



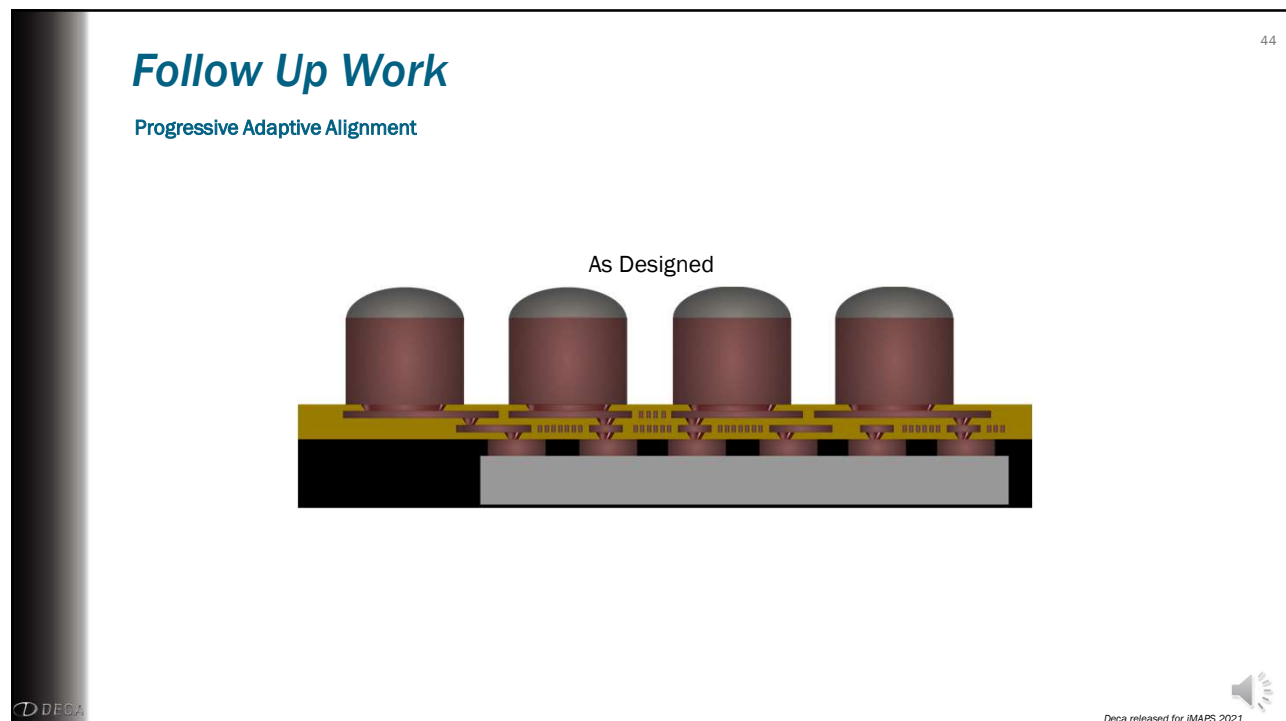
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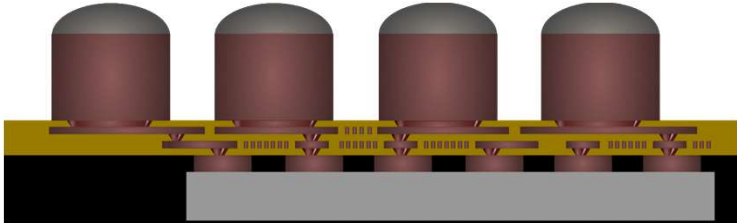
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Follow Up Work

Progressive Adaptive Alignment

Adaptive Alignment



The diagram illustrates the 'Adaptive Alignment' process. It shows four cylindrical components (dark red with grey domes) positioned on a yellow substrate. Below the substrate is a grey base. The components are aligned with the substrate, and the text 'Adaptive Alignment' is centered above them.

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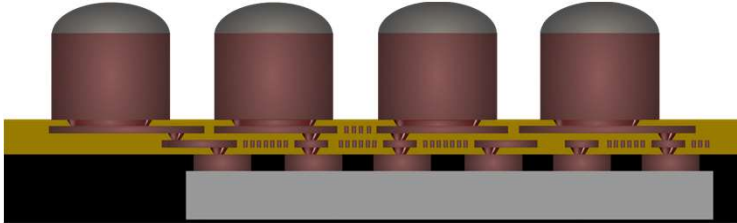
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Follow Up Work

Progressive Adaptive Alignment

Progressive Adaptive Alignment



The diagram illustrates the 'Progressive Adaptive Alignment' process. It shows four cylindrical components (dark red with grey domes) positioned on a yellow substrate. Below the substrate is a grey base. The components are aligned with the substrate, and the text 'Progressive Adaptive Alignment' is centered above them.

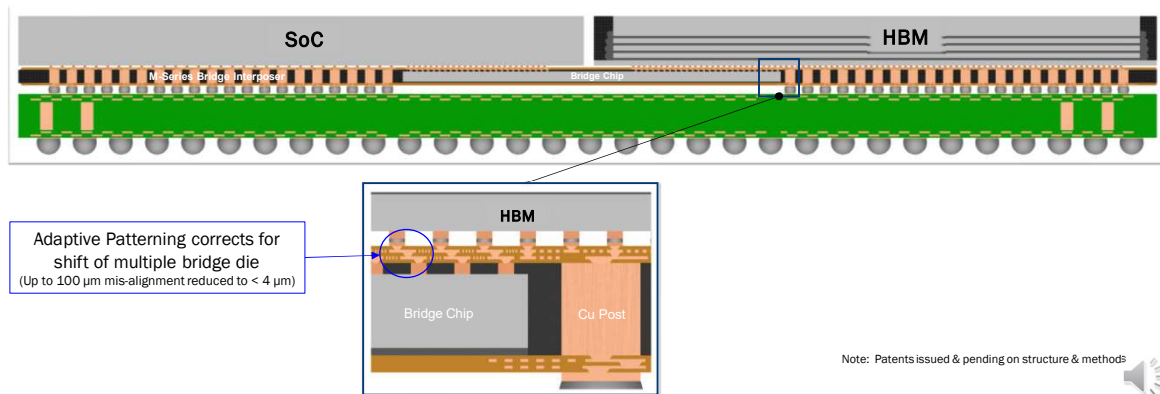
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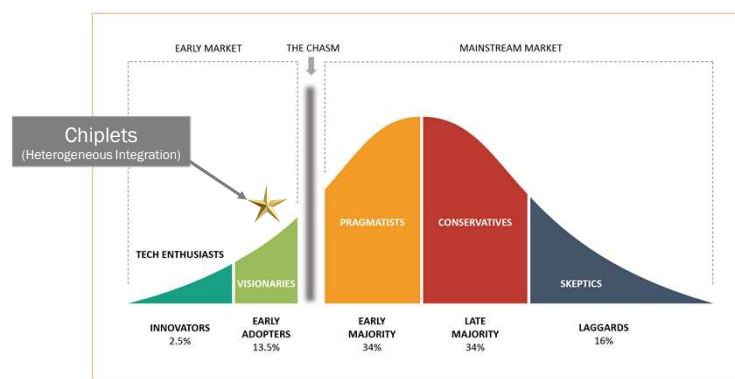
Follow Up

- Opportunity to combine fan-out and bridge chip technologies
- Integrating silicon bridge into chip-first fanout and using chip-last approach to place SOC's and HBM



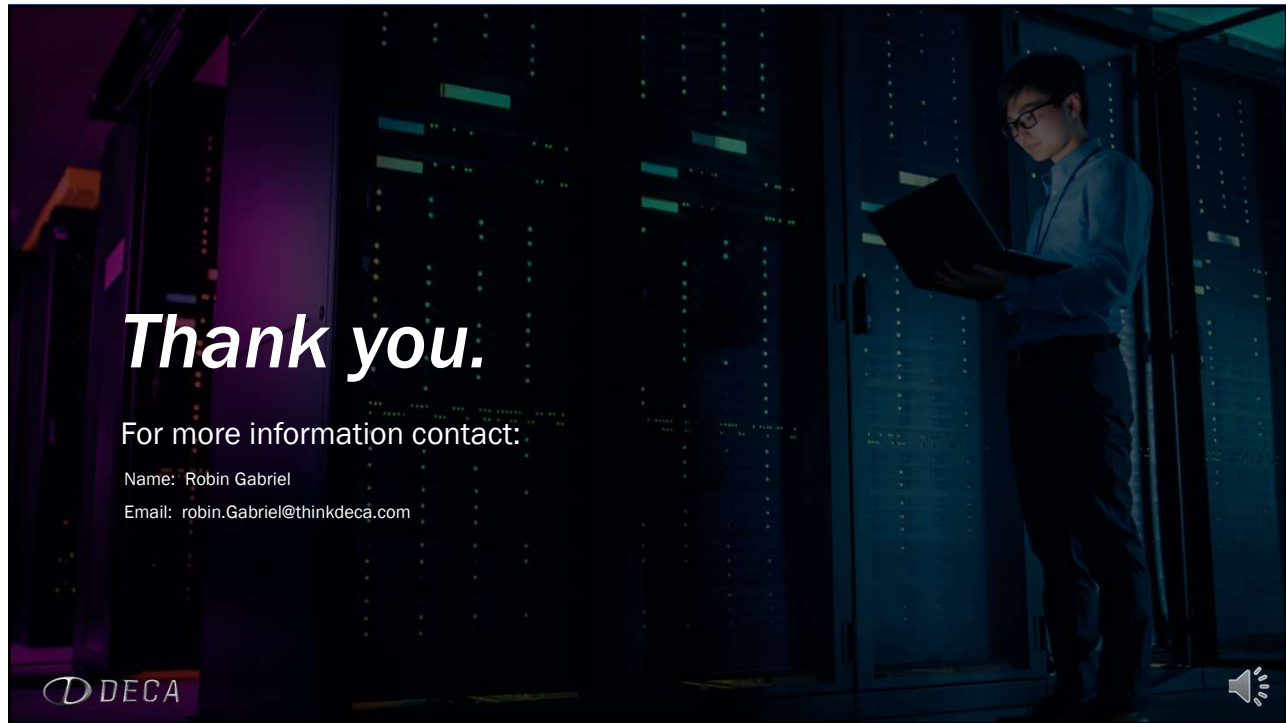
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Conclusion



- Chiplets are close to crossing the chasm to mainstream adoption but cost-effective high-density integration is necessary to do so
- Adaptive Patterning provides a way to break through these barriers and make the transition to mainstream adoption

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