Die-to-Die Interconnect Design and Simulation for 2.3D Organic Interposer Package

Cindy Muir, Intel Corp. (Bernd Waidhas, Abdallah Bacha, Carlton Hanna, Beth Keser)

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Cindy Muir

Analog Engineer
Technology Enablement Group
Intel Chandler, AZ

She works on the development of HSIO channel design creating EM models for analysis and characterization of electrical performance and SI.

She has worked several years in the Si industry where she first started with Motorola as a product engineer for RF Low Power products. This group was spun off to Freescale and then acquired by Fujistu where she began working on design and simulation of on chip magnetic devices and the wlcsp packages for RF transceivers. She joined Intel seven years ago with the most recent acquisition of the team. More recently she began interposer design for high-speed interconnects studying the EM impact on SI and signal quality using eye diagrams.

Cindy holds a master's degree in electrical engineering from Georgia Institute of Technology.

Bernd Waidhas

Principal Engineer Package Architecture
Technology Enablement Group
Intel Munich.

He works on definition, development and characterization of advanced package types like 2.xD/3D from external suppliers.

He started his business career at Siemens Semiconductors, later Infineon, in 1996, where he was working in several positions in package development such as package concept engineering and package project management mainly for wireless products and as Package Platform Owner responsible for Fine Pitch BGA roadmap.

He joined Intel with the acquisition of Infineon's Wireless Solutions Business in 2011.

Bernd holds a master's degree in electrical engineering from the Technical University Dresden. He has been granted 20 patents and several additional patents pending.

Agenda

- Introduction
- 2.3D High Density RDL Package Capabilities
- Die-to-Die Interconnect Design
- Electrical Simulation Model
- Results
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Heterogeneous Integration Background

- The disaggregation of large silicon SOCs into smaller silicon elements has been shown to have benefits in both silicon manufacturing yields and design scalability for high performance compute (HPC) applications
- The silicon elements are re-aggregated using advanced packaging technologies with high bandwidth die-to-die connections.

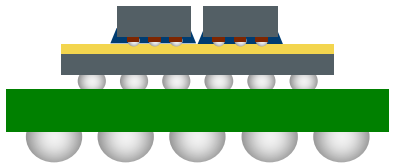
2.xD Package Architecture Overview

Si-Wafer Technology Based

Minimum 0.4µm Line / 0.4µm Space
Typical 2µm Via

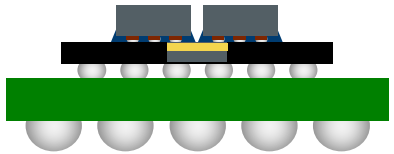
Si-Interposer

with TSV

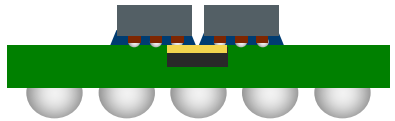


Si-Bridge

in Mold Interposer



in BGA Substrate

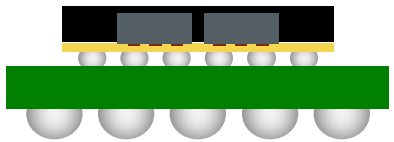


HD RDL Technology Based

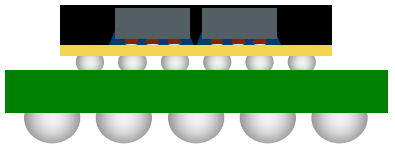
Typical 2µm Line / 2µm Space
Typical 10µm Via

HD-FO RDL Interposer

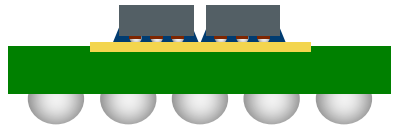
Chip First



Chip Last

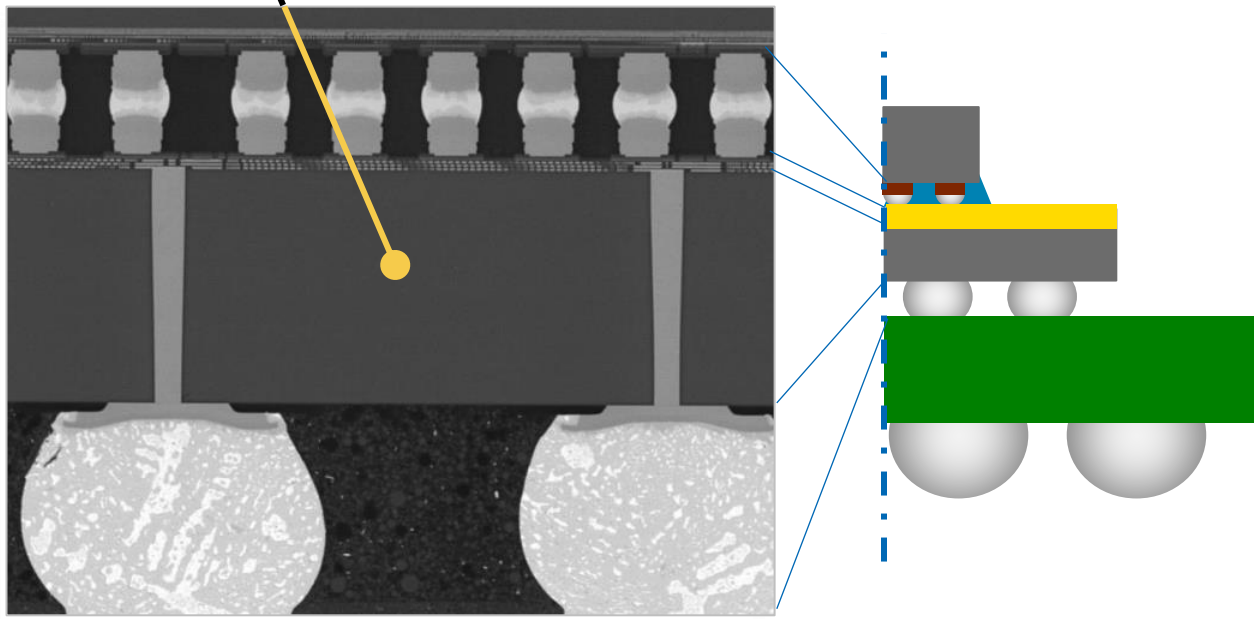


Hybrid Substrate



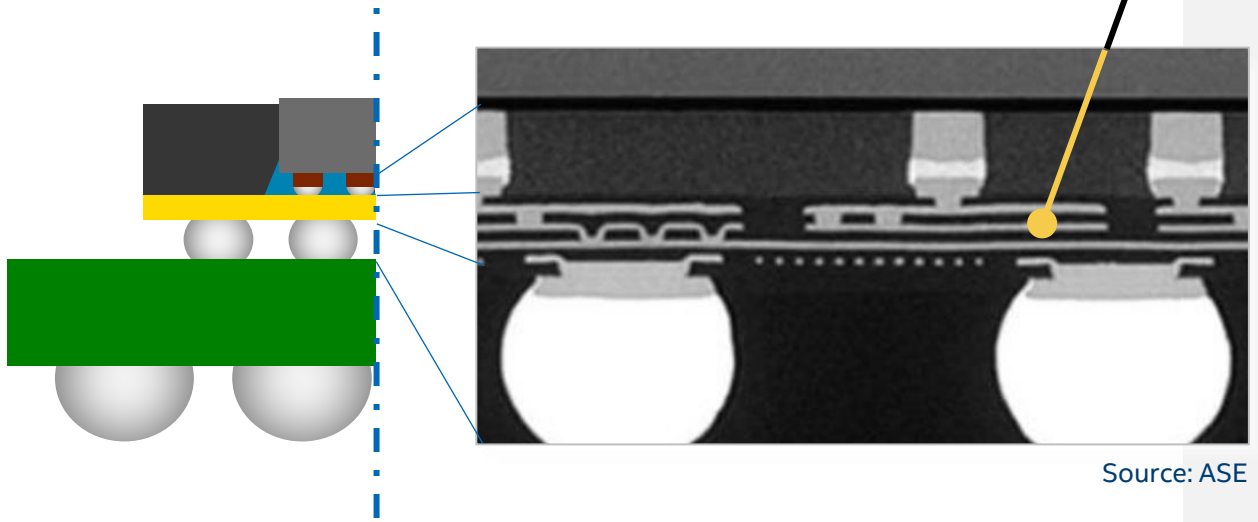
2.3D High Density RDL vs. 2.5D Si Interposer

Si Interposer (2.5D)



- Fine Line/Space Routing Capability
- Optional Capacitor Integration in Interposer

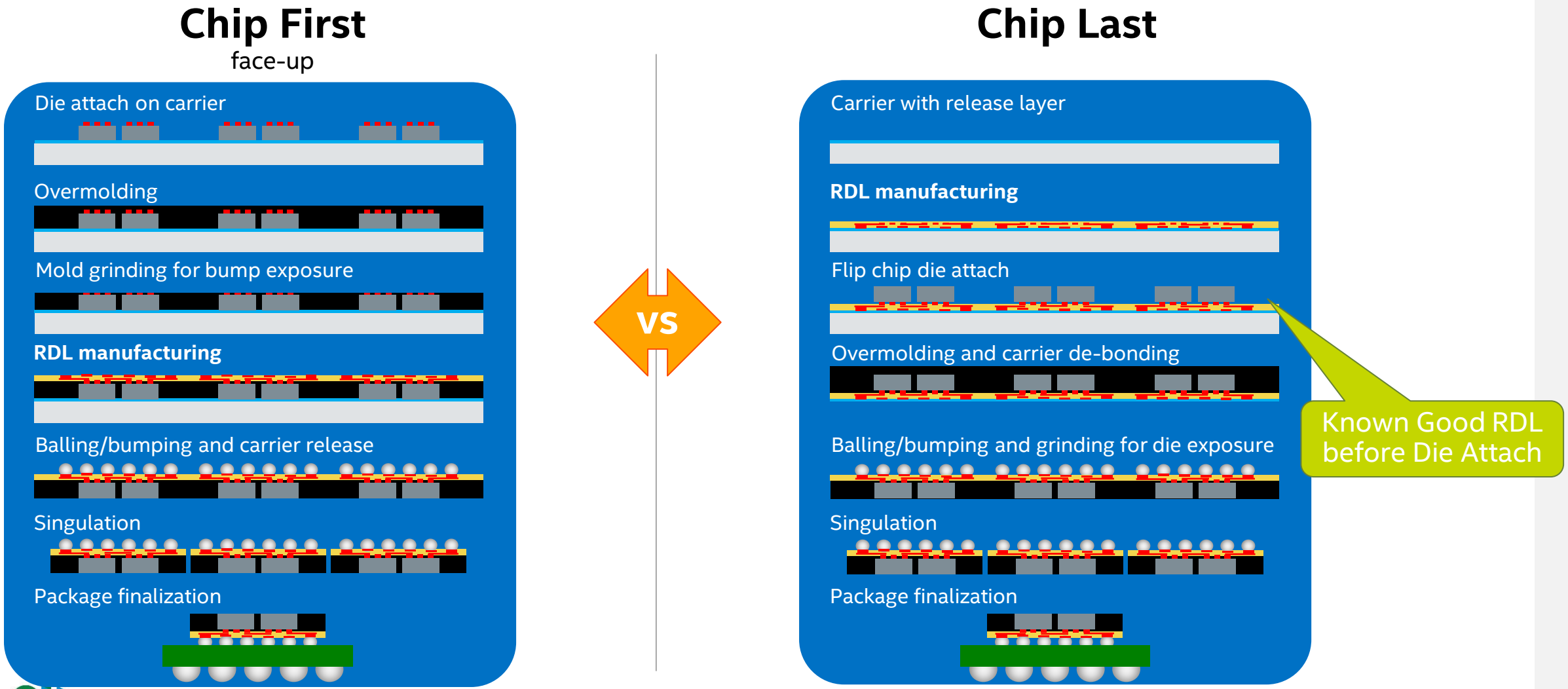
HD-FO RDL Interposer (2.3D)



Source: ASE

- Electrical Performance Improvement by TSV-less Technology
- Less Restrictions in Maximum Interposer Size
- Cost Reduction Opportunity vs. 2.5D Si Interposer

2.3D HD-FO RDL Interposer Process Flow



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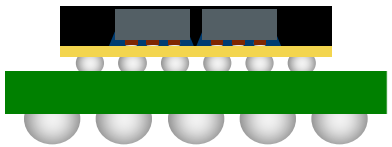
HD-FO RDL Interposer

Chip First

Chip Last



Hybrid Substrate

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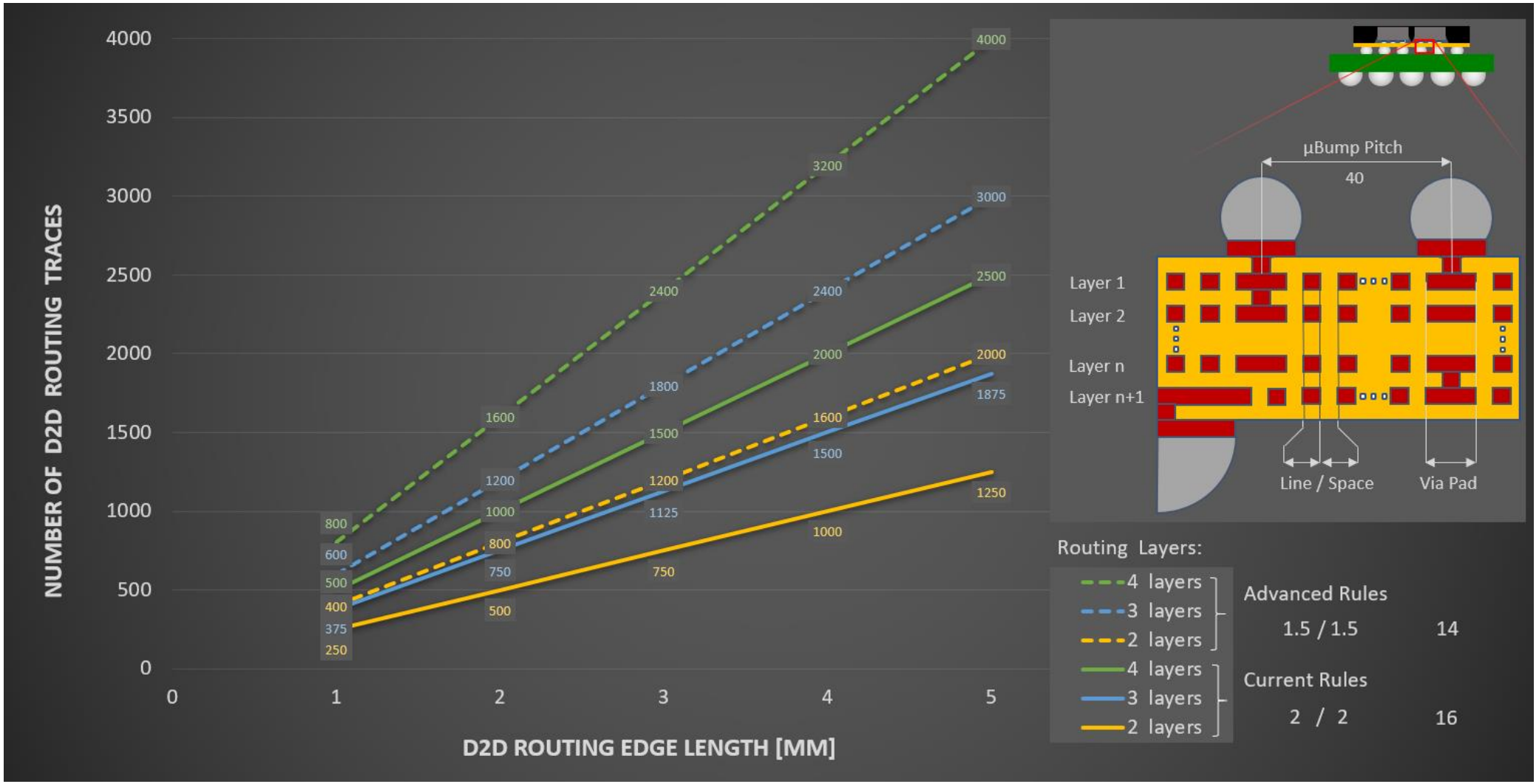
2.3D Routing Capability – Simplified Model



Interconnect Scaling Classification

- IEEE Heterogeneous Integration Roadmap
  - Peripheral Interconnect Pitch Roadmap for Solder based Interconnects

Generations		1	2	3	4	5
Raw Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (µm)	55	50	40	35	30
	IO/mm	500	667	1000	1500	2000
	IO/mm^2	331	400	625	816	1111
Signaling Speed (Gbps)		2	3	4	5.33	8

Source: https://eps.ieee.org/images/files/HIR_2019/HIR1_ch22_2D-3D.pdf

2.3D Capability

4L RDL, L/S 1.5/1.5
G-S-G

4L RDL, L/S 1.5/1.5
G-S-S-G

2.3D Interposer Characteristic

- 2.3D HD-FO Interposer packaging is for some applications an attractive alternative vs. 2.5D Si passive interposer
- The technology has the capabiliy up to 500 signals/mm shoreline density on 4 RDL layers
- All major OSATs as well as the SiFos are in 2.3D package development, HVM for chip last is forcasted for Q1'21
- Future economy of scale is possible by change from wafer format to panel level production

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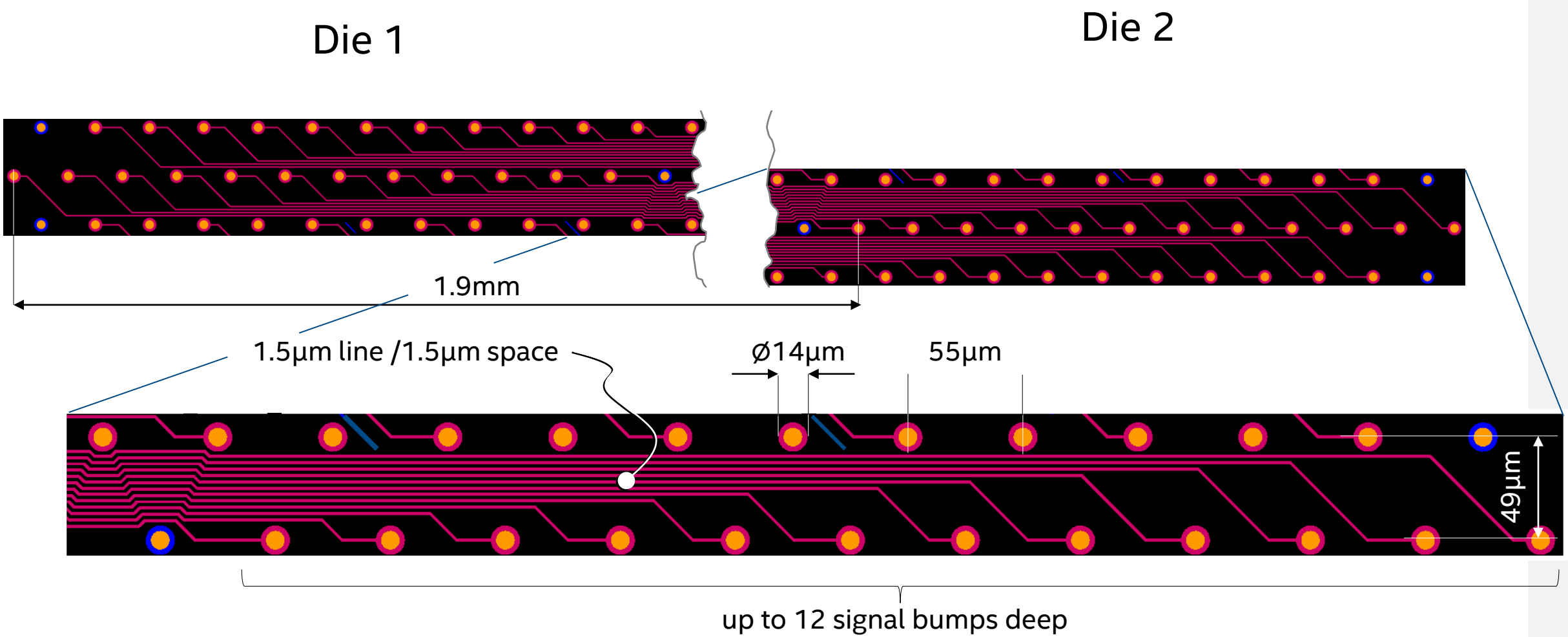
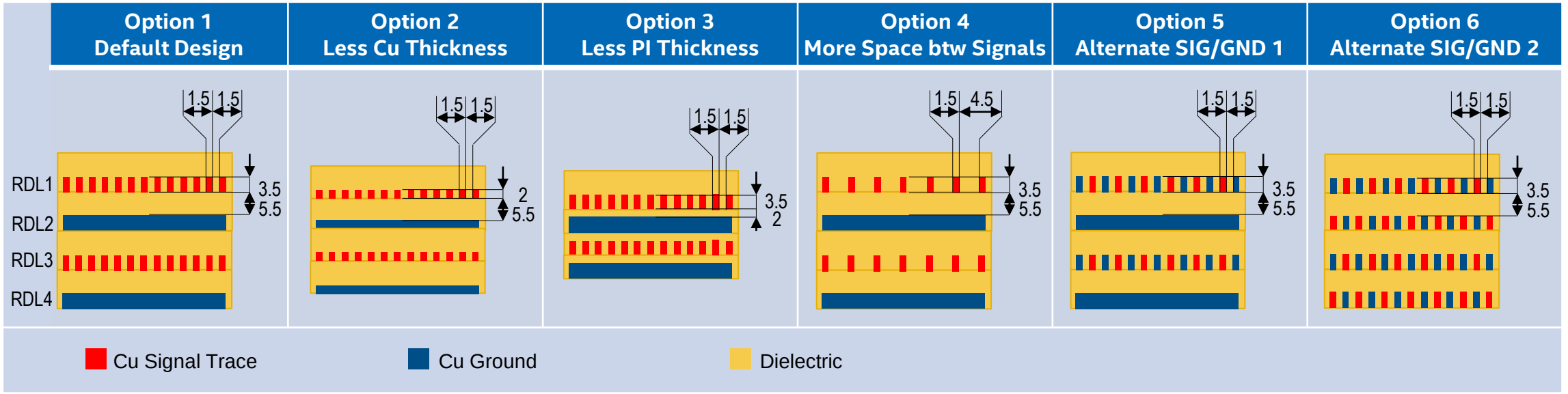
Die-to-Die Interconnect Routing



RDL Layer Stack-up and Die-to-Die Design



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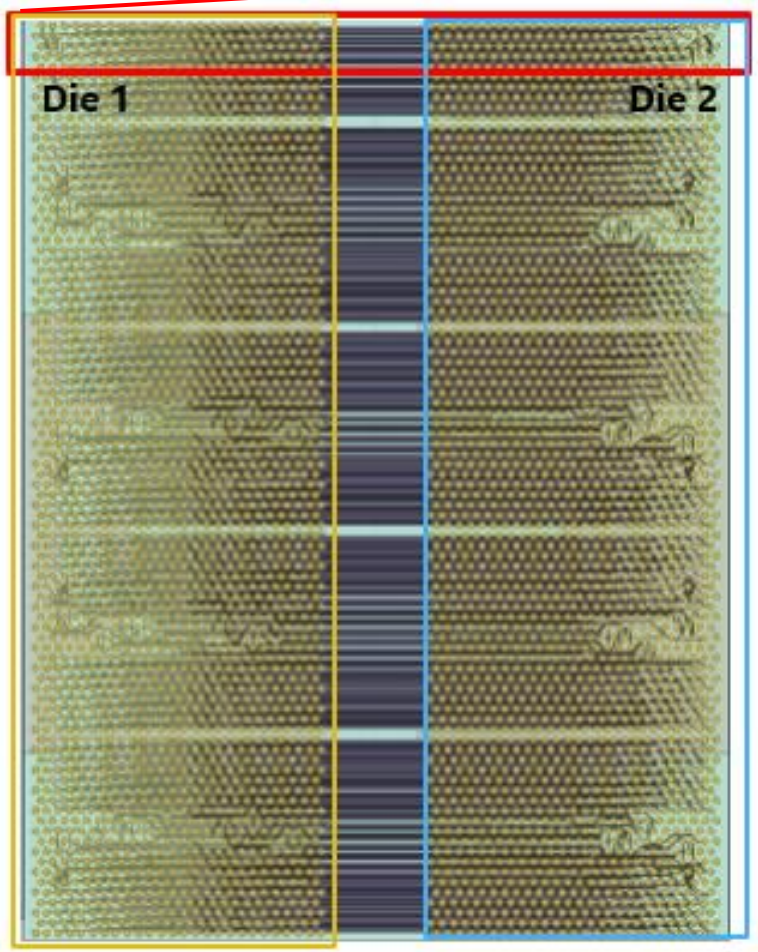
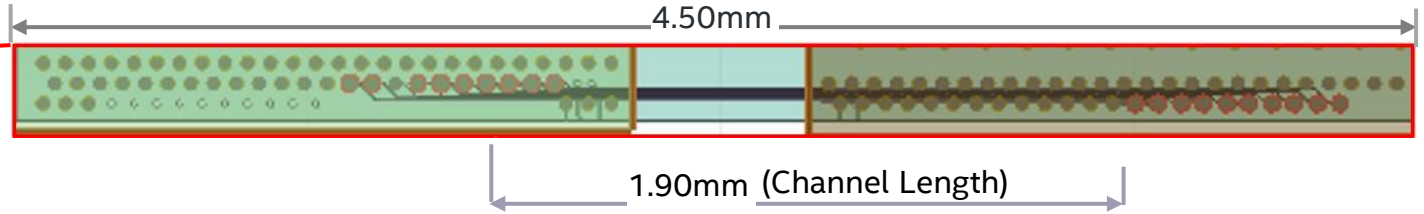
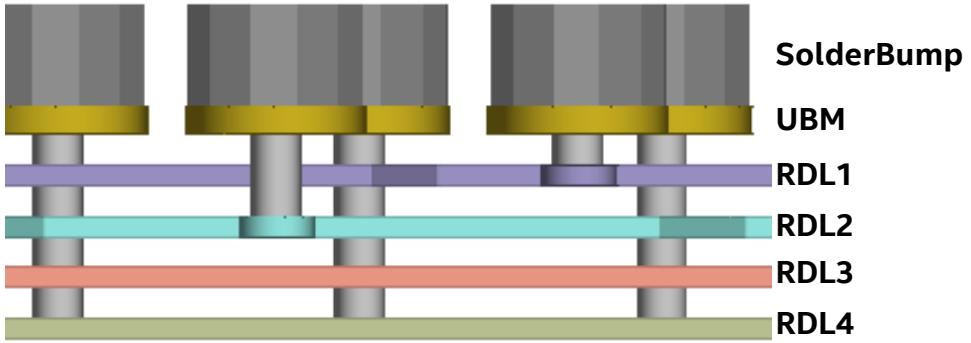
2.3D interposer GSG topology for EM simulation



Sample for Simulation

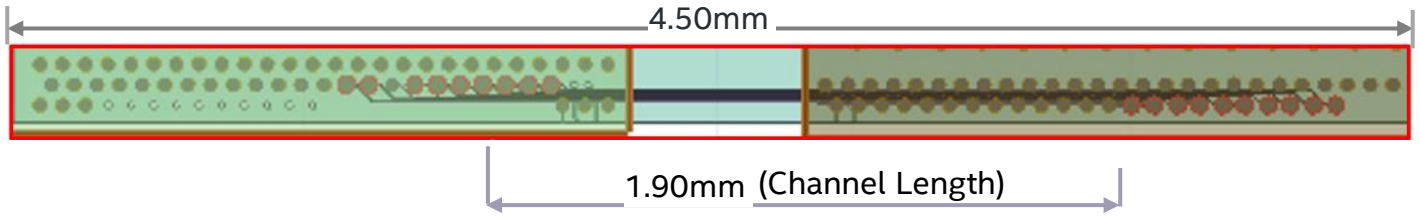


Stack-up

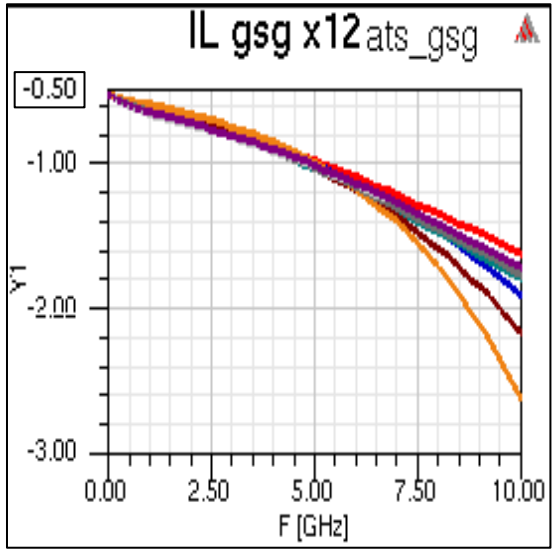


2.3D Insertion Loss, Return Loss and Isolation

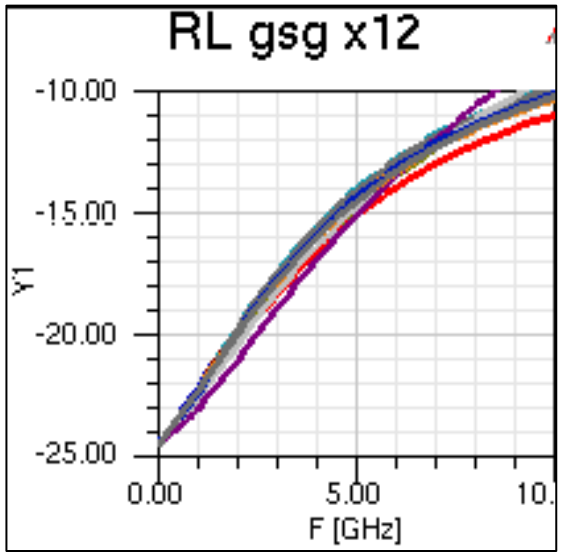
Sample for Simulation



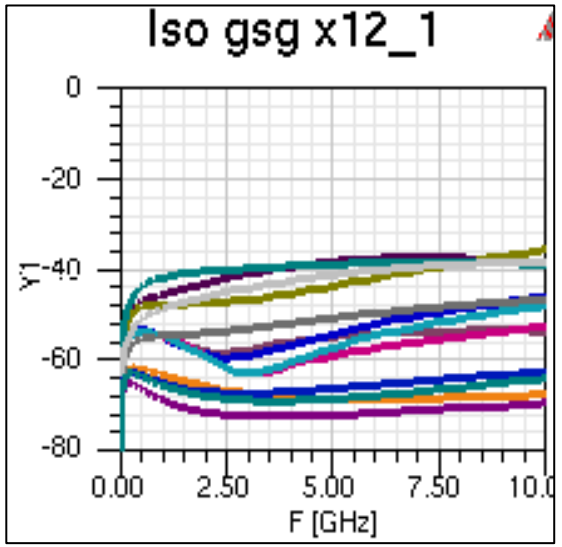
Insertion Loss



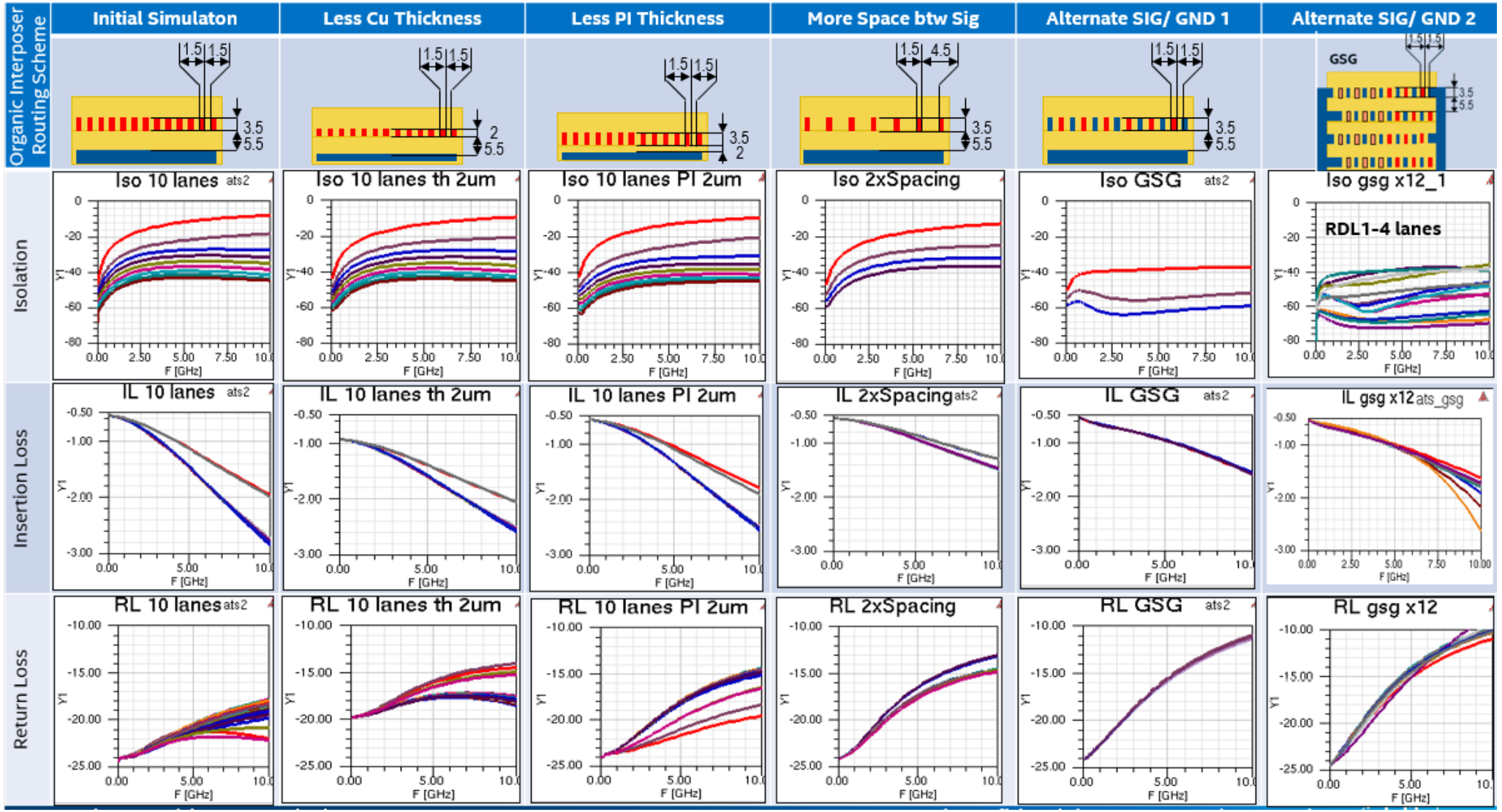
Return Loss



Isolation



Electrical Differences per Design Variation



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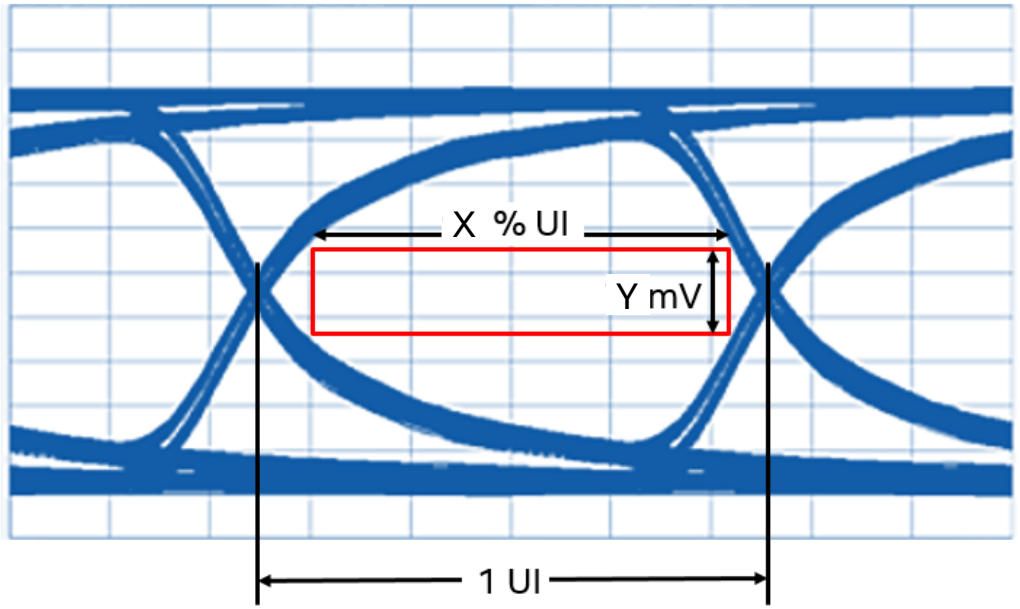
General SI Specifications:

Low-swing TX Driver with a nominal supply voltage.

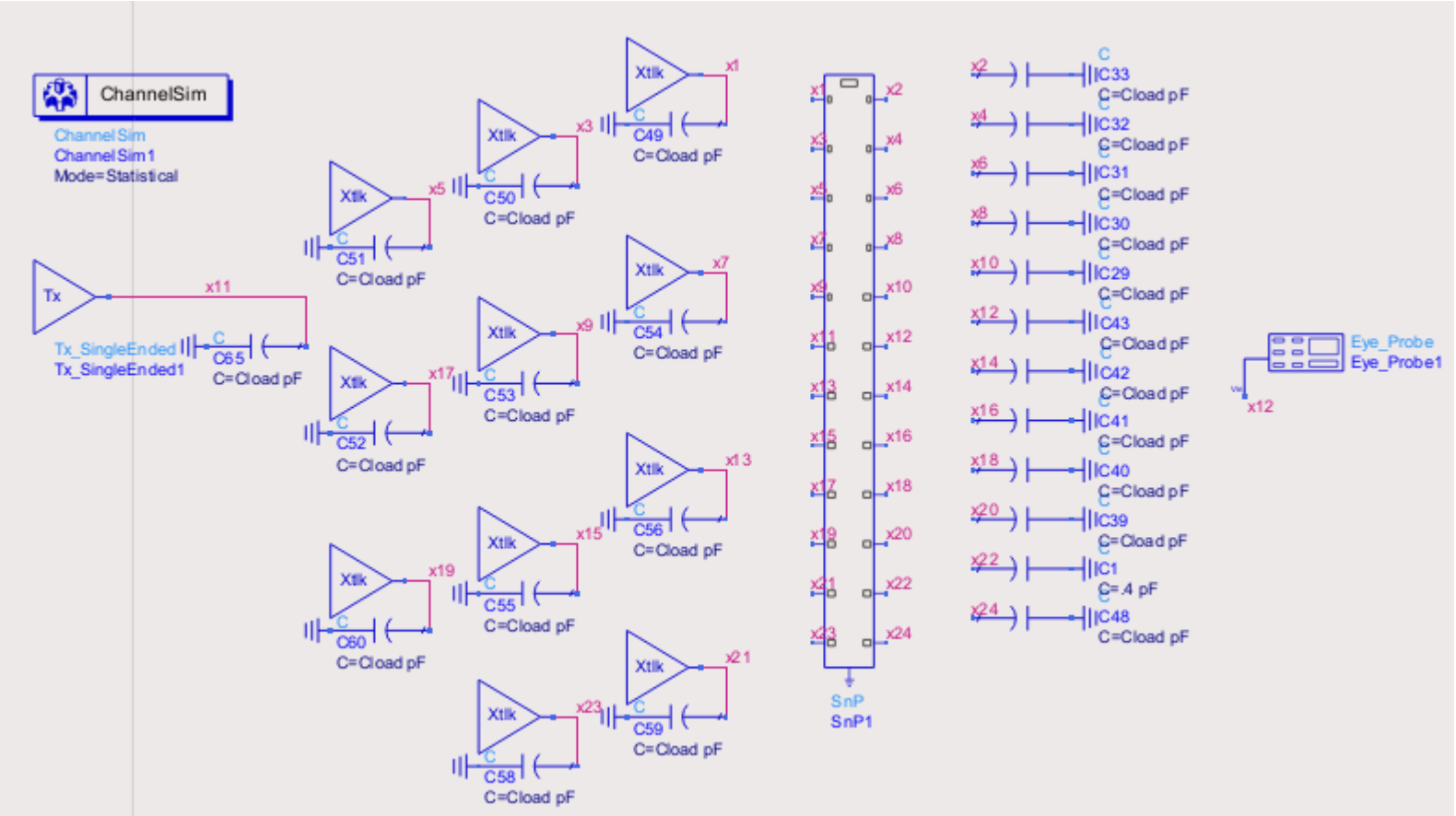
~500-1000mV



Bit Rate: >5.4Gbps
Load: 20-40 ohm

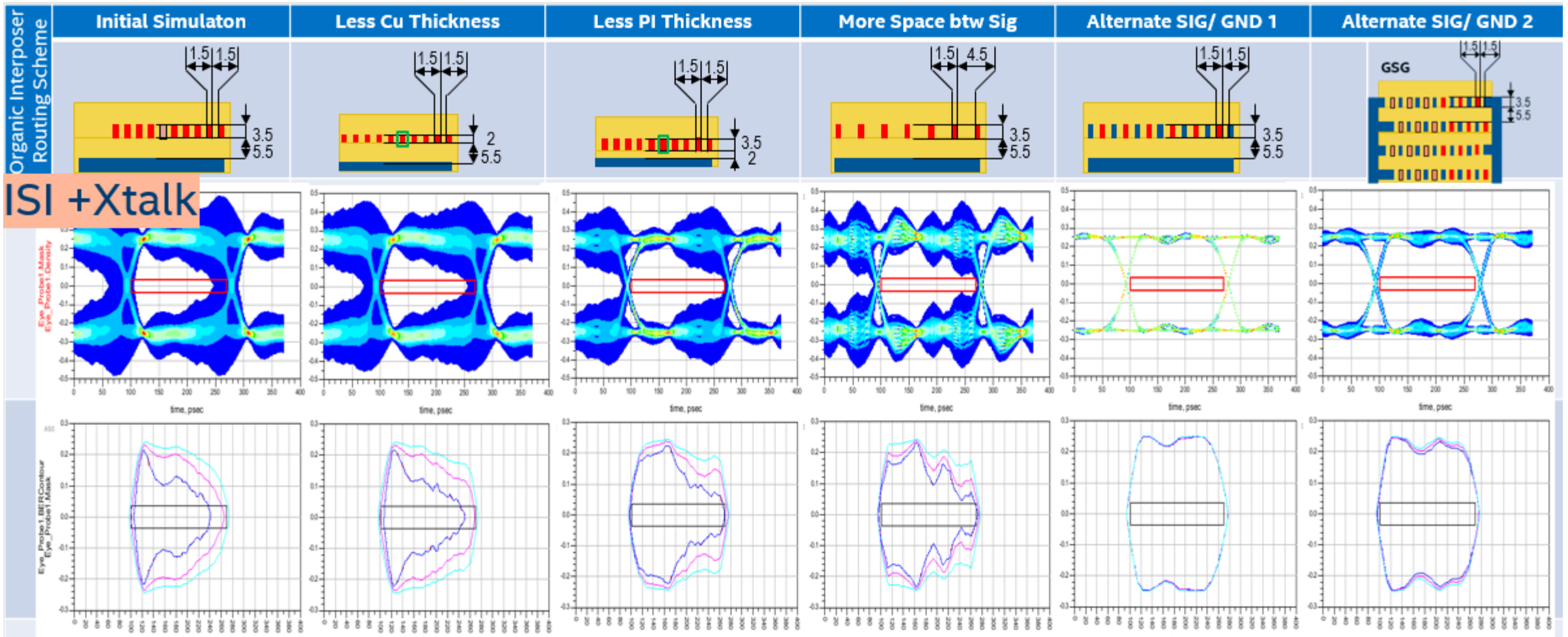
Single Ended Channel Simulation: Create Eye Diagram for ISI +Xtalk

Keysight ADS Test Bench Xtalk

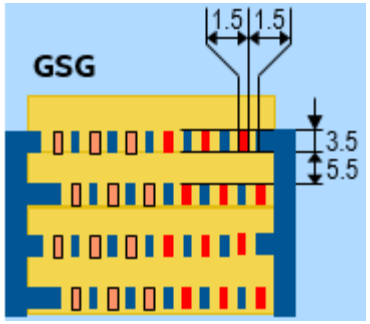


- Use same RC Loads on all Drivers (Tx and Xtalk).
- TX Drivers are unique on the schematic however there is no limit to the number of Xtalk components allowed.
- Xtalk drivers inherit their properties from the TX driver but many parameters may be overridden. In this case, Xtalk phase is 180 degrees to TX to produce a worst-case scenario.

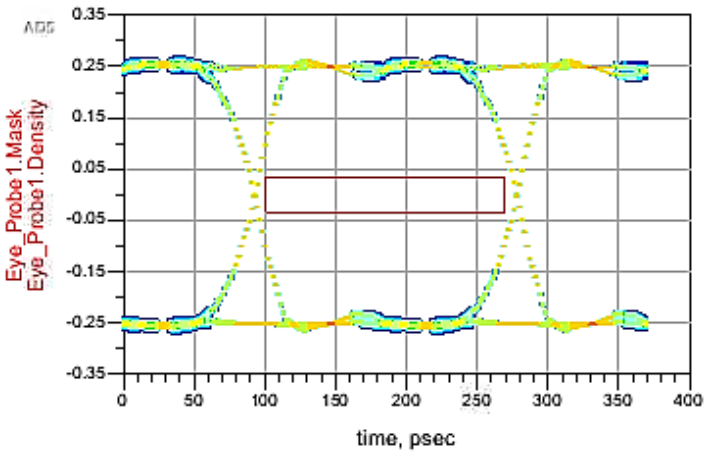
Results for Eye Diagram per Variation



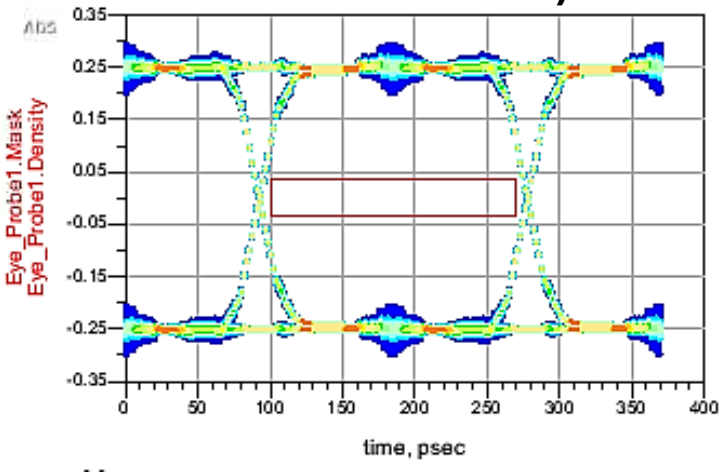
GSG Topology: Further investigation



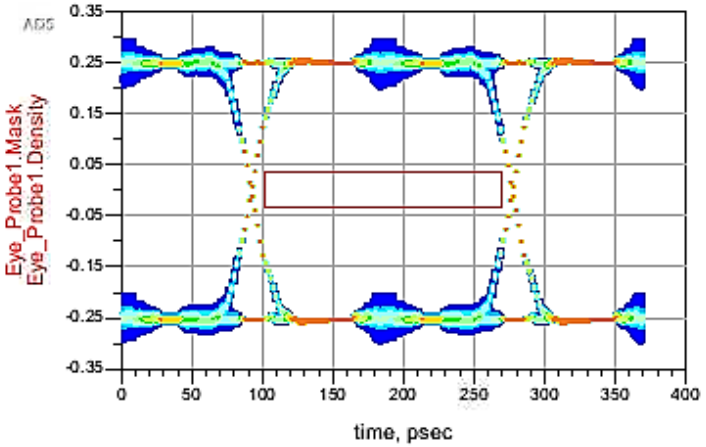
Eye Diagram: 12 Channels



Eye Diagram: 12 Channels Increased Freq Range from 10GHz to 20GHz (Adds Harmonic Content)



Eye Diagram: 20 Channels Increase Number of Channels in Simulation (Increases Xtalk)



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SUMMARY

- The investigations confirm the general feasibility of 2.3D interposer technology with advanced design rules for die-to-die interconnects.

- The high-density organic interposer extends the 2.xD passive interposer package portfolio with the advantage of cost reduction vs. 2.5D packages.
  - Higher bandwidth of the D2D interconnect could be achieved with a PHY co-designed for 2.3D design rules and future advances of the organic interposer capabilities.

- First competitor products on the market using 2.3D chip last technology are expected Q1'21 for networking application with several dies on the interposer.

- Several design topologies have been investigated.
  - The GSG topology is the desired choice for our study as it has very good electrical performance, passes SI requirements and meets the shoreline density.

Thank you!

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Bernd Waidhas: bernd.waidhas@intel.com