High Performance TIM for Lidded FCBGA Products

YoungDo Kweon I Sr. Director, Research and Development

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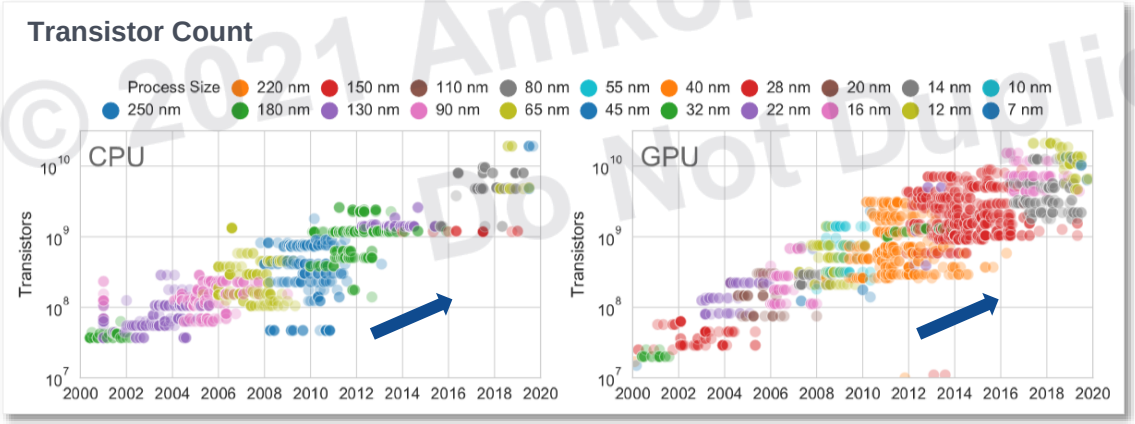
Agenda

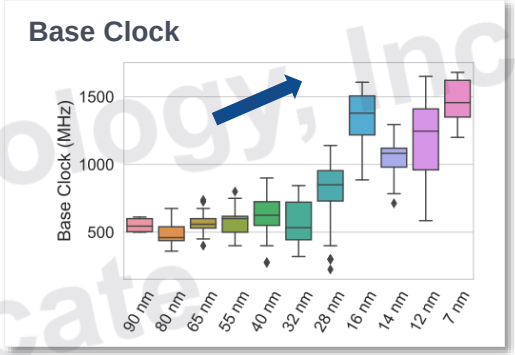
1. Technologies Trend
2. TIM (TIM I) for Lidded FCBGA Products
3. Summary

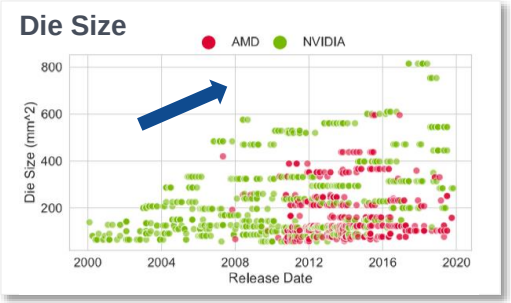
Technology Trends

Transistor Density

- Moore's Law is still valid for both CPUs and GPUs
  - Transistor density is continuously increasing
  - Base clock and die size are increasing steadily as well







Source: Summarizing CPU and GPU Design Trends with Product Data, Northeastern University

Power Density

- Power density is still increasing yearly
  - Logic static power trend is increased dramatically
  - Decreasing node size requires lower junction temperatures for reliability

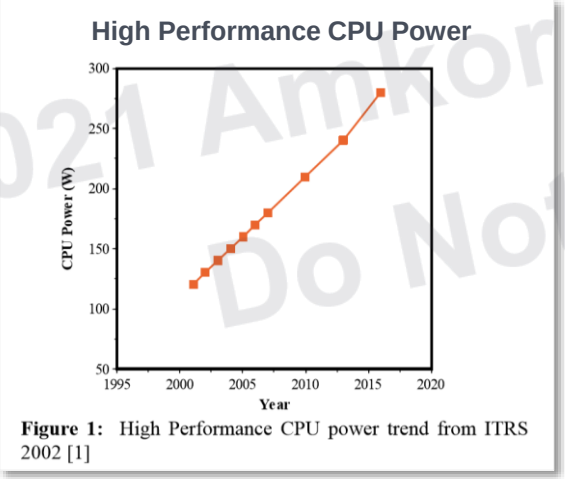
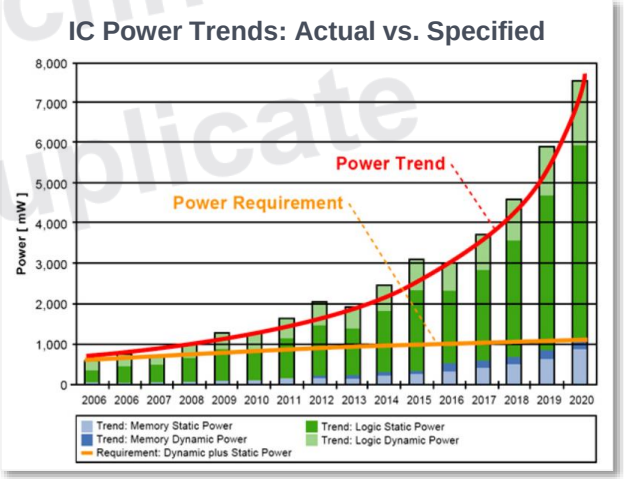


Figure 1: High Performance CPU power trend from ITRS 2002 [1]

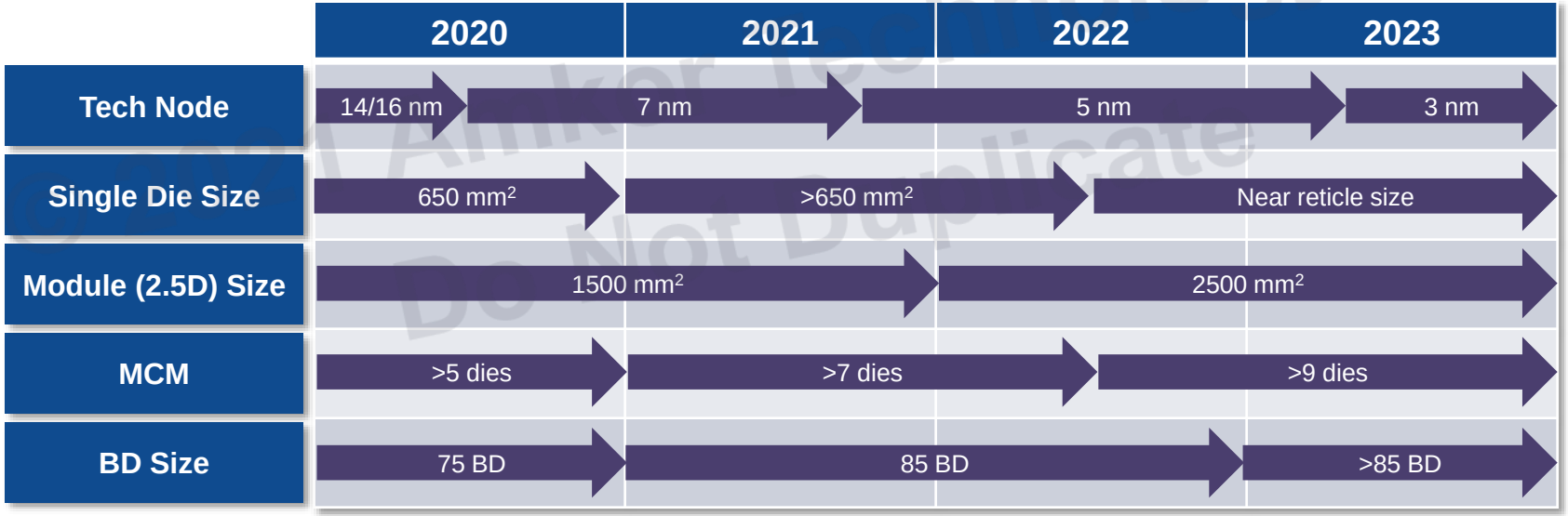
Source: ITRS



Source: ITRS

FCBGA Products Trends

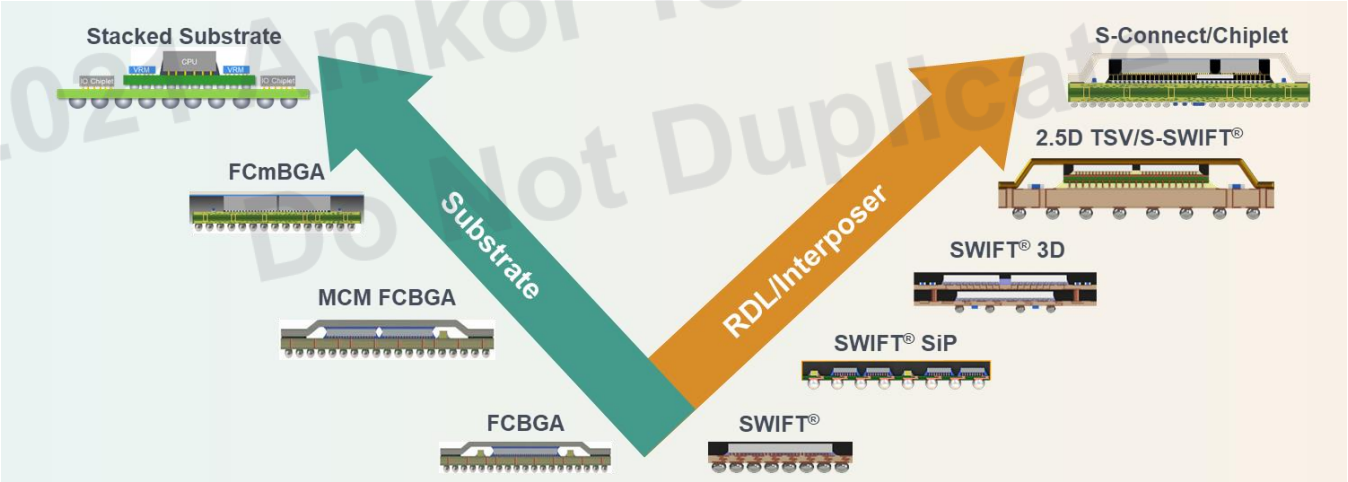
- More 2.5D and MCM products; need heterogeneous integration
  - Large BD and die (module) size increasing package thermal stress



Advanced FCBGA with Heterogeneous Integration

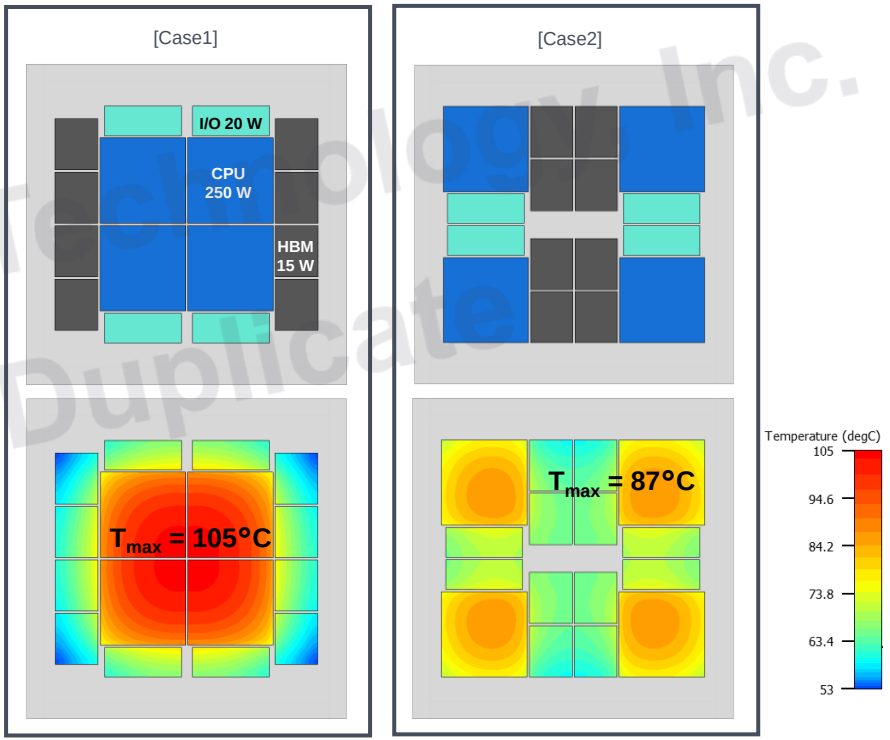
- Advanced FCBGA packaging is needed continuously
  - Challenges: An efficient thermal dissipation and a proper accelerated reliability test condition selection with considering the higher thermal stress

Heterogeneous Integration Path



Case Study: Thermal Dissipation for MCM Layout

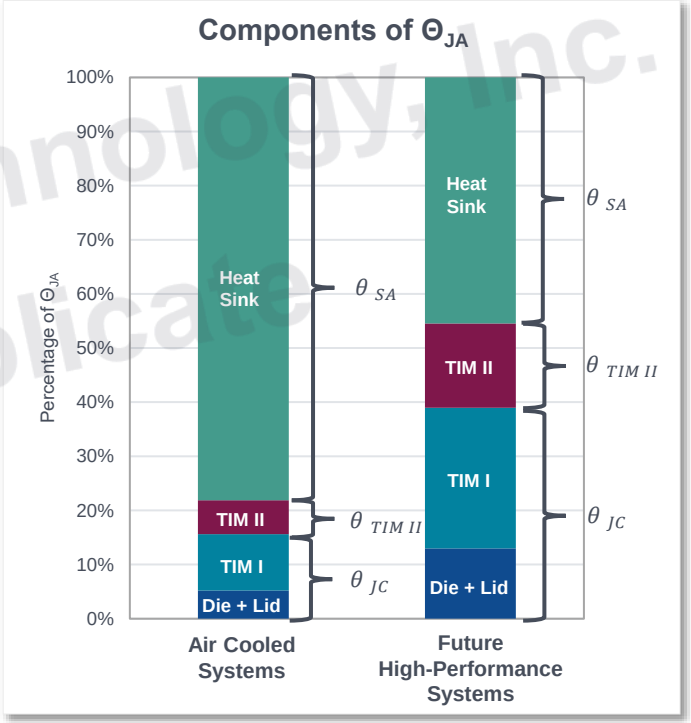
- Spacing between high power die can significantly impact temperatures
- High power die should still not be placed too near package corners



TIM (TIM I) for Lidded FCBGA Products

Thermal Packaging Challenges

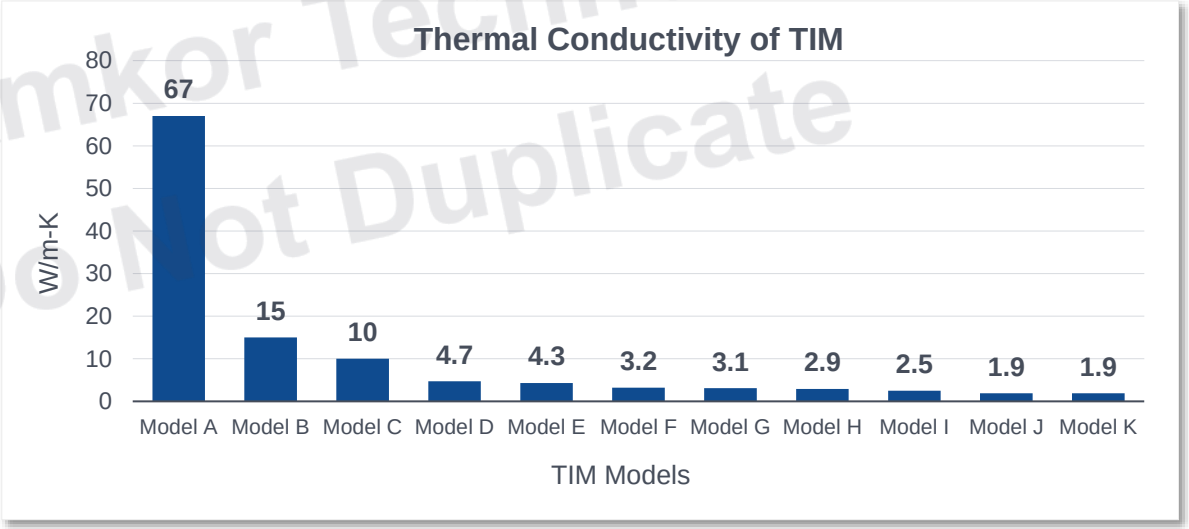
- Trends
  - Theta SA <0.05°C/W
  - Die power densities >0.5 W/mm2
- Innovations in cooling solutions resulting in Θ_{JC} becoming a significant component of total thermal resistance
  - Liquid cooling in data centers have ΘSA <0.04°C/W
- Decreasing node size requires lower junction temperatures for reliability, and a lower Θ_{JC} is needed critically
  - TIM I is an important portion for Θ_{JC}



TIM: Thermal Conductivity

- TIM thermal bulk conductivity value is provided by TIM suppliers, but thermal conductivity measurement is not carried out on the same metrology for all suppliers
  - ASTM D5470, transient hot wire method, laser flash method and so on

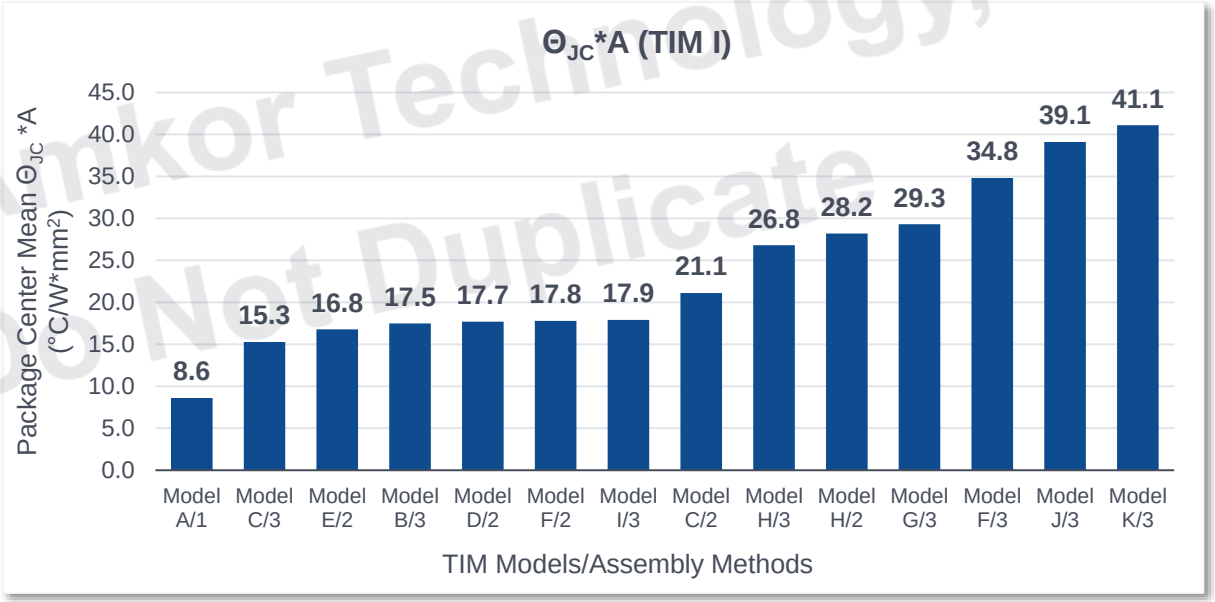
TIM	TC (W/m-K)
Model A	67
Model B	15
Model C	10
Model D	4.7
Model E	4.3
Model F	3.2
Model G	3.1
Model H	2.9
Model I	2.5
Model J	1.9
Model K	1.9



TIM: Theta JC (Θ_{JC}) Measurement

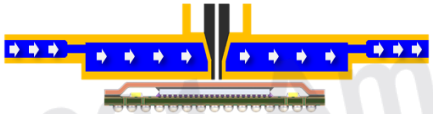
- Theta JC can not be derived from the TIM thermal bulk conductivity
- Interfacial thermal resistance value can be very significant and must be included

TIM Model/ Assembly #	Θ_{JC}*A (°C*mm^2/W)
Model A/1	8.6
Model C/3	15.3
Model E/2	16.8
Model B/3	17.5
Model D/2	17.7
Model F/2	17.8
Model I/3	17.9
Model C/2	21.1
Model H/3	26.8
Model H/2	28.2
Model G/3	29.3
Model F/3	34.8
Model J/3	39.1
Model K/3	41.1



Case Study: TIM Model F

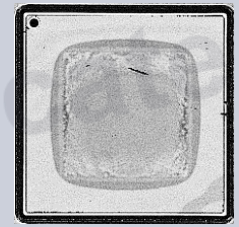
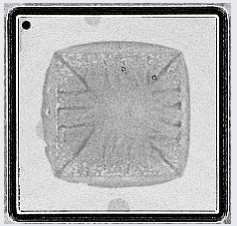
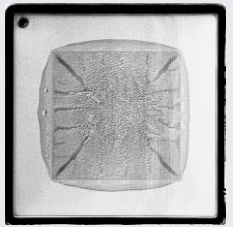
- TIM BLT and its quality are dependent on assembly methods
- TIM BLT quality is changed on board (SAT image result)



$$R_{TIM1} = \frac{BLT}{k * A} + R_{Contact}$$

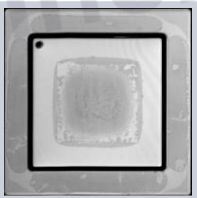
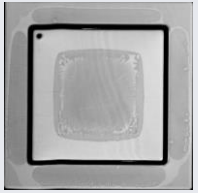
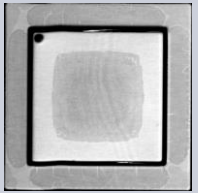
k : TIM1 bulk thermal conductivity
A : Die area

- TTV: 60 BD (25.6 x 25.6 mm^2 die)
- Cooling method: Cold plate with water (20°C)
- Center Θ_{JC} results

60 BD TTV	Package	On Board
Model F/2 Sample #4 BLT: 21.4 µm 19.46°C * mm^2/W		
Model F/3 Sample #2 BLT: 31.5 µm 30.17°C * mm^2/W		

Case Study: TIM Model D

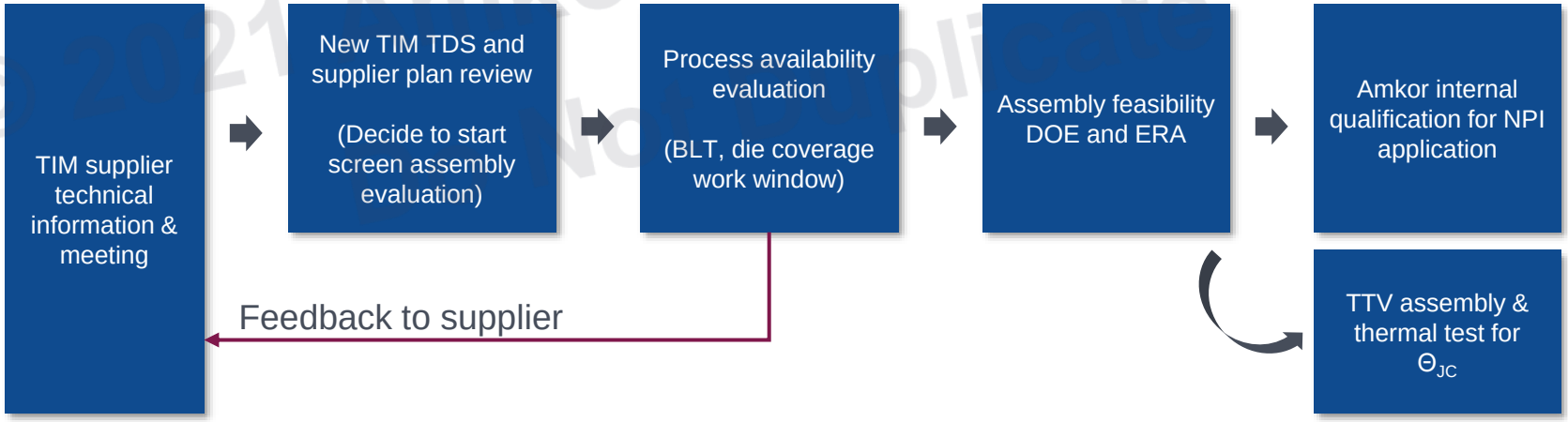
- TIM BLT and quality are dependent on assembly condition
- A thicker TIM BLT shows a lower void ratio

60 BD TTV	BLT (Mean)	Void Ratio	
Model D	19 µm	12%	
	37 µm	7%	
	45 µm	1.5%	

Summary

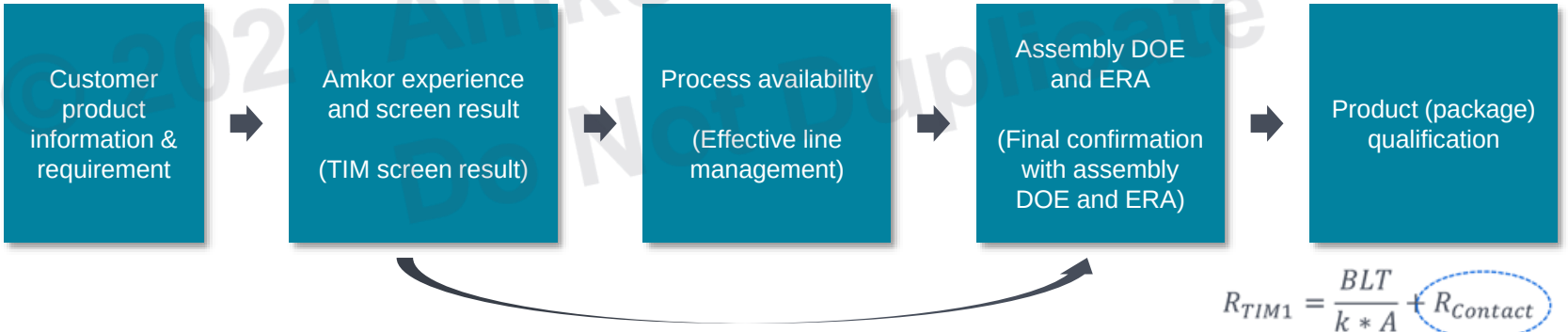
New TIM Screen Flow in Amkor

- Assembly quality is critical to confirm new TIM because TIM I thermal contact resistance value is dependent on its assembly quality
- The thermal Theta JC measurement is needed to know the real thermal performance in the package as TIM I



TIM I Selection Flow for Customer Product

- TIM thermal conductivity (*k* value) is an indicator-only of expected thermal performance
- However, the actual thermal performance as TIM I includes thermal interfaces as well
- TIM I thermal resistance of package (Theta JC: Θ_{JC}) measurements in a well controlled lab are essential



Summary

- Transistor and IC power densities are still increasing yearly
- Decreasing node size requires lower junction temperatures for reliability, and a lower Θ_{JC} is important
- TIM (TIM I) is an important factor for reducing Θ_{JC}
- TIM thermal conductivity is an indicator-only of expected TIM I thermal performance of package
- Amkor has the capability to provide actual thermal performance using thermal test die and realistic package assembly
- Amkor continually assesses the market for the best TIMs available as well as assembly know-how to complement them

Thank You

amkor.com