Design of a Subsystem Module Package for Power Distribution Network

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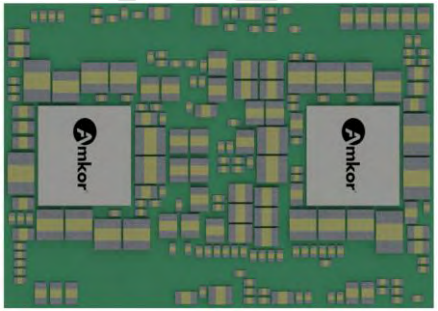
Agenda

1. Introduction of Subsystem Module
2. Comparison Between DSCP and Subsystem Module
3. DC IR Drop Analysis
4. Impedance Analysis with Decap Combination
5. Discussion

Why Subsystem Module Package?

- Enabled by
  - Small form factor – miniaturization
  - PDN improvement – power consumption
  - Low cost – business
- Drive for higher level of performance and efficiency
- Subsystem module is not always the best, but it is better when we design effectively

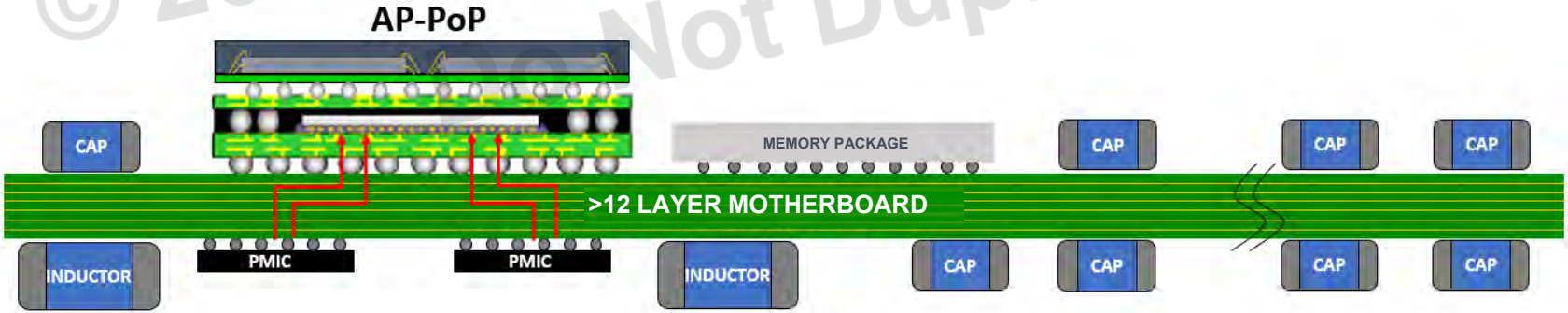


Objective

- DCIR drop and AC analysis in frequency domain
  - The subsystem module design for PDN
  - Double-sided component placement (DSCP) motherboards vs. subsystem module package
  - Three terminal decap configurations for optimum performance with cost effective model
    - Capacitor size
    - Capacitor count
    - Capacitor value

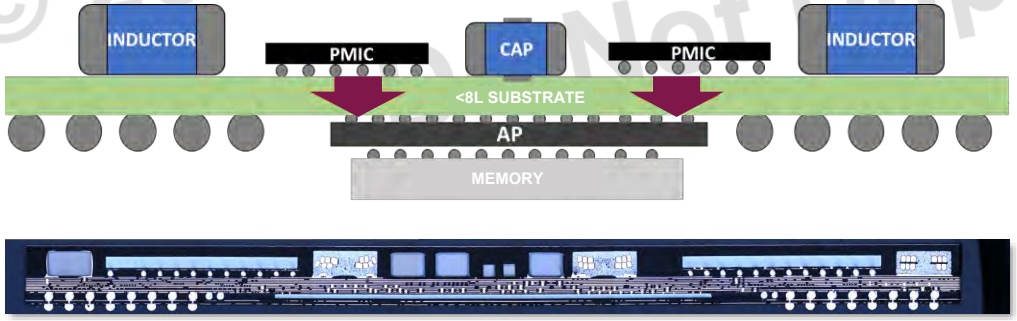
Double-Sided Component Placement (DSCP) Motherboard in Mobile

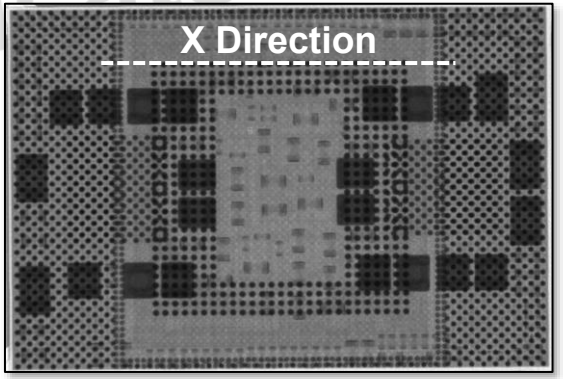
- >12 Layer motherboards
- AP-PoP and memory and Flash memory on top
- PMICs and inductors on bottom
- Caps are both top and bottom

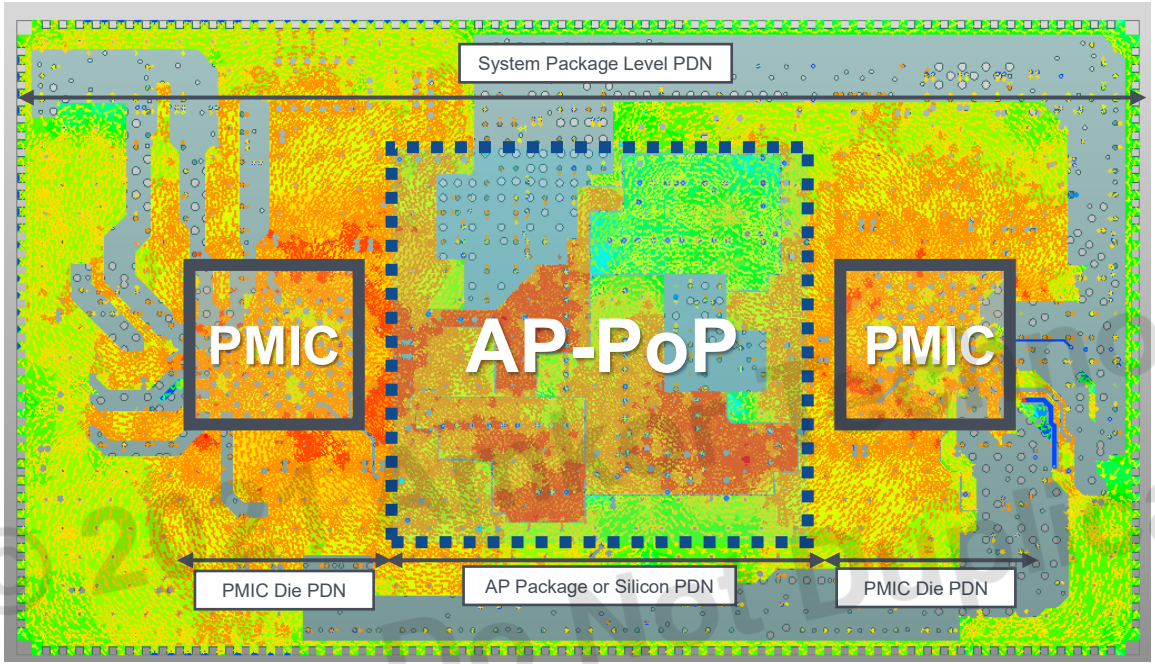


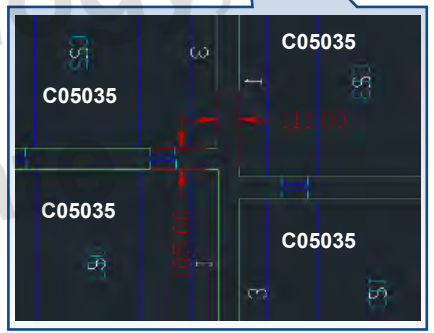
Subsystem Module

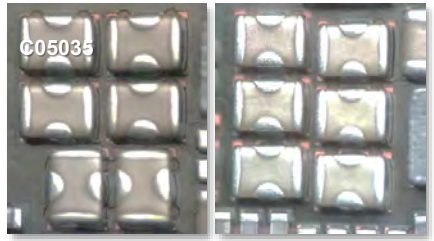
- Much smaller than motherboard design
- <8 Layer laminate substrate → low mounted inductance
- PMICs, capacitor and inductors on top → low speeding inductance
- AP-Chip and memory on BTM

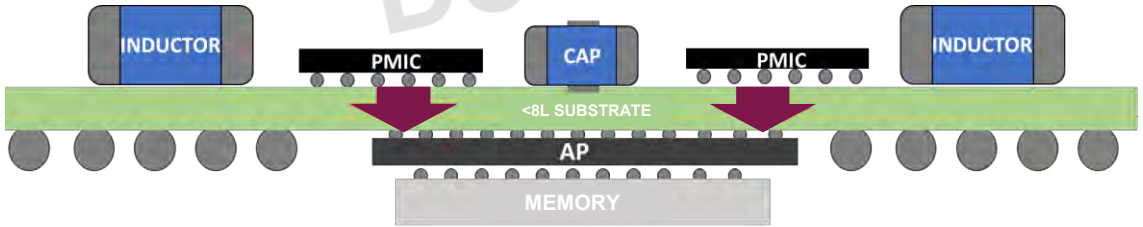


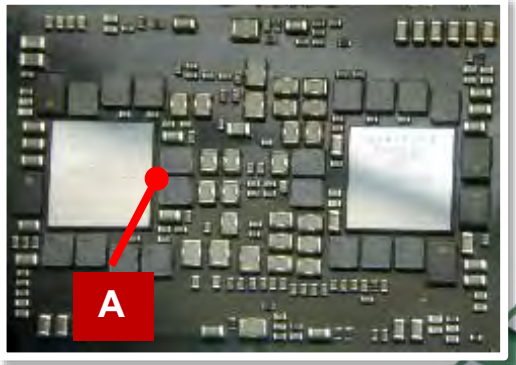




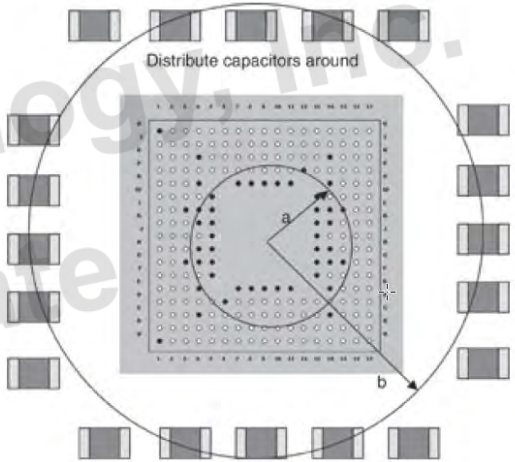








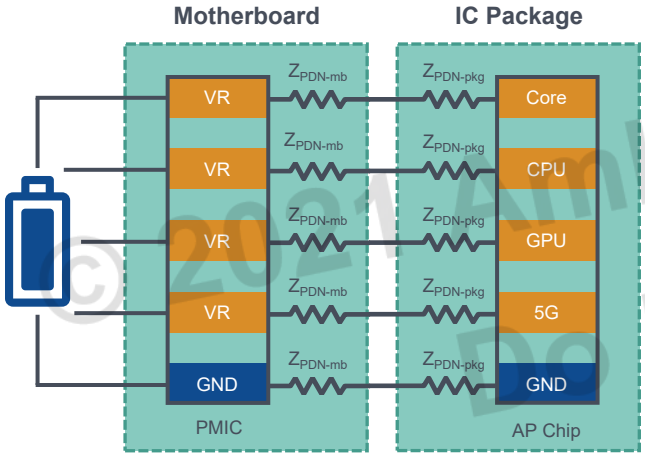
Spreading Inductance



$$L_{Spread} = \frac{\mu_0}{2\pi} \times h \times \ln\left(\frac{b}{a}\right)$$

Double-Sided Component Placement (DSCP) Motherboard

Schematic diagram

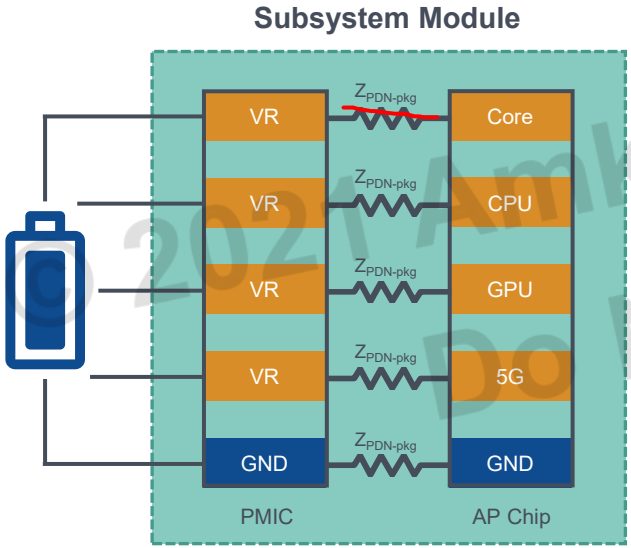


$$Z_{PDN\_MB} = \left\{(R + j\omega L + j\frac{1}{\omega C})_{MB} + (R + j\omega L + j\frac{1}{\omega C})_{PKG}\right\} // Z_{VR}$$

$$V_{PDN} = Z_{PDN\_MB} \cdot I_{MAX}$$

Subsystem Module

Schematic diagram

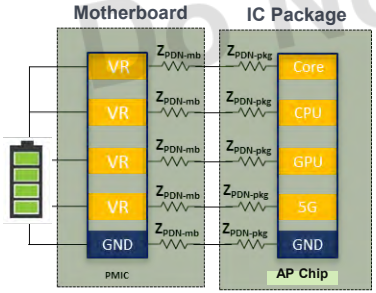


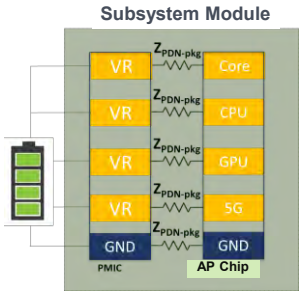
$$Z_{PDN\_MD} = (R + j\omega L + j\frac{1}{\omega C})_{PKG} // Z_{VR}$$

$$V_{PDN} = Z_{PDN\_MD} \cdot I_{MAX}$$

Comparison of DC IR Drop

	Motherboards + Package Model (mV)					Subsystem Module Model (mV)		
	Package			Motherboard	Total			
Power	ΔVp_pkg	ΔVg_pkg	ΔVpkg(ΔVg+ΔVp)	ΔVmb	ΔV(ΔVpkg+ΔVmb)	ΔVp_pkg	ΔVg_pkg	ΔV(ΔVg+ΔVp)
CPU Core	3.253	3.043	6.295	7.500	13.795	2.821	1.400	4.221
CPU 1	0.065	3.043	3.108	15.000	18.108	3.999	1.798	5.797
CPU 2	0.997	3.043	4.039	15.000	19.039	11.160	1.798	12.958
Modem	0.657	3.043	3.700	15.000	18.700	6.216	1.400	7.616
GPU	0.121	3.043	3.164	5.020	8.184	4.495	1.798	6.293
Memory	2.808	3.043	5.851	8.300	14.151	11.132	1.798	12.930

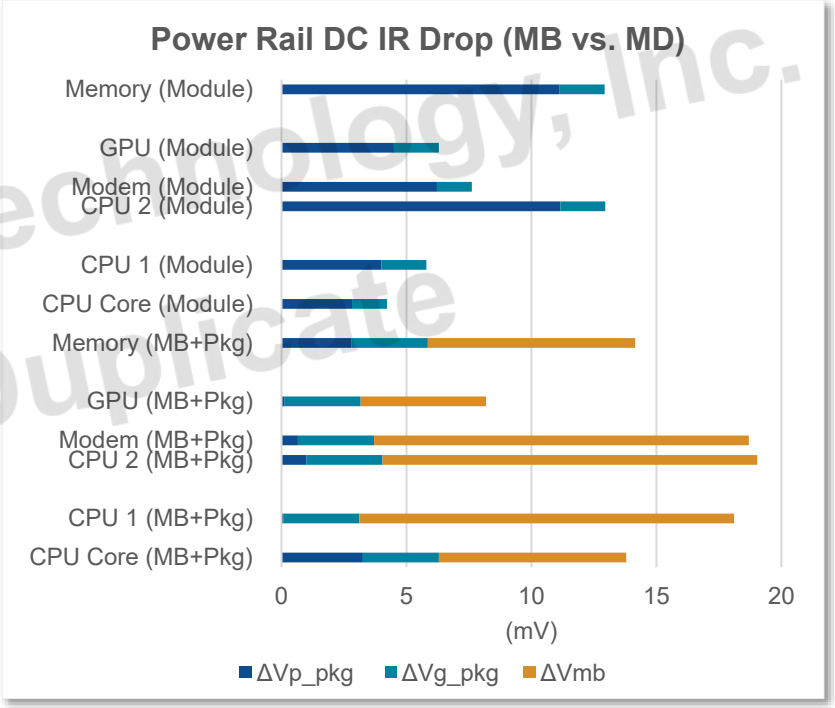




Comparison of DC IR Drop

- DSCP (motherboard + package) model
  - Power rail: IR drop ▲▲
  - Ground: IR drop ▼
  - Total IR drop ▲
- Subsystem module
  - Power rail: IR drop ▲
  - Ground: IR drop ▼▼
  - Total IR drop ▼

▲: High
▼: Low



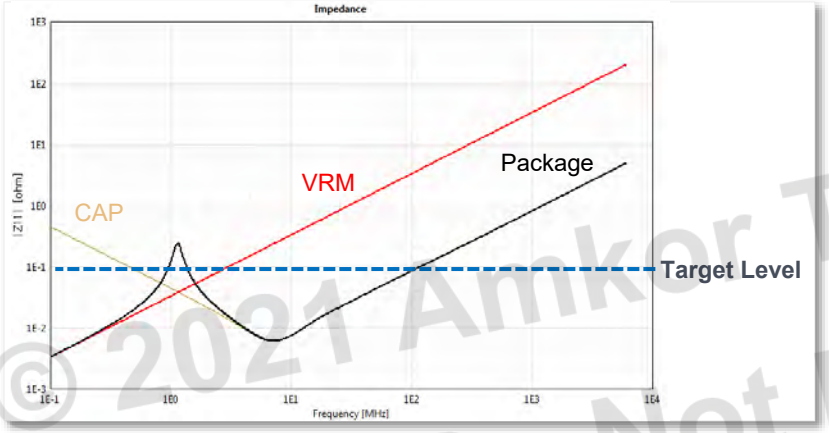
Using Controlled ESR Caps to Reduce Peak Impedance Heights

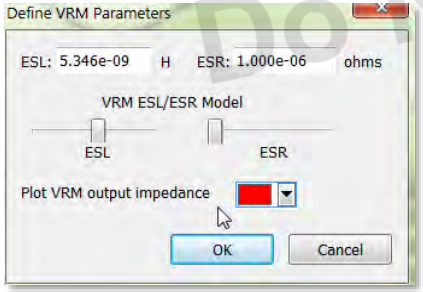
- The Q factor of the cavity resonance dramatically reduces, and the peak impedance dramatically lowers if capacitor ESR maintain higher. The peak impedance at the parallel resonance of capacitors' ELS and the cavity's capacitance is:

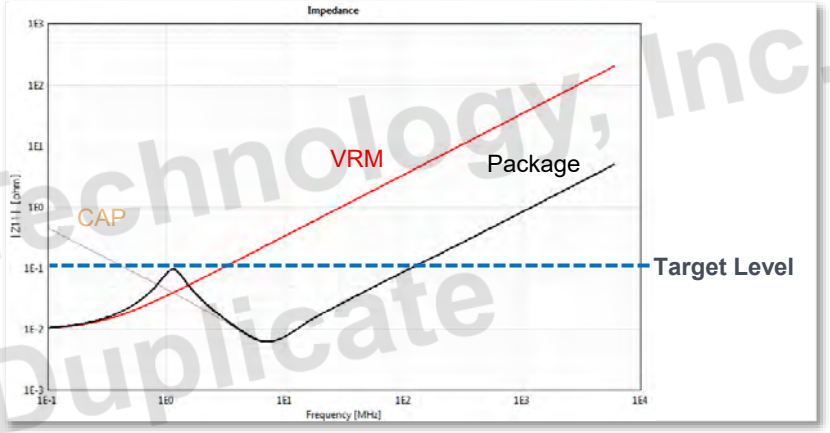
$$Z_{peak} = q - factor \times Z_0 = \frac{n}{ESR} \cdot \frac{\left(\frac{1}{n}\left(ESL_{CAP} + L_{spread}\right)\right)}{C_{cavity}}$$

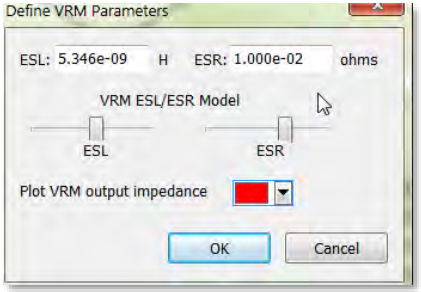
(Principles of Power Integrity, Eric Bogatain)

ESR(Equivalent Series Resistance) vs. Peak Impedance of System

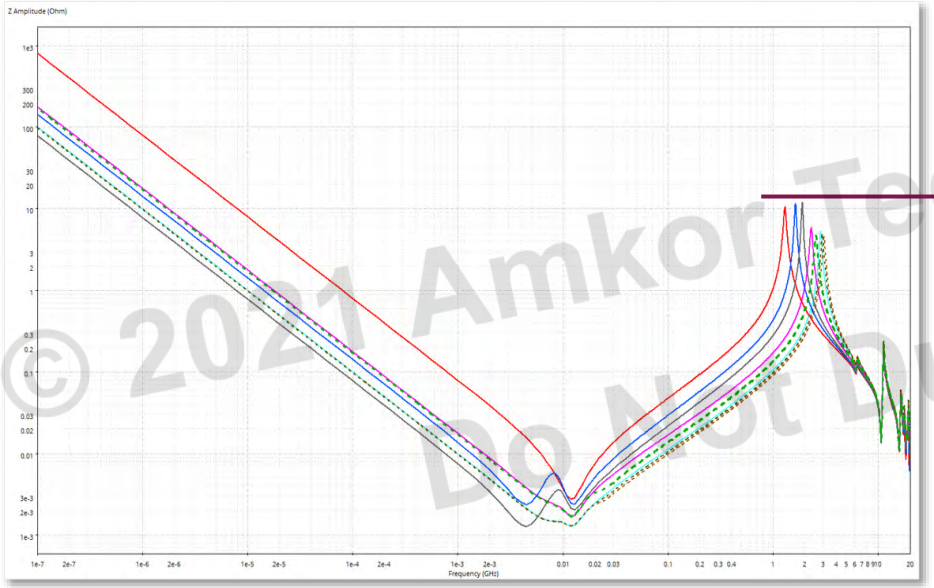








Decap Configuration in Subsystem Module

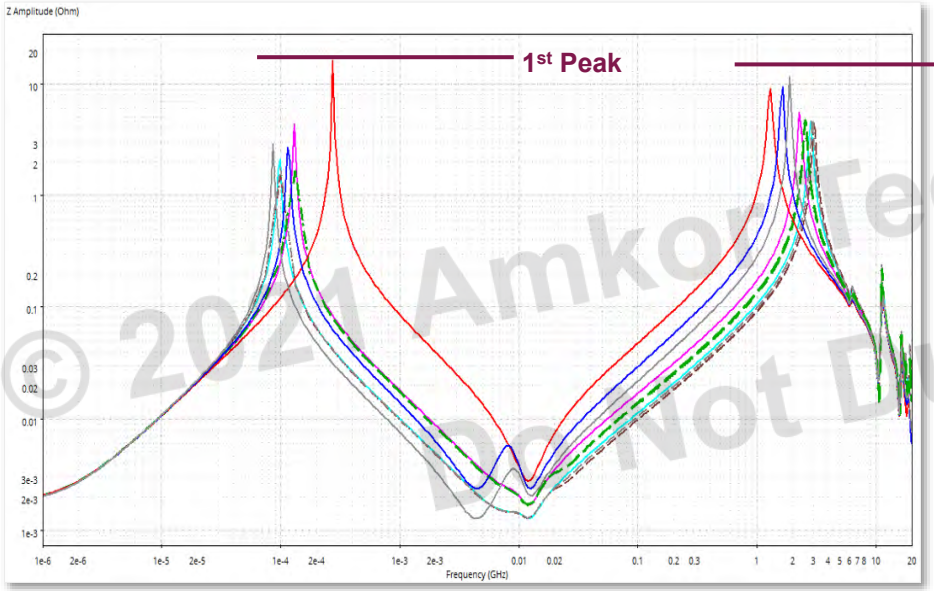


Peak

Legend	LEG	Capacitance combination (uF, Size, Count)				Z_{PDN}		Density (%)	Cost Factor
		Chip	Sub system module			10MHz	100Mhz		
		0.22uF	1.0uF	4.3uF	15uF				
		0201	0201	0402	05035				
	1	0	2	0	0	4.15E-03	4.44E-02	-	-
	2	0	2	0	2	4.03E-03	2.80E-02	216%	559%
	3	0	2	0	4	3.29E-03	2.08E-02	432%	1118%
	4	0	2	4	0	1.43E-03	1.07E-02	200%	200%
	5	0	2	2	0	2.13E-03	1.63E-02	100%	100%
	6	2	2	4	0	3.27E-03	1.93E-03	236%	217%
	7	1	2	4	0	3.25E-03	1.93E-03	218%	208%
	8	2	2	2	0	3.81E-03	1.91E-03	136%	117%

Impedance profile with bulk capacitors for variants

Decap Configuration in Subsystem Module



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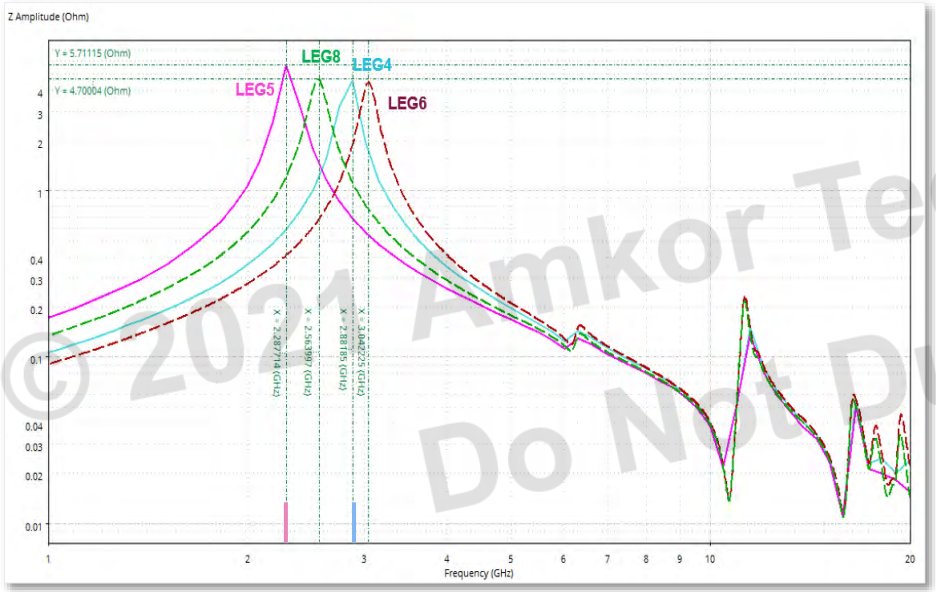
Impedance profile with VRM and bulk capacitors for variants

Decap Configuration in Subsystem Module



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		Chip	Sub system module			10MHz	100Mhz		
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		0201	0201	0402	05035				
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Discussion

- Subsystem module enables
  - Smaller micro vias, thinner dielectric, tight component placement
  - Lower mounting inductance and spreading inductance
- Improved the DC IR drop
- Low ESR
- Finding the optimized combination of decaps

Conclusion

- Subsystem modules reviewed
  - Power integrity performance improvement with the optimum design
  - Capacitor combinations
  - Lower peak impedance, low cost and small form factor

Thank you

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