Chip Scale Power Transistor Packaging

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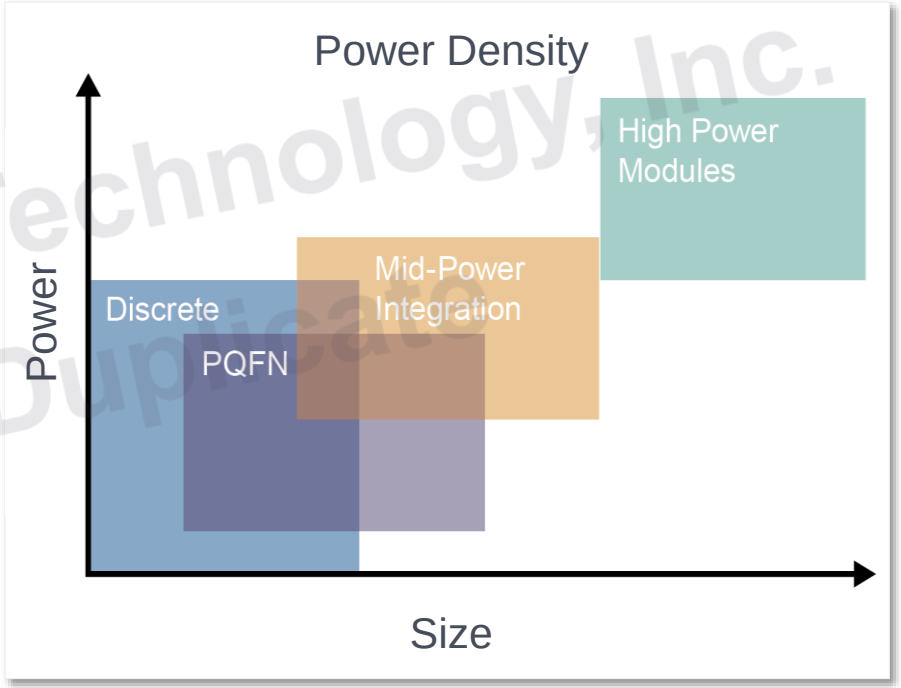
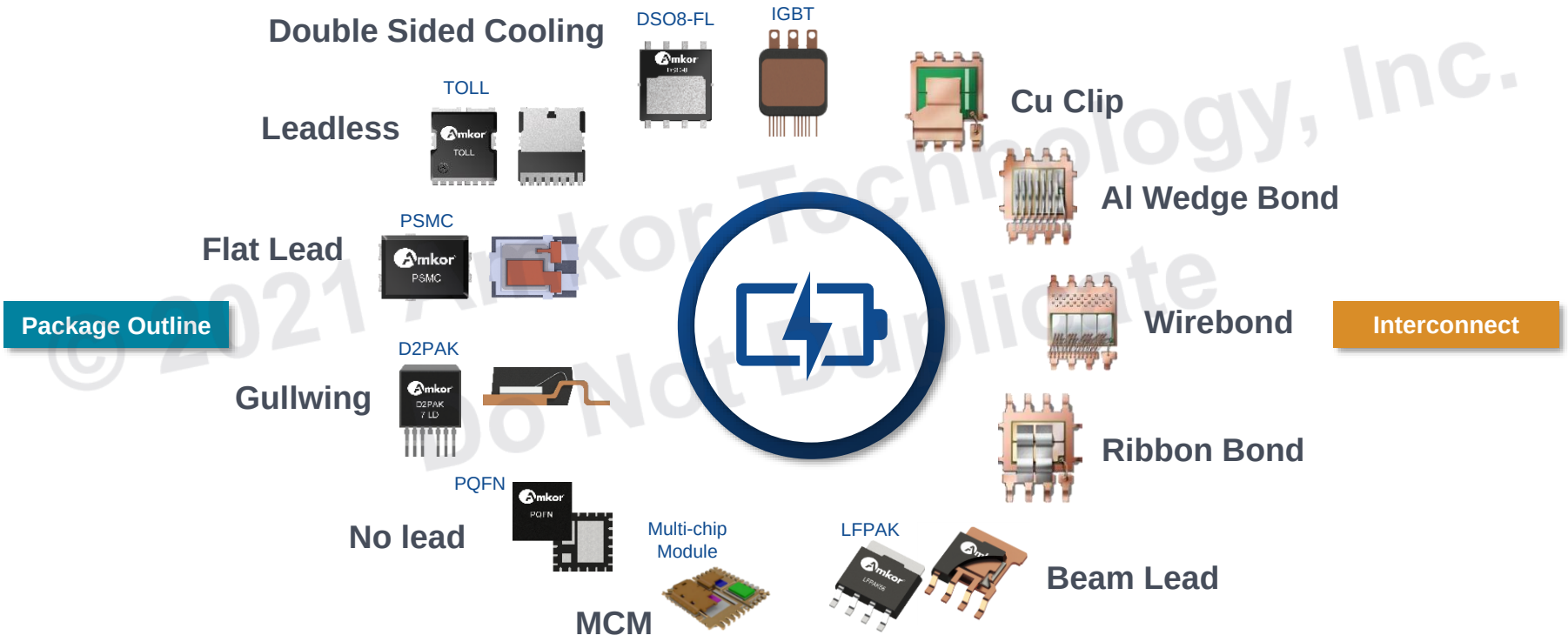
Package Positioning in Power Semi

- Vectors for discrete and integrated power
  - Low resistance/inductance
  - Dual-sided cooling
  - Reduced form factor
  - Add controller/logic/passive
- Gaps
  - High density packaging
  - Universal formats for discrete and integrated use



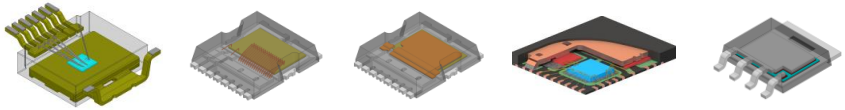
Amkor Power Package Solutions



The need for high density packaging

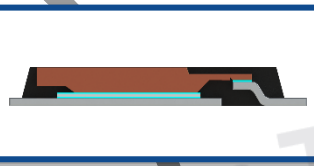
- Performance based on mass and area disruptive to system goals
- SiC and GaN are pushing package density requirements
  - Reduced die size
  - Higher op temps
  - Low-loss packaging
- If form factor reduces, then density must increase

Pkg Type	Pkg Size (mm)			mm²	
	x	y	h	Area	Total Copper Volume %
eD2PAK	14	11.7	3.6	163.8	28.96%
D2PAK	10	10.5	4.45	105	23.24%
TOLL Wire	9.9	10.4	2.3	102.96	17.23%
TOLL Clip	9.9	10.4	2.3	102.96	20.10%
PQFN	5	6	0.83	30	13.65%
LFPAK-BL	4.9	4	1.05	19.6	32.07%



Maximum Power Density Solutions

High Performance



Dual-Sided Discrete Packages

Low Resistance
Low Inductance

Ultra Heavy Cu Wire

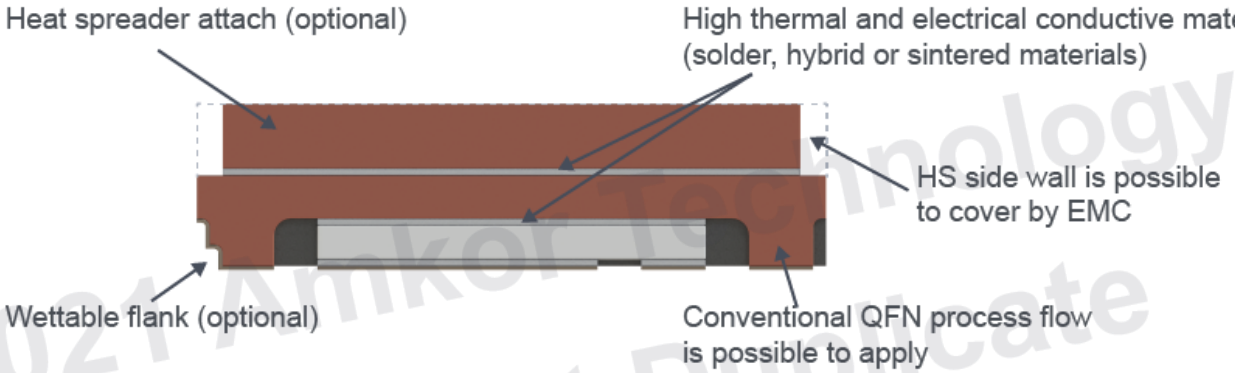
High Thermal Conductivity

Sintering Die Attach Paste

PowerCSP™ Technology Introduction

- Simplified architecture for MOSFET devices
- Source and gate directly bonded to PCB
- Maximum conductivity between source and drain
- Conductive material increase to 30-70% range

PowerCSP™ Technology Flexibility



- Simplified process steps and removal of interfaces
- Scalable to application or to emulate common sizes
- Adaptable to discrete or modular designs

PowerCSP™ Technology Packaging Variations

- Many configurations for chip scale power
  - Integrated heatsink or thick leadframe
  - Exposed and overmolded options
  - Single or multiple sided terminals
  - Routable leadframe for internal gate

Covered back drain

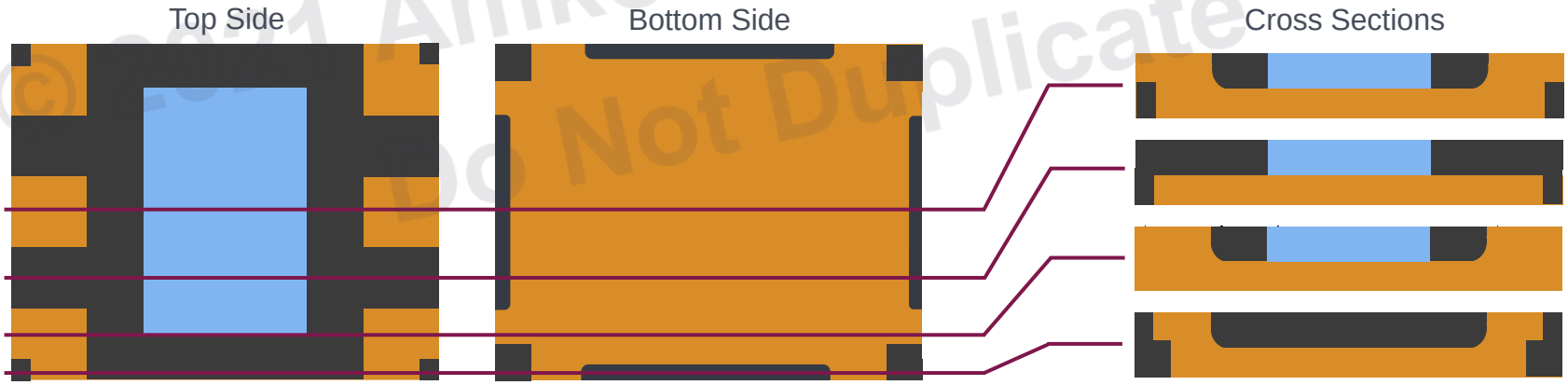
Exposed back drain

Gate on PCB

Internal Gate

Power CSP™ Technology

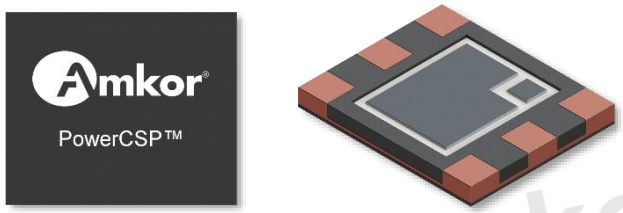
- “QFN” outline from etched substrate
- Attached to PCB using SMT
- Optional additional HS mounting

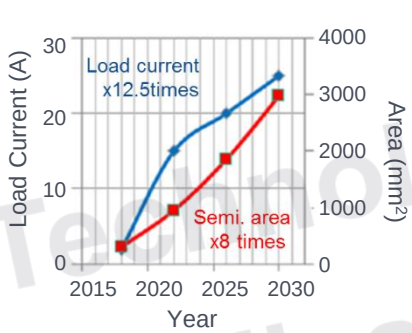


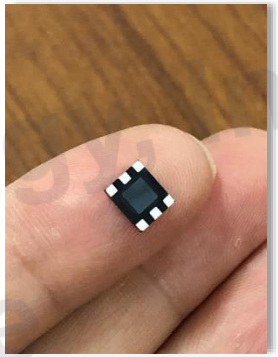
Power CSP™ Technology Process Flow

- Die attach
- Molding
- Exposing bottom Cu pad
- HS attach (optional)
- Surface finish (tin plating)
- Singulation (wettable frank)

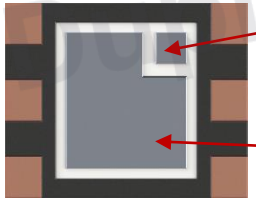
Power Density and Form Factor Shifts

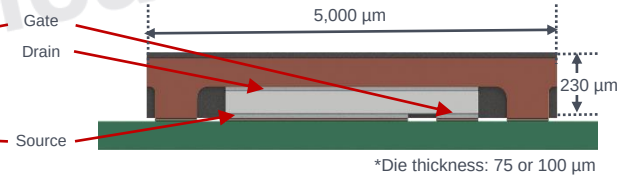


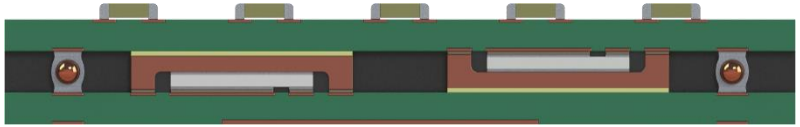




- PowerCSP™
  - Smaller form factor
  - Low R_{DS}(on)
  - Leads to embedded options

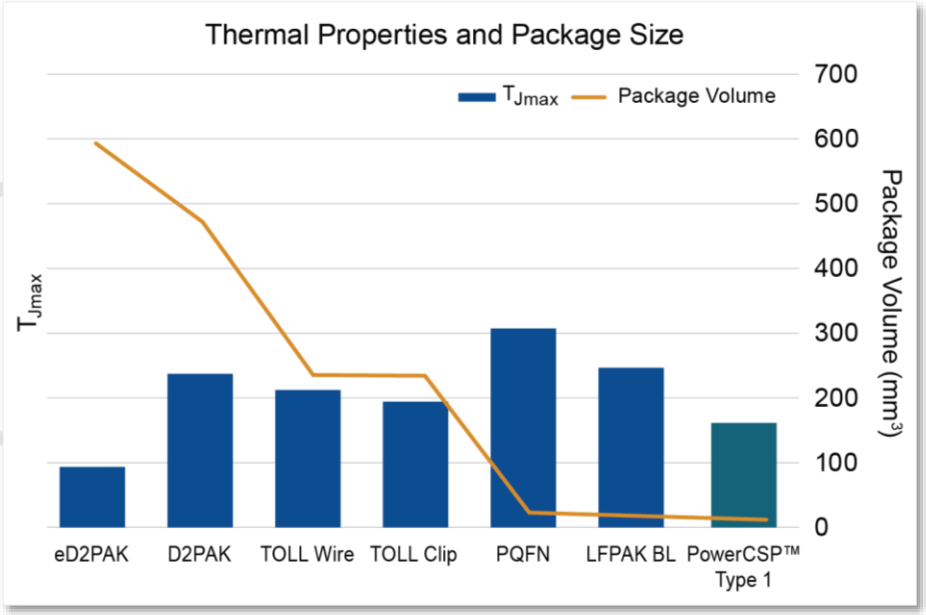






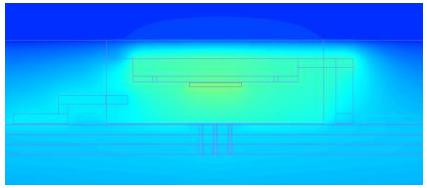
PowerCSP™ Thermal comparison

- Conductive material density leads to performance advantage in small volume packages
- Large volume packages have advantage in X-Y thermal spreading
- High heatsink and TIM influence

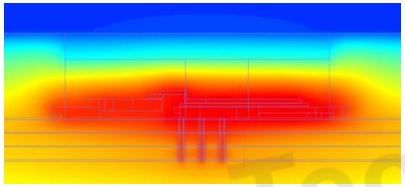


Temperature Profile Results (10W, With Heatsink)

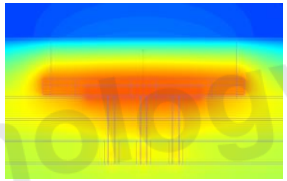
eD2PAK



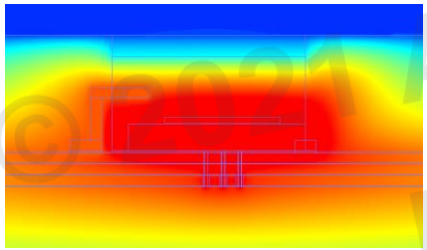
TOLL (Clip)



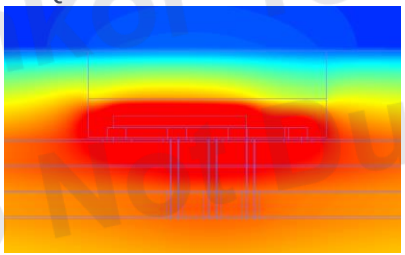
PowerCSP™



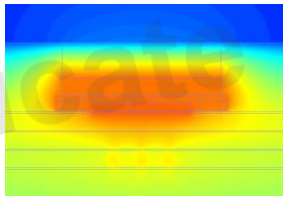
D2PAK

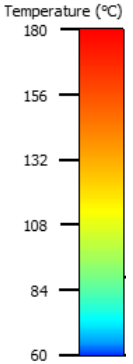


PQFN

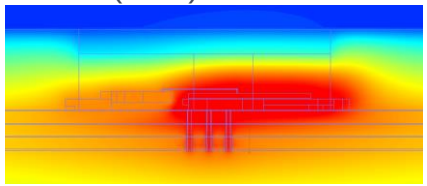


PowerCSP™ + HS

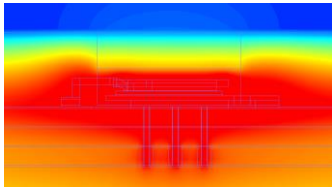




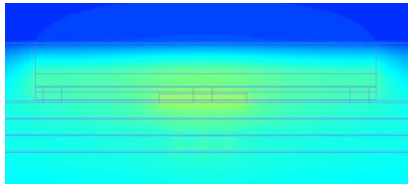
TOLL (Wire)



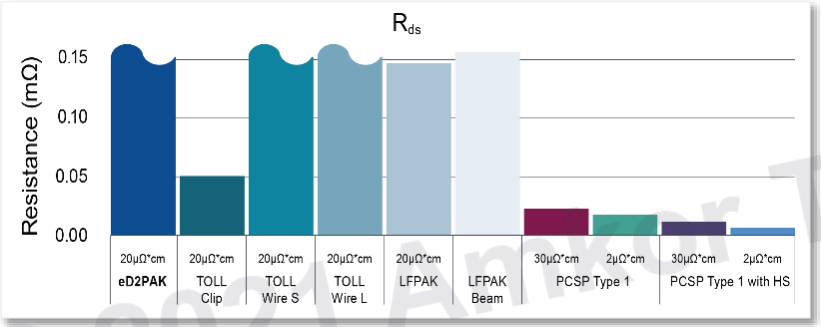
LFPAK

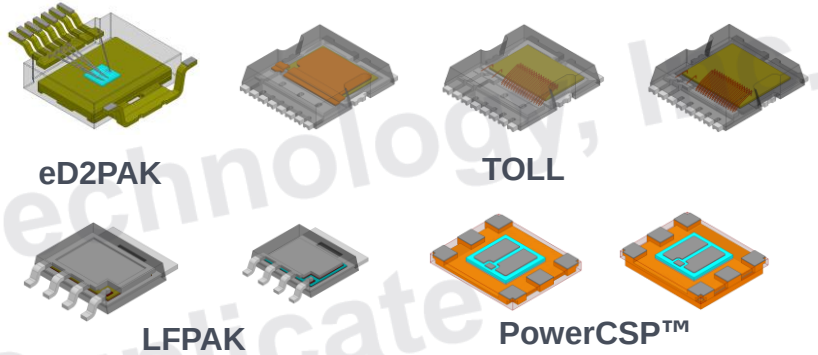


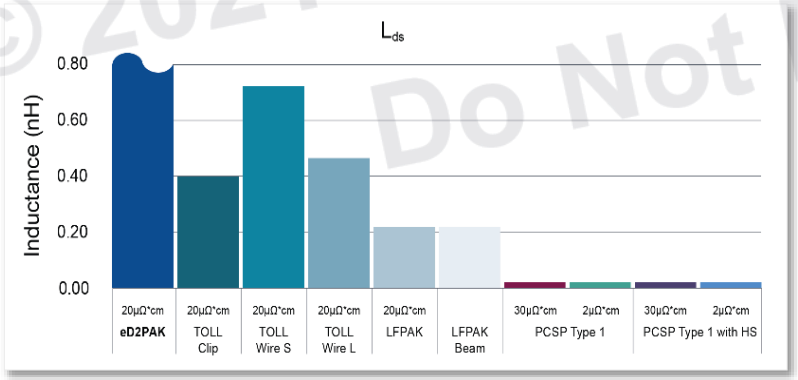
PowerCSP™, 11 x 11 + HS

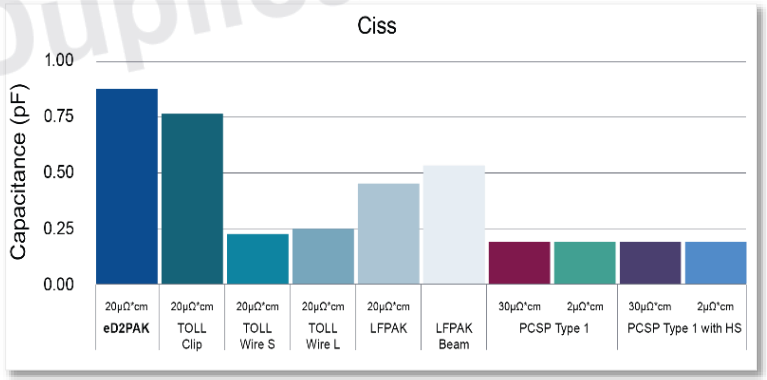


Electrical Simulation Result (LCR)



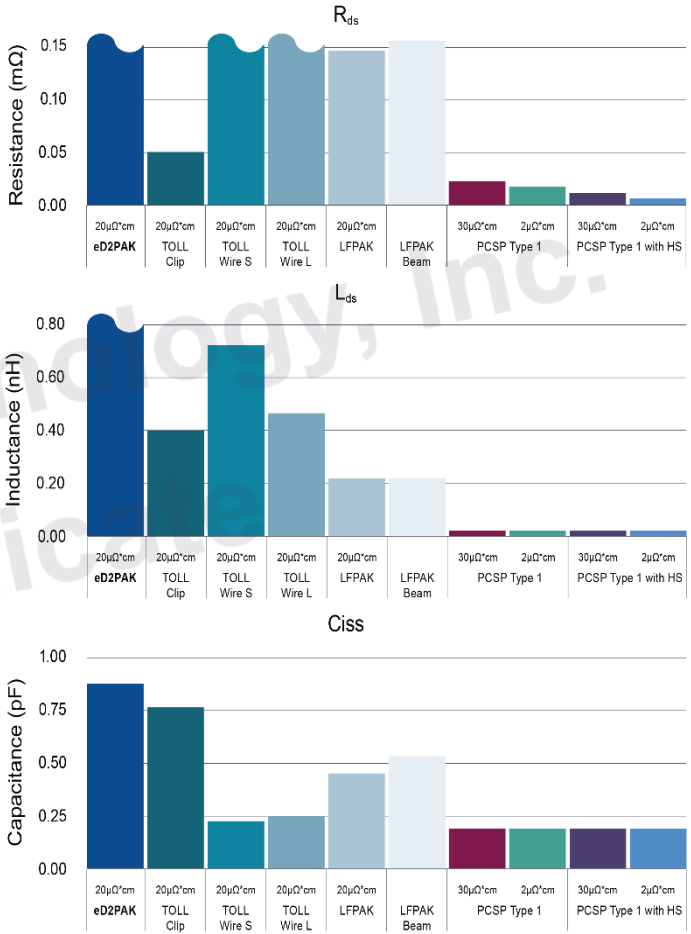






PowerCSP™ Technology Electrical Comparison

- Lowest resistance package of characterization group
- Significantly lower inductance than any other package
- Slightly lower capacitance than devices in characterization group
- Values consistent with both high and low conductivity die attach material



Power Package Integration Paths

Low- to Mid-Power

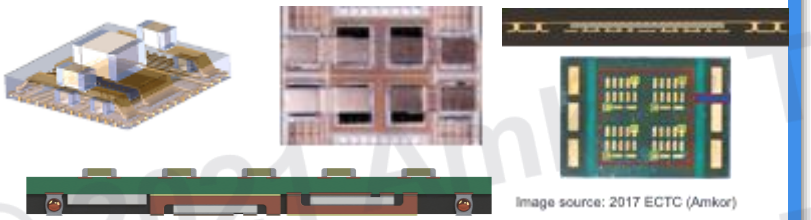


Image source: 2017 ECTC (Amkor)

High Power

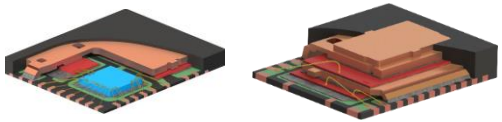
Image source: IEEE Xplore

Divergent Paths

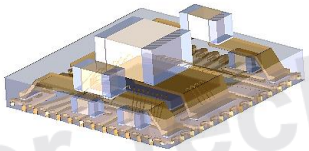
- PQFN derivatives
- Embedded
- Dual-sided module

- Large body (~50 mm++)
- Overmolded leadframe (dual sided)
- Specialized thermal substrates

Evolution of PQFN/PMIC Integration



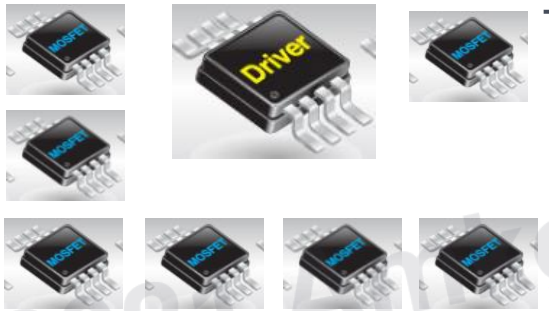
- Multi die
- Clip and wire capable
- Stacked MOSFET or side by side
- Cu to Cu process



- Integrated inductor and passives for electrical efficiency
- Uses exposed Cu from clip

- Reduce inductor electrical path
- Form factor reduction
- Auto/Mobile/Network markets

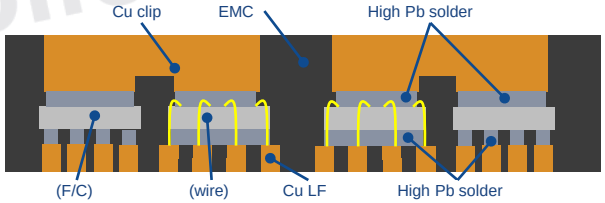
Large Form Factor PQFN



Multiple Power and Driver Devices Into One Package

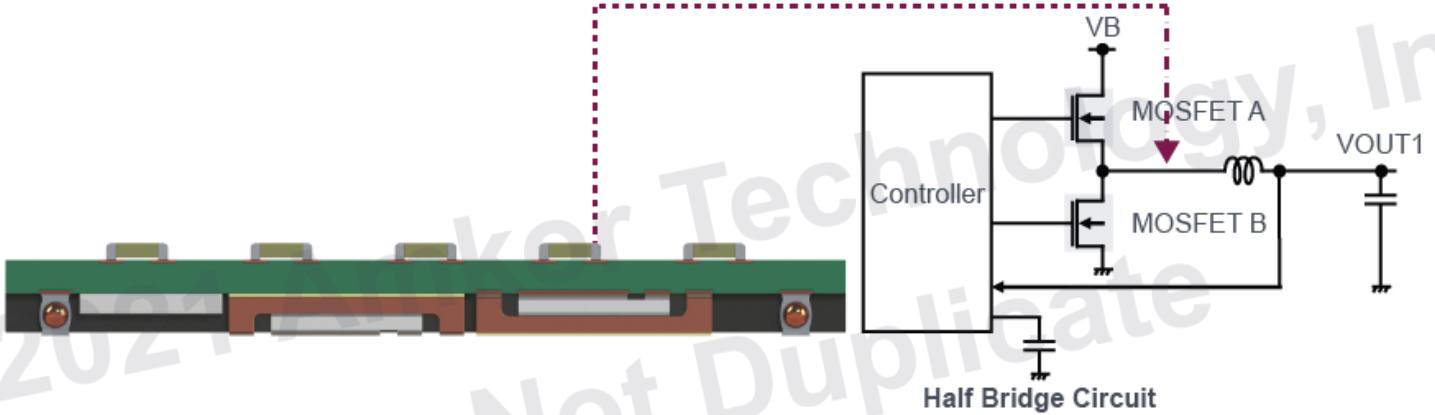
Body size:16.3 x 16.3 x 1.05 mm

- Increased size PQFN (~3x)
- Exposed pads for passive integration
- Thicker Cu substrate
- Cu Clip + wire or flip chip
- Many die attach steps



Large Form Factor Package Structure

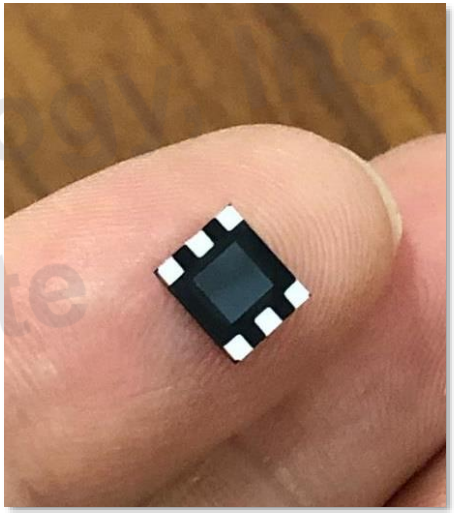
Power Module Using PowerCSP™ Technology

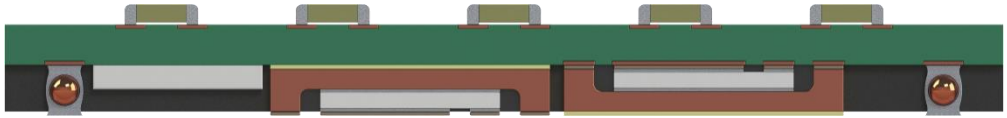


- PowerCSP™ technology as KGD
- PowerCSP™ allows thick Cu only where you need it
- Line inductance minimization between MOSFET and passive comp.

Summary

- Packaging innovation needed to match increasing power product demands
  - Low resistance/low inductance packaging
  - Reduced form factor and conductive density
  - Discrete and integrated application compatible
- PowerCSP™ architecture offers a scalable and flexible platform to meet a wide variety of power applications





For additional information on PowerCSP™, or other packaging needs, contact

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Thank You

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