Emerging Process and Assembly Challenges in Electronics Manufacturing

Glenn Farris – VP Marketing, Universal Instruments

Background

Glenn Farris has enjoyed more than 30 years in the electronics industry, starting as a research engineer at NASA and transitioning to leading marketing organizations for multiple technology companies. He is experienced in advanced simulation technology, semiconductor test and measurement, enterprise hardware and software platforms, and nanoscale MEMS applications, and dealing with clients in consumer, automotive, medical, networking industries.

Glenn has a broad vision of market trends and deep understanding of technology challenges. He joined Universal in 2013 as Vice President, Marketing and has been instrumental in leading the company into developing strategic relationship with some of the world's largest technology leaders.

Outline/Agenda

- Introduction
- Discussion Topics
- Results of Experiments
- Conclusions
- Acknowledgements
- Q & A

Introduction

Semiconductor and Semi equipment industries expect to see a strong upturn in the next few years. 5G, AI, Edge Computing, Persistent Memory, Integrated Power Management, and the transition to sub 5nm silicon technology are all driving the need for innovative packaging solutions.

These solutions integrate silicon produced with disparate process nodes and deliver maximum performance at optimal cost. Heterogeneous Integration, utilizing a multitude of interconnect methodologies (from Fan-out to Silicon Interposer, to Chiplet), addresses this challenge but requires unique solutions for efficient, cost effective die placement.

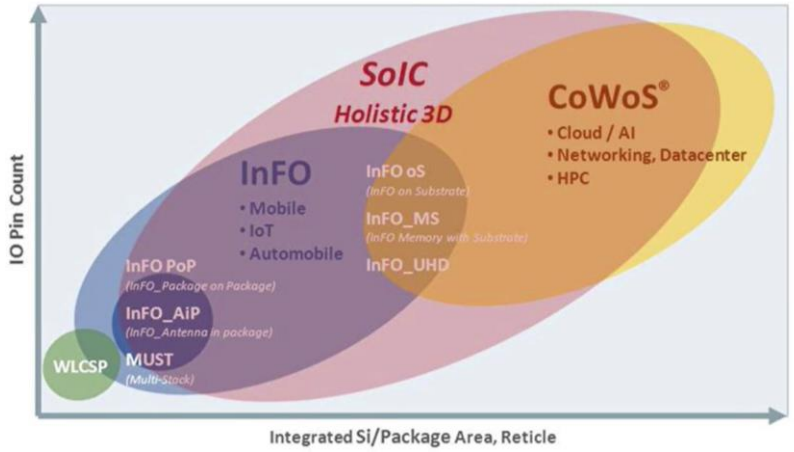
This presentation looks at the challenges and potential approaches for efficient and cost-effective solutions.

Market Drivers

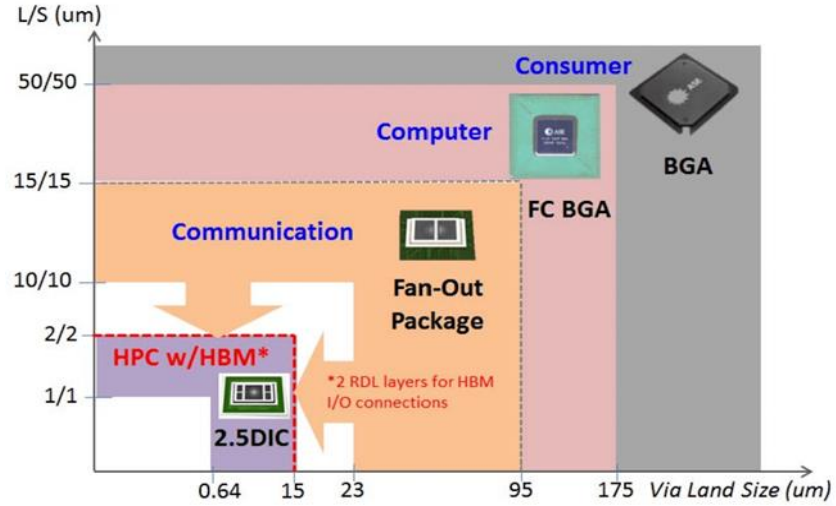
5G
AI
Edge Computing
Sub 5nm Silicon Technology
Moore's Law Scaling Limitations

Heterogeneous
Integration Solutions

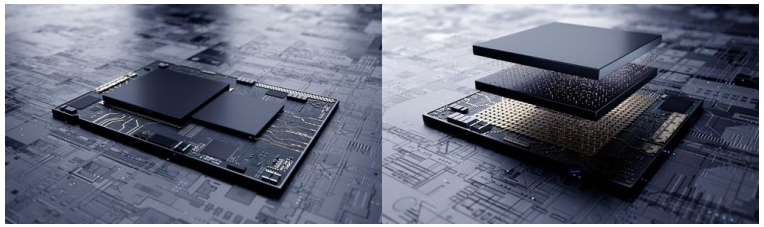
Example Technologies



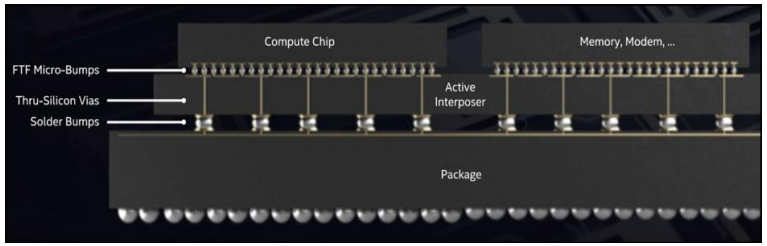
Source: TSMC



Source: ASE



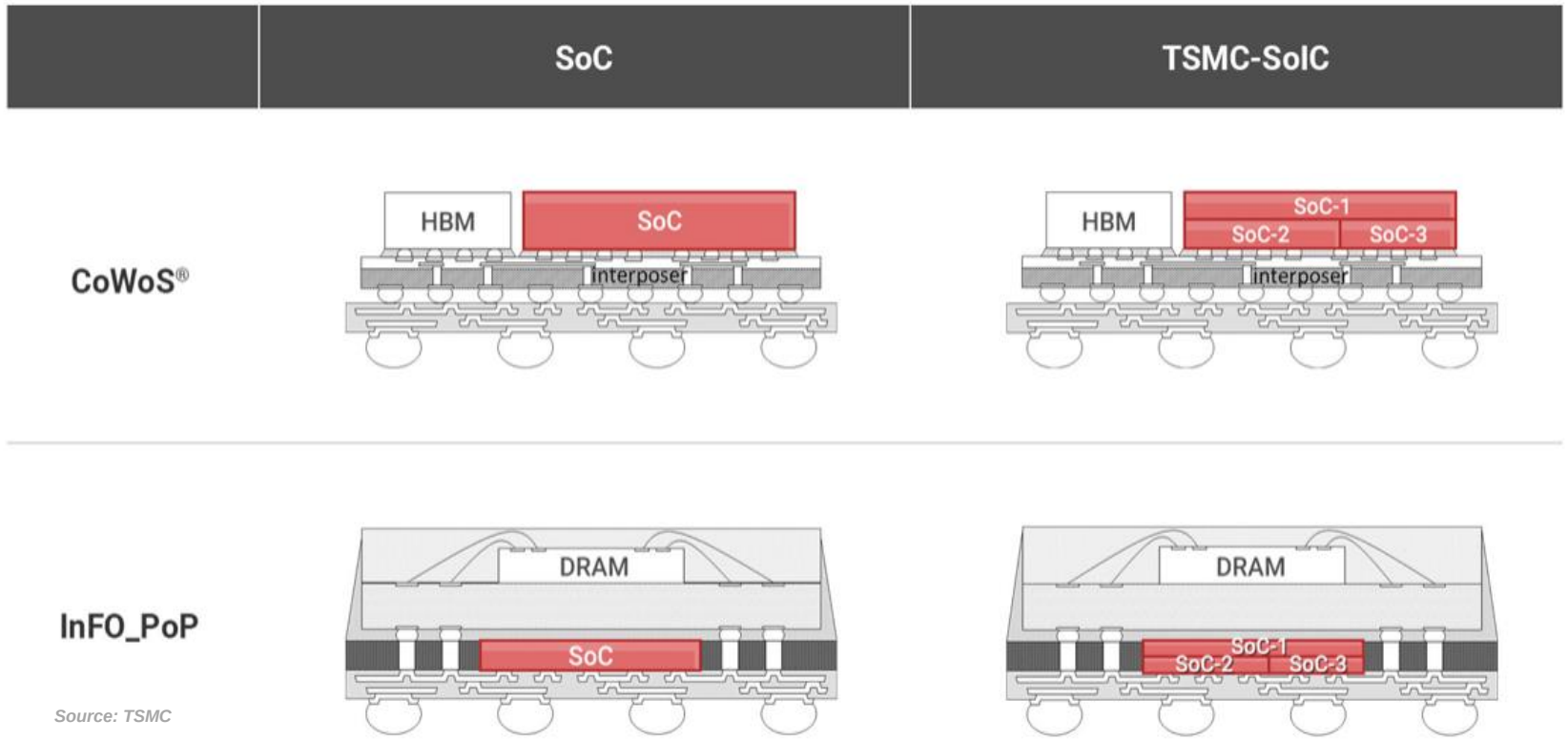
Source: Samsung



Source: Intel

Wafer Level System Integration Offerings – leveraging Silicon Foundry to the backend

InFO POP & CoWoS

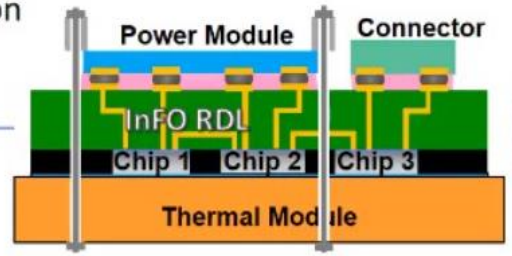


Source: TSMC

- SOIC replaces monolithic SOC chip with partitioned bonded multi-die product
- Multifunction assembly solutions are required

InFO SoW

Index	Key Advantages of InFO_SoW- Higher compute density & faster training time
Electrical Performance	✓ Low latency C2C communication ✓ High bandwidth density ✓ Low PDN impedance
Cost & Yield	✓ Mature InFO process ✓ Known-good chip ✓ Heterogeneous integration



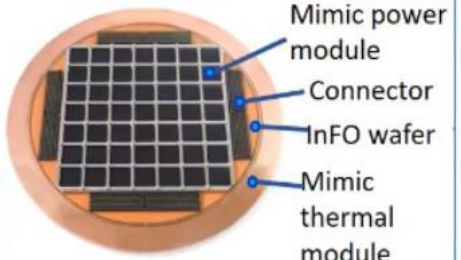
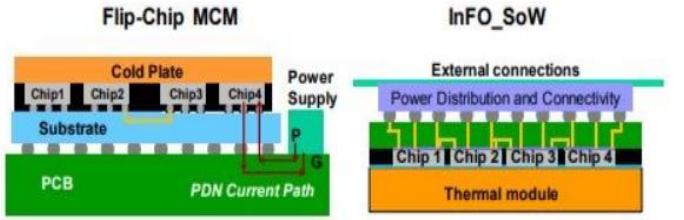


Figure 1: Key advantages of the InFO SoW package (Courtesy of TSMC)

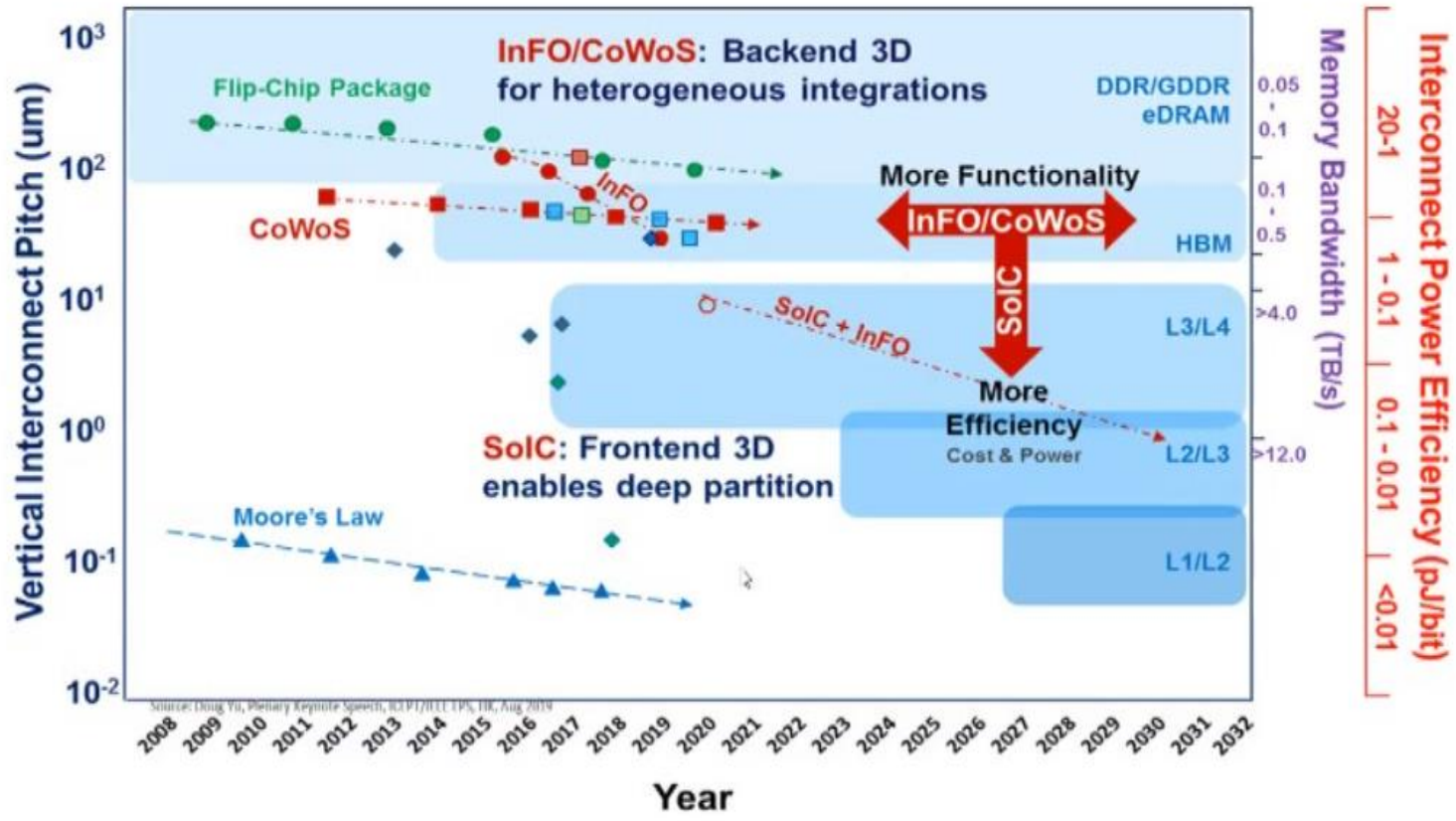


Line width / space (µm)	10 / 10	5 / 5
Line density	1x	2x
Bandwidth density	1x	2x
PDN impedance	1x	0.03x

Figure 2: Flip Chip packaging comparted to InFO SoW package (Courtesy of TSMC)

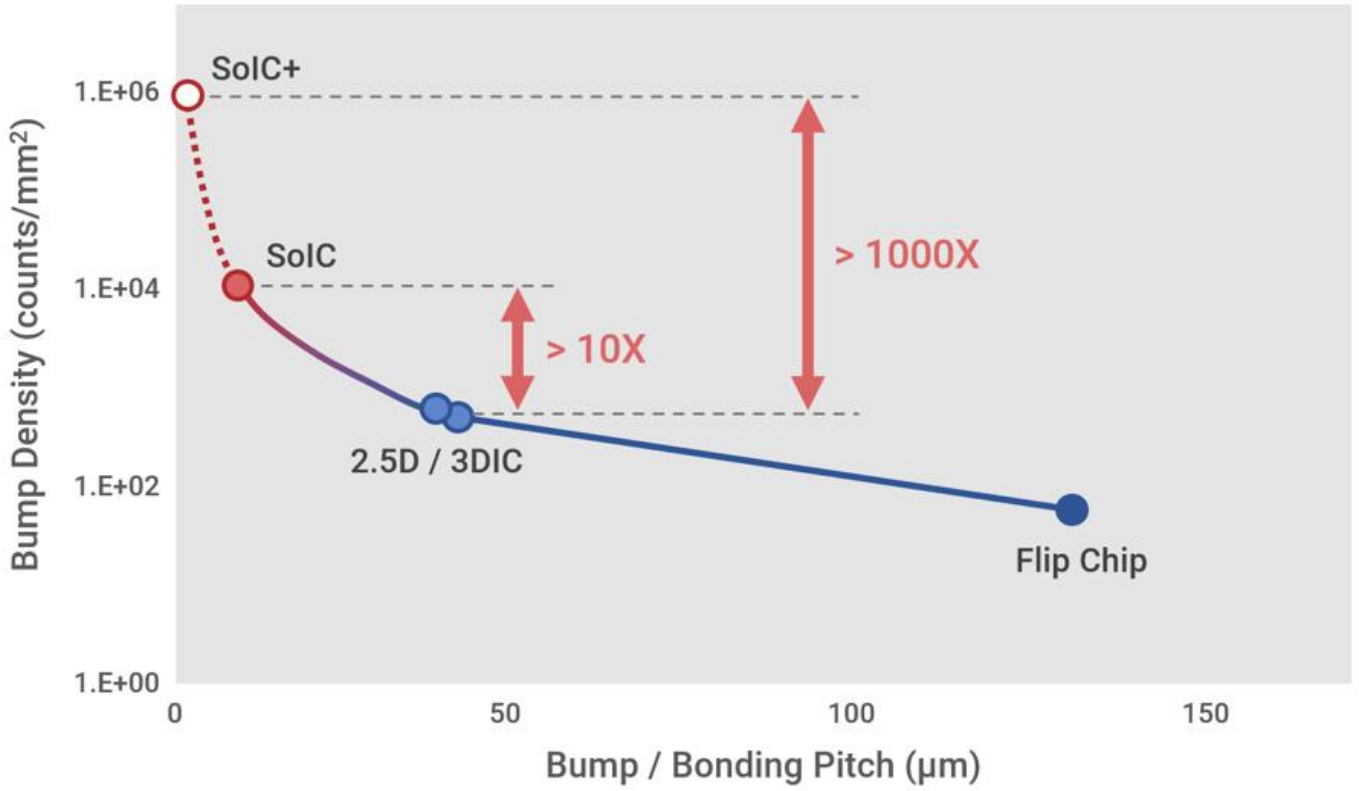
- Requires multifunction placement of die, connectors, thermal and power modules

BEOL Technology Roadmap



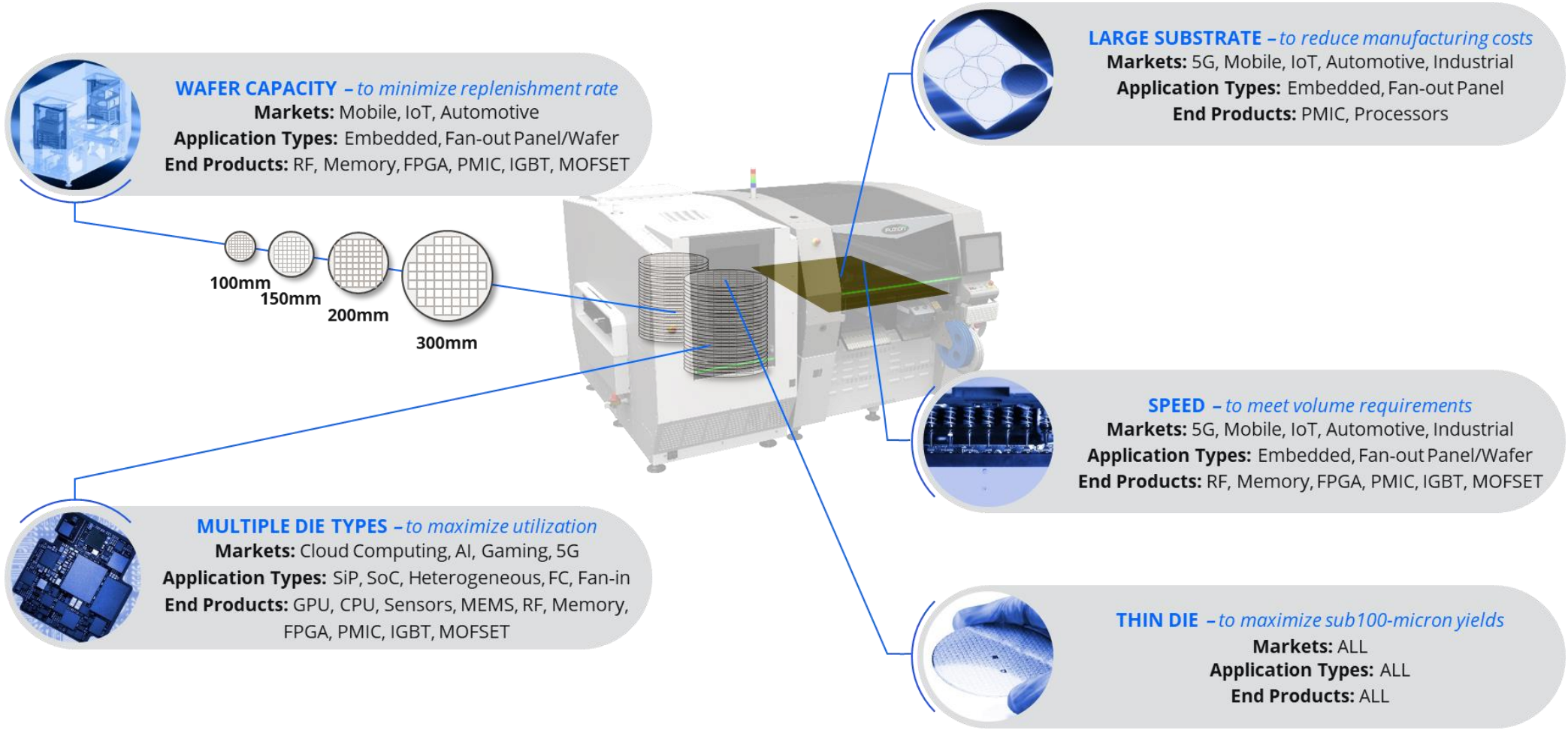
- InFO & CoWoS support backed 3D for heterogeneous integration
- SoIC enables front end 3D and SOC partition for highest interconnect power efficiency

Scaling by Technology



- Fan-out and TSV scale to 40um interconnect pitch, supportable with ~ 6-10um accuracy
- SoIC scales to micron level interconnect pitch, but still requires multi- “die” support

Solution Implications



Multi-Die HBM Case Study

Challenges

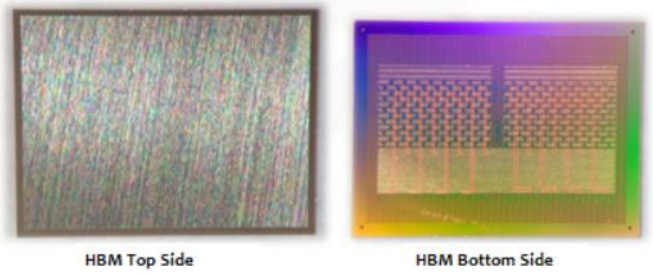
- Accuracy: Bump diameter of 25µm
- Four die per interposer substrate
- 4942 bumps
- Substrate fiducial FoV

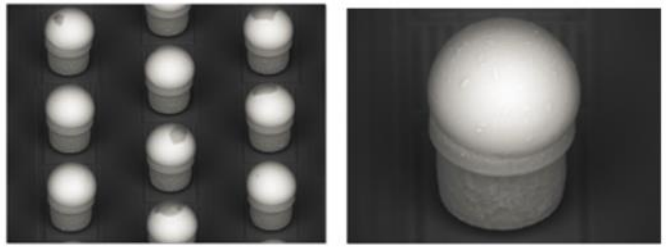
Solution

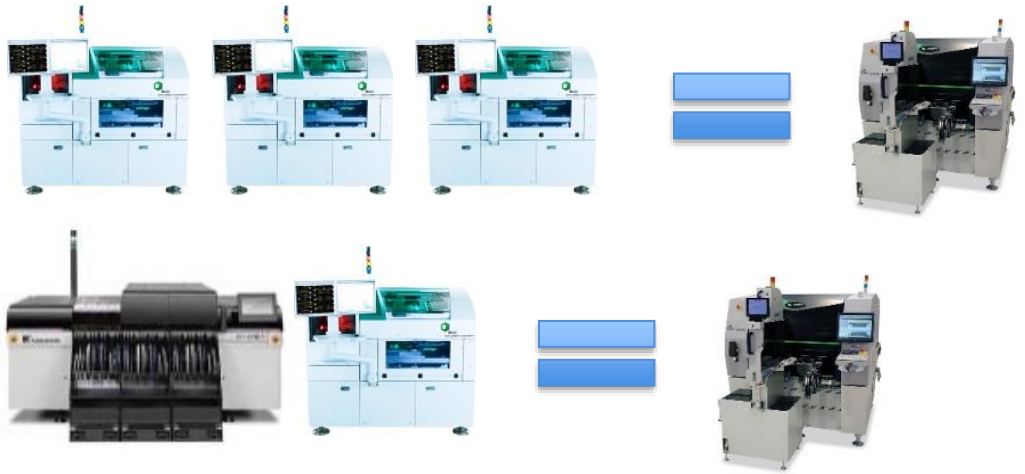
- FuzionSC with T&R
- LTFA
- Precision lifter with custom tooling

Benefit

- **Throughput and accuracy over large substrate**
- **Vision algorithm for bump inspection**
- **Post-bond inspection**







SiP Case Study

Challenges

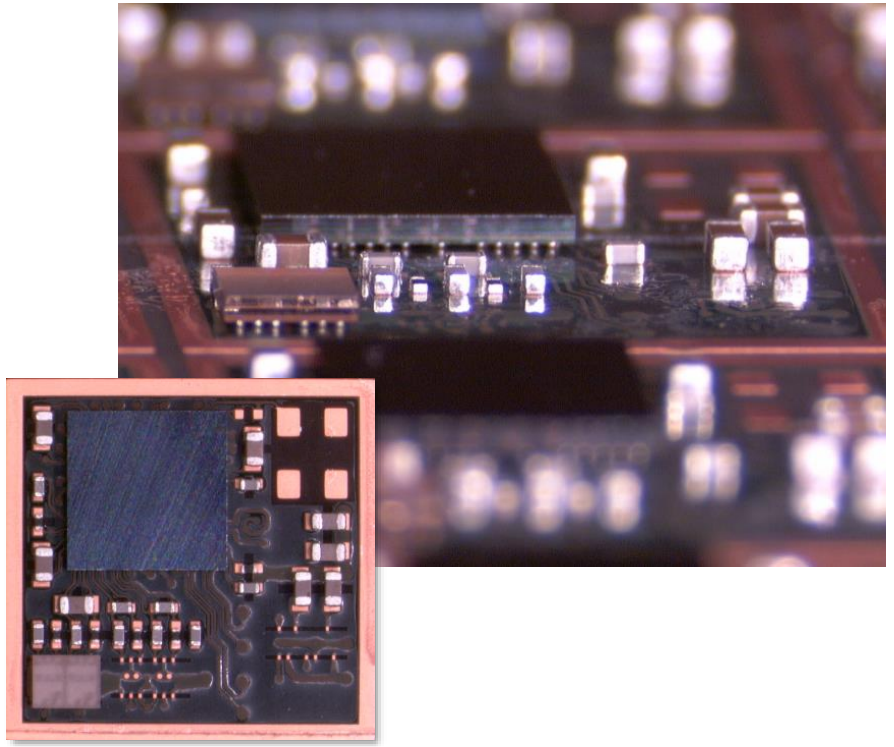
- Single station to place active + passive components
- Large die handling (100 x 100mm)
- Embedded in large panel (600 x 600mm)
- Flex substrate and component handling

Solution

- FuzionSC with T&R, Wafer feeder, and tray feeder
- Large substrate handler
- Bare wafer stage
- Precision LTFA lifter with custom tooling

Benefit

- **Throughput and accuracy over large substrate**
- **Large die handling up to 150 x 150mm**
- **All-in-one solution for both passive and active components**
- **High feeder capacity for complex SIP application**



Fan-Out Case Study

Challenges

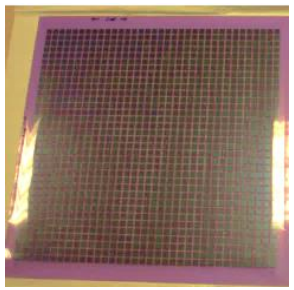
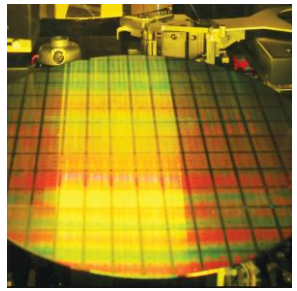
- Maximum panel size: 625 x 625mm
- <10µm placement accuracy
- >10K CPH
- Wide range of die size

Solution

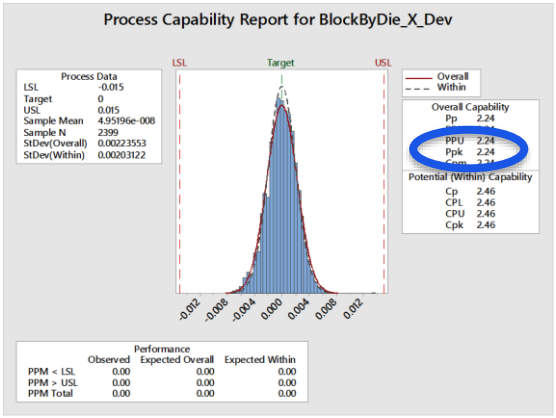
- FuzionSC with wafer feeder
- Large-panel kit
- Standard and bare wafer options

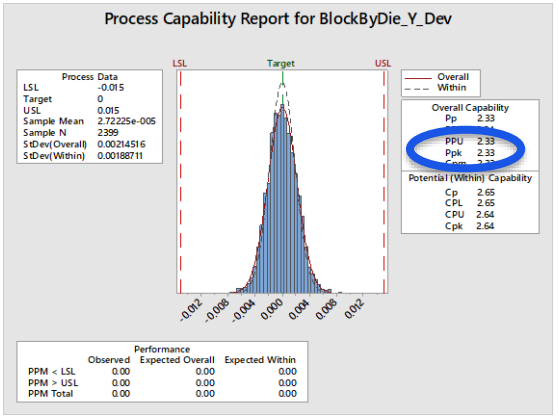
Benefit

- **Best cost per placement @ 10µm accuracy**
- **Large panel handling**
- **0201 metric – 150 x 150mm component range**
- **Extended solution for SiP, PoP, and embedded, lead frame application**


625mm PANEL ACCURACY





- **8 Panels built, measured (~ 30,000 placements)**
- **4 panels built at ~ constant temp, placement data used for trim**
- **4 Panels built using trim**
  - **Results: X,Y Cpk > 2.2 @ 15µm (~2.3µm Std Dev); Theta Cpk>3 @ .3deg**

High-Performance Computing Case Study

Challenges

- Large module size (~40mm x 50mm) – some warpage
- High CPH demand over small part count (4)
- Assemblies packaged in thick JEDEC trays – material handling

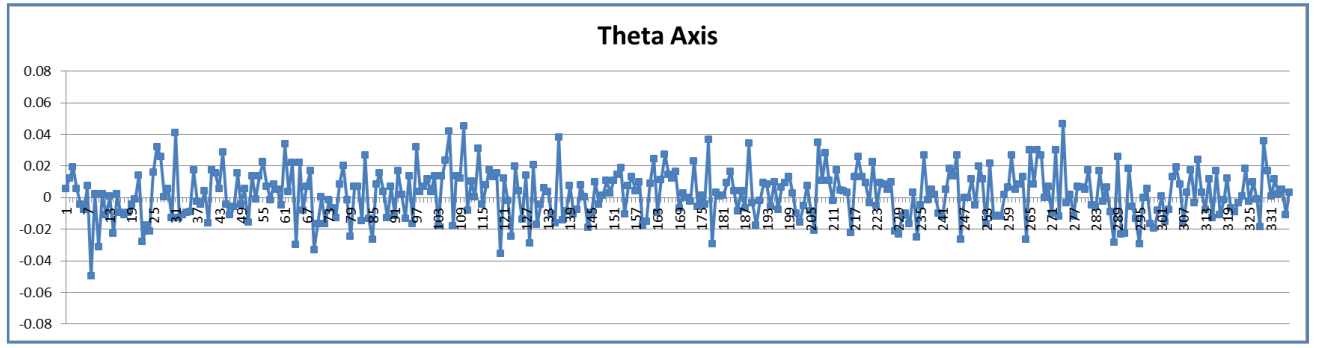
Solution

- FuzionSC
- Precision lifter with custom tooling
- JEDEC Tray Feeder (JTF) – 40 trays
- Automated tray handling cell

Benefit

- **Precision rotational (theta) accuracy**
- **Met throughput targets**
- **Delicate placement for large, warped parts**
- **Component & circuit-level traceability**
- **Fast tray exchange enables sustained high throughput**
- **Automated tray handling enables continuous operation**

6 Board Run (56 placements/board) @ 0, 90, 180, 270º Orientations
All theta orientations within 0.05º



All Rotations	Theta
Min	-0.04949
Max	0.04672
STDev	0.02
Avg	0.00
Cpk @ .075º	1.56

Questions?

Thank You!

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