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Thermal Performance Enhancement of Dual Side Molding SiP Module for 5G Application

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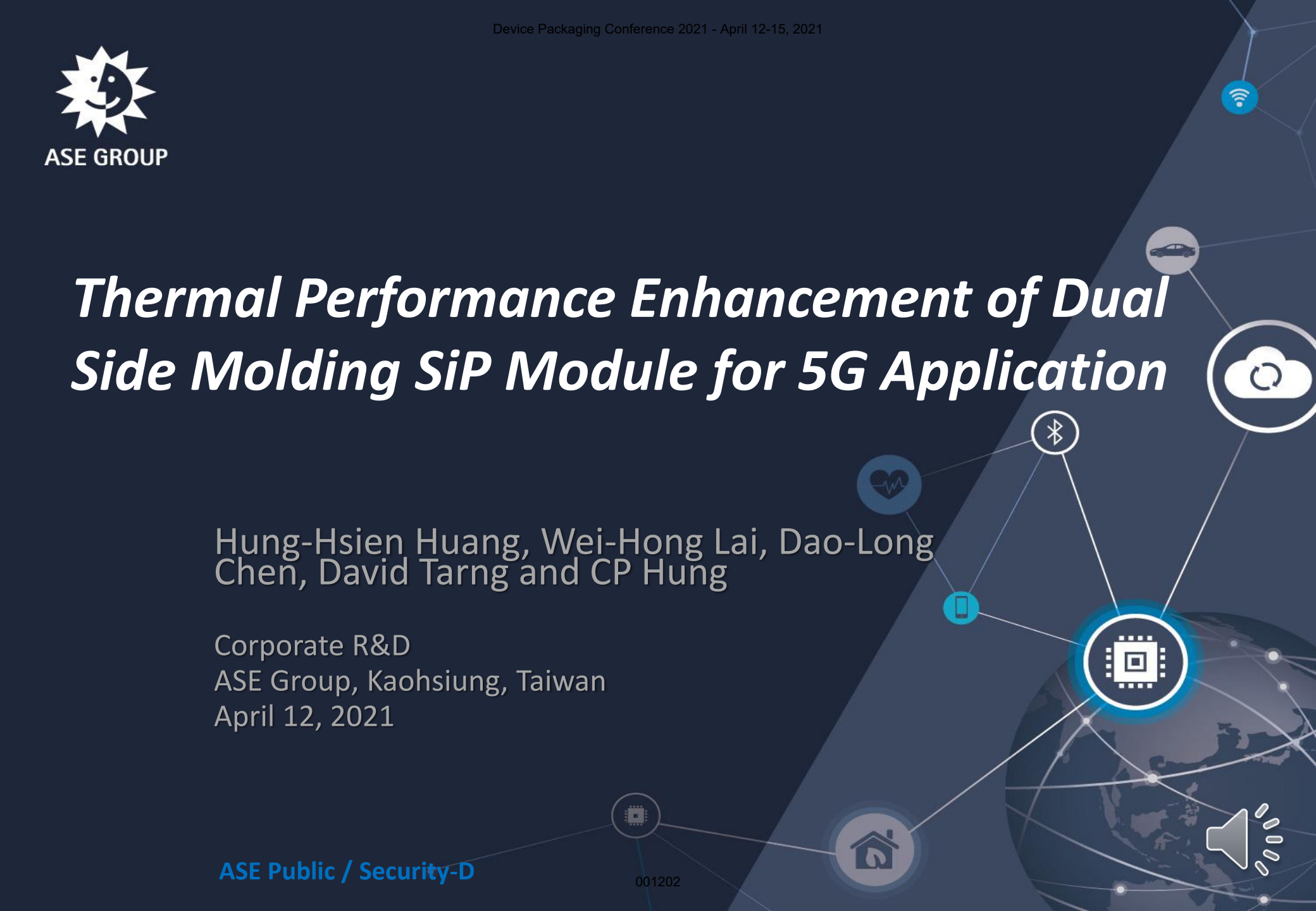

Outline

- Packaging Technology and Trend
- Introduction of Dual Side Molding System In Package (SiP)
- Thermal Solution with Metal Studded Layer
- Simulation Results with Different Modeling Methodology
- Summary

IC Packaging Technology – Value proposition

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Small form factor

- ✓Small form factor enables more design flexibility
- ✓Re-configure to fit 5G content in mobile devices

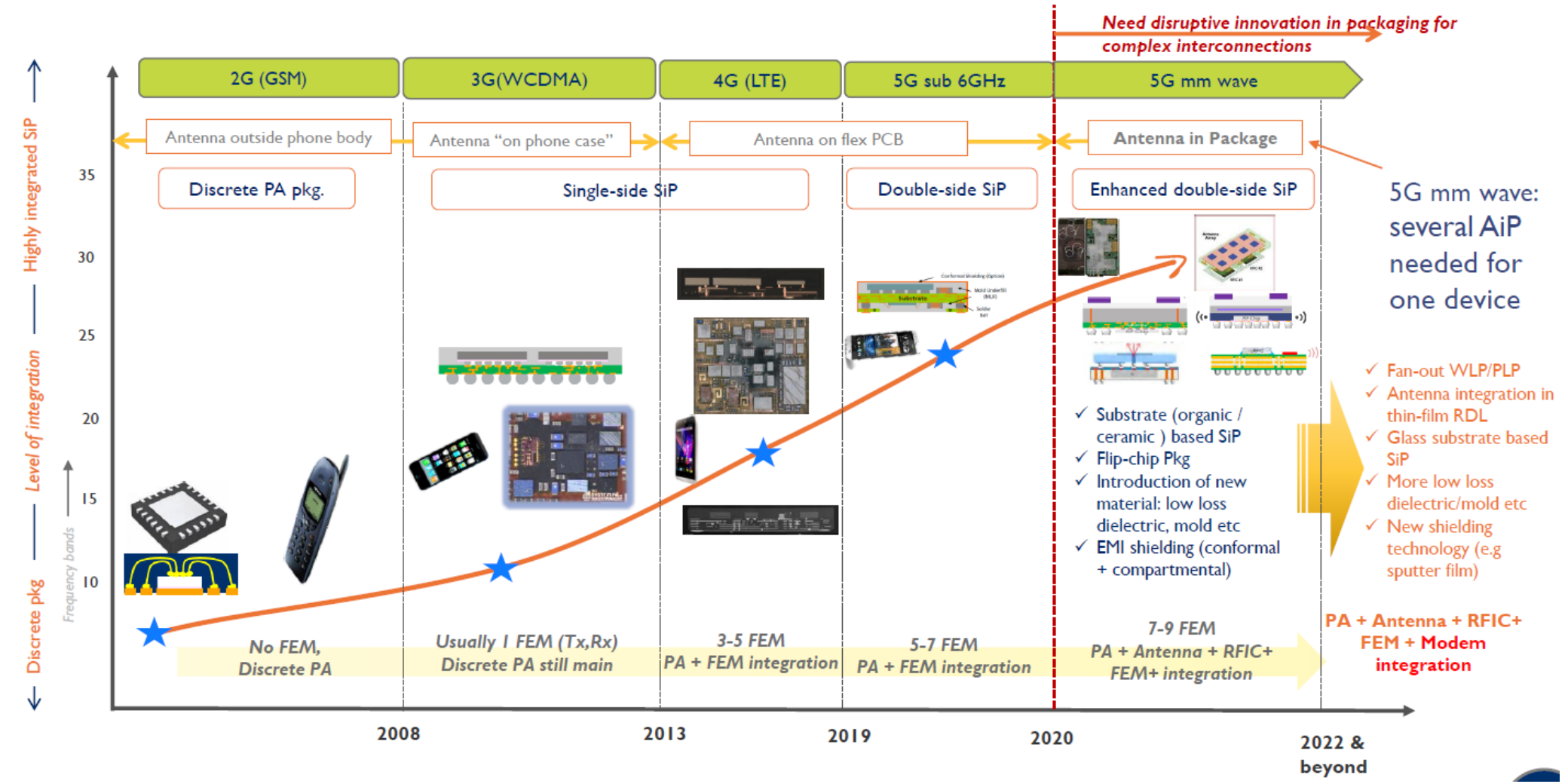
Turnkey solution

- ✓Complete turnkey System in Package (SiP) or Module
- ✓Including system design, module testing and simulation technology

Faster time to market

- ✓Pre-certification at module level
- ✓Components pre-integrated and tuned to meet performance specs

SiP Technology Roadmap: From Low Density to High Density



Source : Yole development

SiP's demand for high density, integrated, functional and all in one

Dual Side Molding SiP Module

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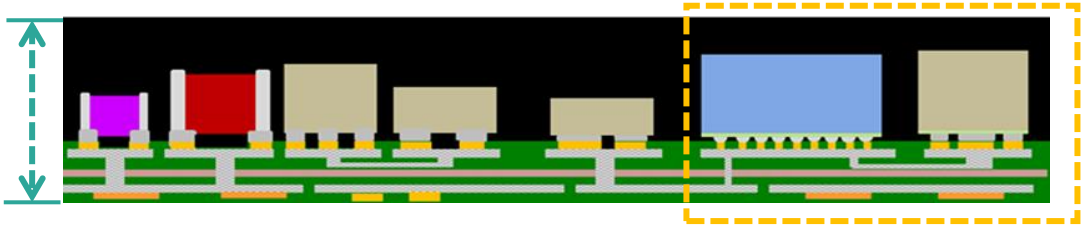
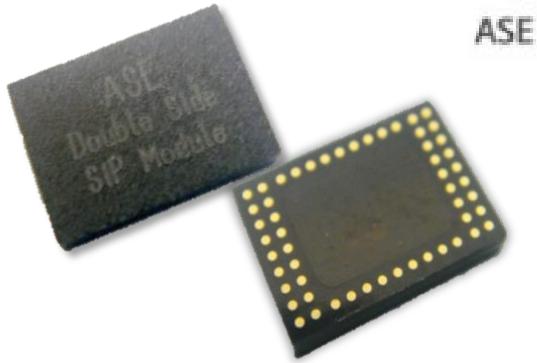
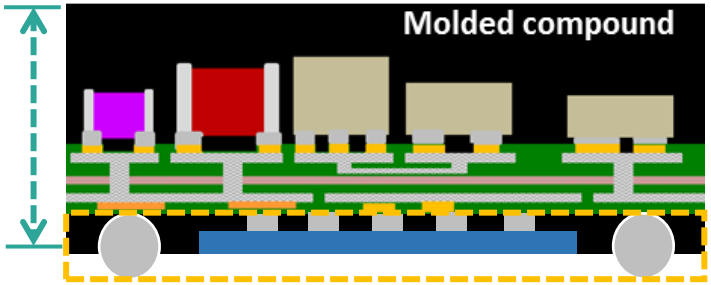
Normal Single Side Molding SiP Concept





ASE's Dual Side Molding (DSM) SiP Module

Dual Side Molding SiP Module Concept



- Reduce package size
- Increase SMT area
- Reducing the signal path
- Substrate-based solution for heterogeneous integration

Area reduced 30% ↑

Module total thickness 10% ↑

SiP Opportunities for Smart Phone

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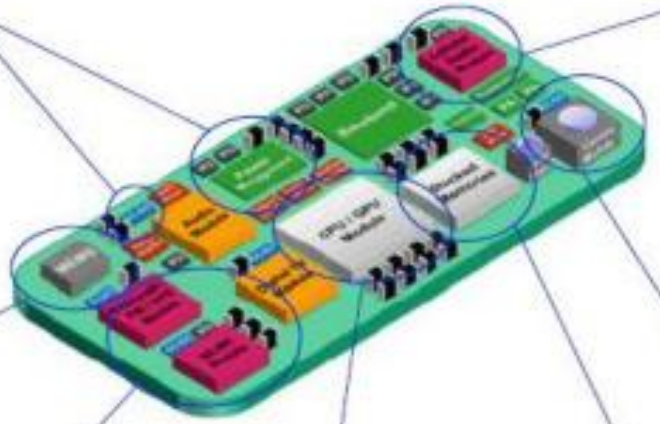
Integration / Miniaturization
Optimization / Simplification



Power Management
- Embedded substrate
- Low Frq. Conformal Shielding
- Thermal mgmt.


DC/DC


PMIC

RF/FEM
- Cu Pillar FC (irregular)
- Conformal/Compartment Shielding
- Embedded substrate


PAM


FEM


Tx/Rx

MEMS
- Embedded Substrate
- Wafer Level MEMS


Open cavity mold


Combo sensor

Sensor
- Non-standard form factor
- Extended BOM
- HD SMT, molding, shielding


Camera Module


Biometric Sensor

Wireless Connectivity
- EMI Shielding
- Embedded substrate
- Double-side Molding
- Antenna on Package


Combo
WiFi, BT, GPS, FM


Low Power Wireless

MPU/MCU
- 2.5D Organic/Si/Glass Interposer
- 3D TSV Die Stack
- HB PoP


High BW PoP


2.5D/3D TSV

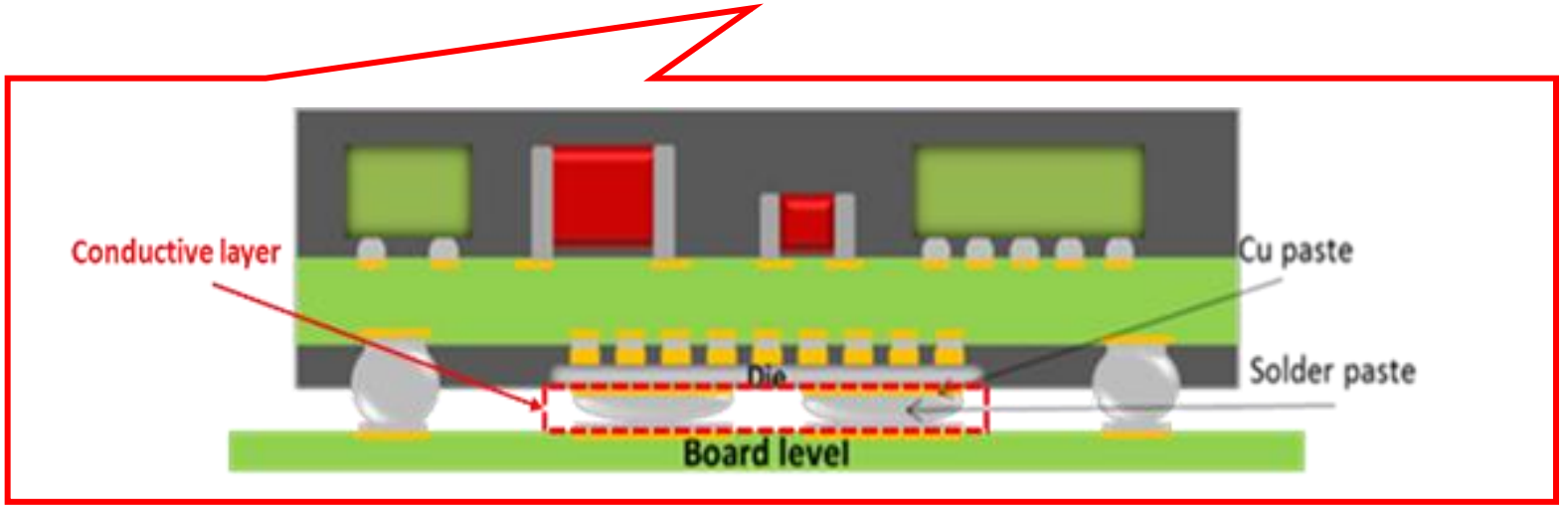
Storage
- Die & package stacking
- Double-side Molding
- Low Frq. Conformal Shielding


Component Flash

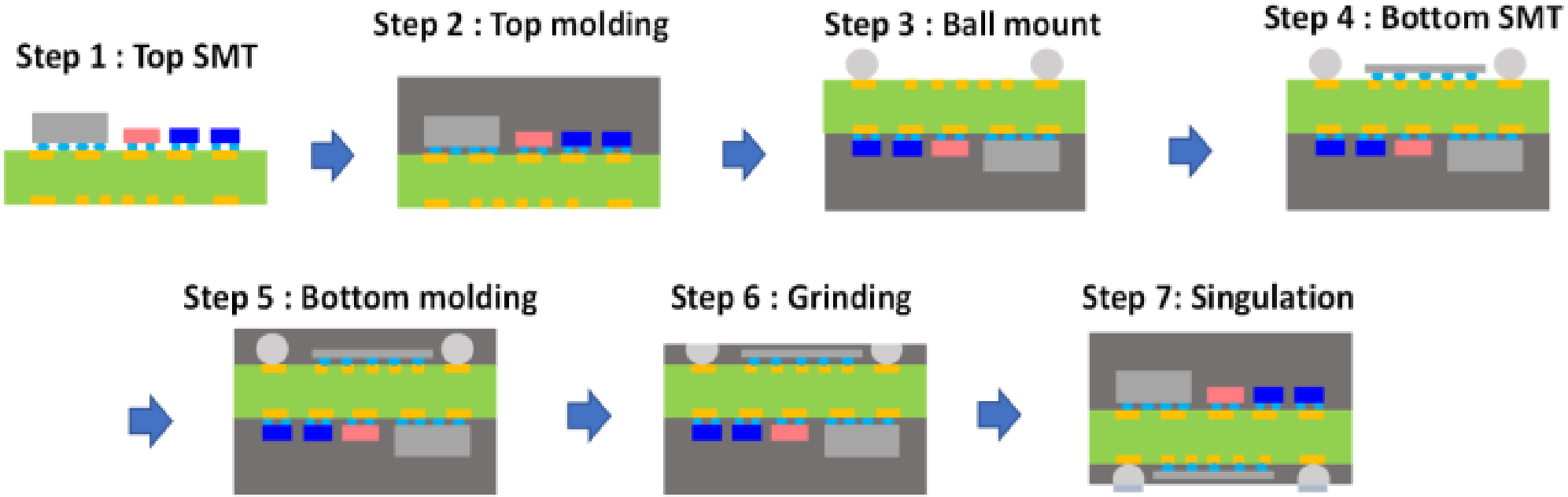

Micro SSD

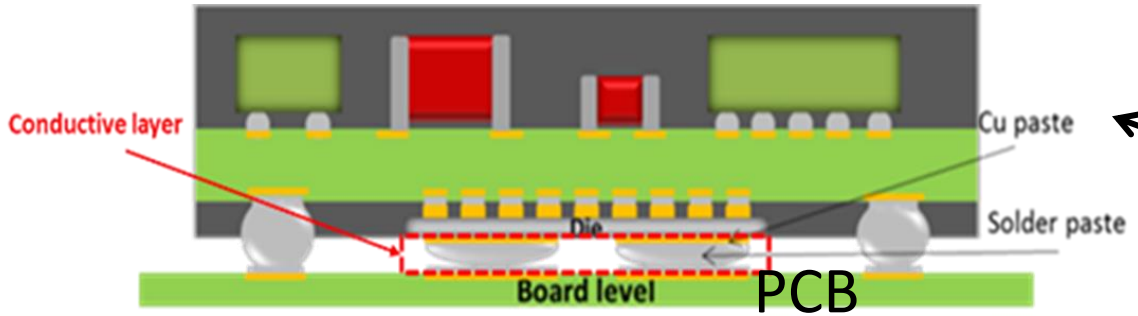
Thermal performance of DSM SiP

- **SiP level knobs to improve thermal performance**
  1. Lower max T_J
  2. Extends time-to-throttle
  3. Lower thermal gradient
  4. Allows uniform height at each side for coupling to heat sink
  5. Larger effective heat transfer area



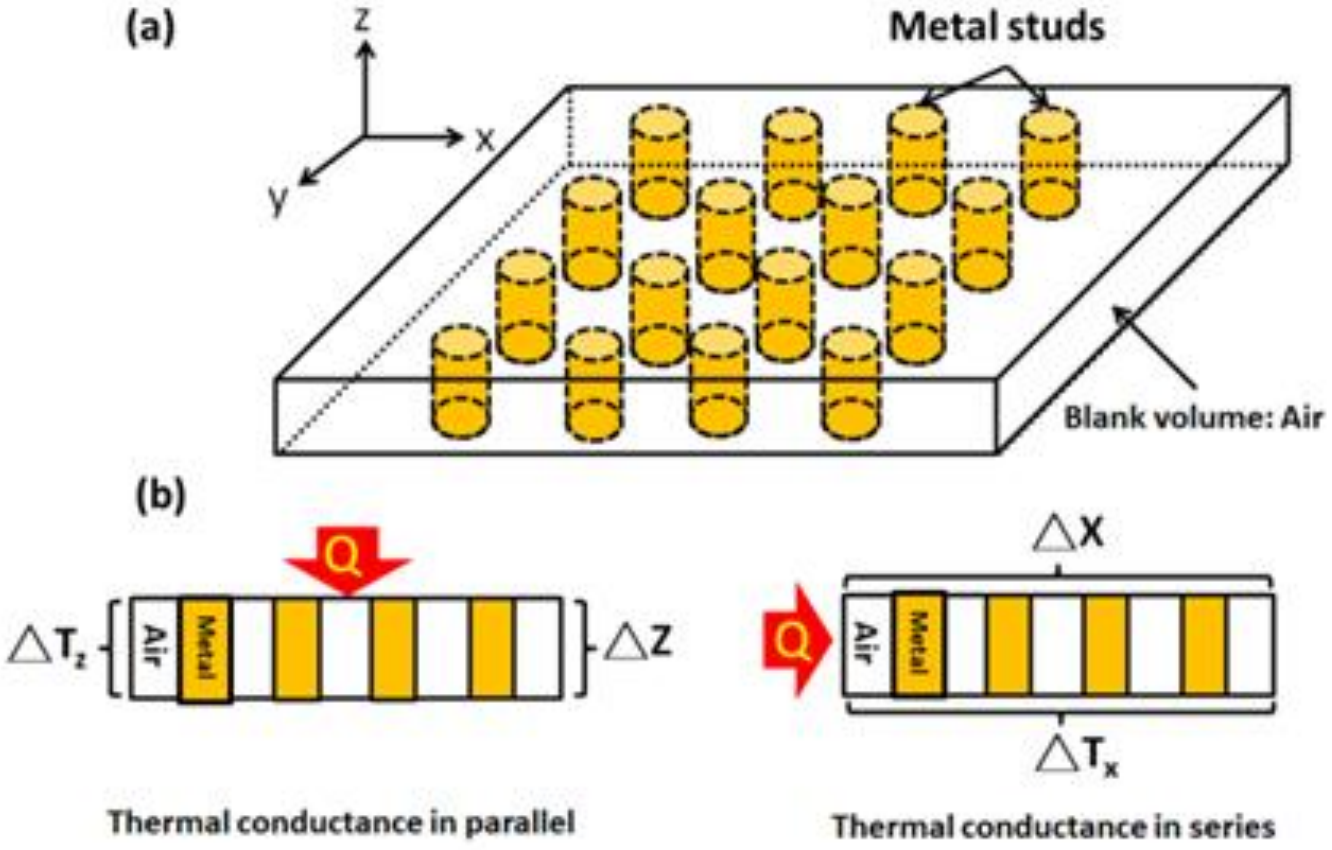
Process of a DSM SiP assembly





by printing process

Equivalent thermal conductivity extraction models



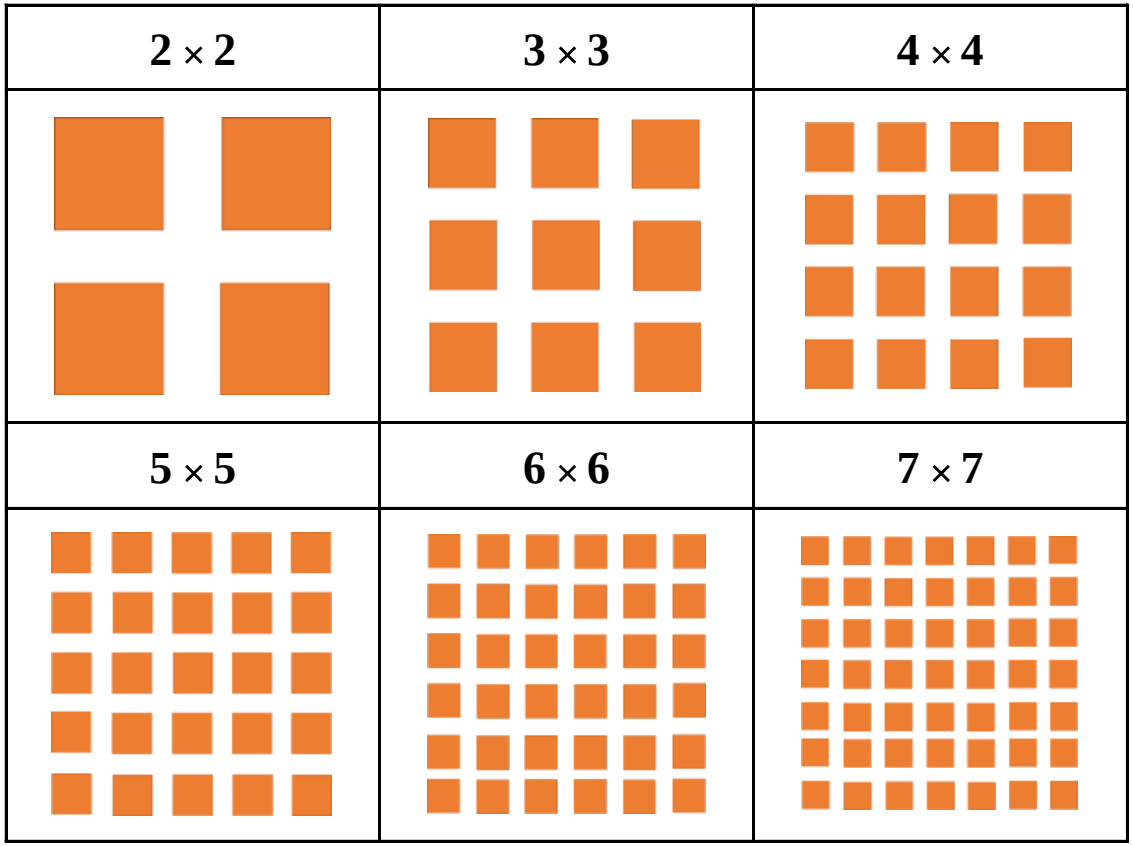
$$Q = k_{eq,z}\frac{\Delta T_z}{\Delta Z} \Rightarrow k_{eq,z} = Q\frac{\Delta Z}{\Delta T_z}$$

$$Q = k_{eq,x}\frac{\Delta T_x}{\Delta X} \Rightarrow k_{eq,x} = Q\frac{\Delta X}{\Delta T_x}$$

$$k_{eq,x} = k_{eq,y}$$

- **Thermal conductivity is anisotropic: Eq.(1) & (2)**
- **The equivalent K of different row arrays was fixed because the metal volume percentage is a constant**

Arrays of Metal Studded Layer

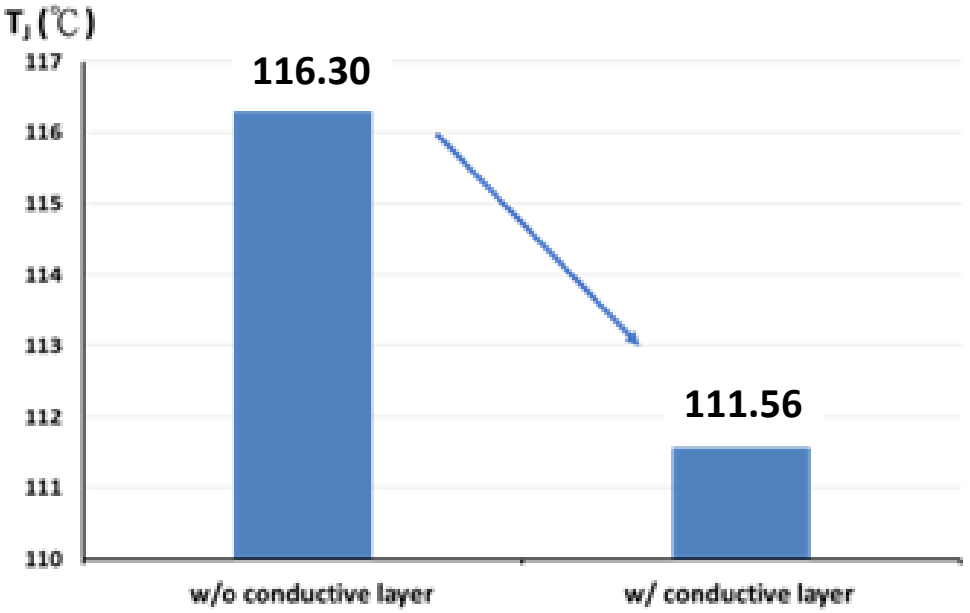


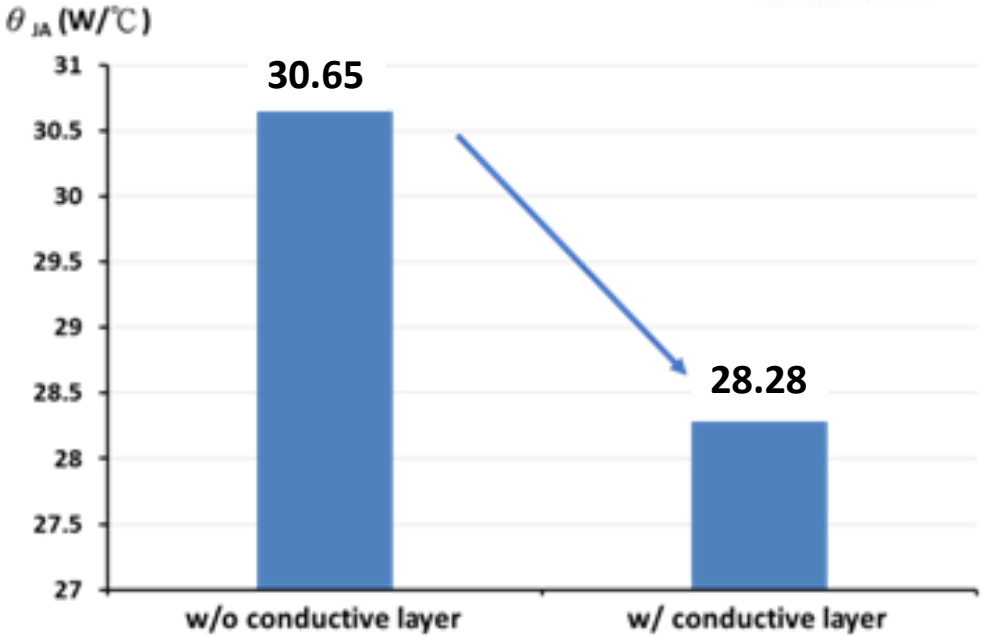
DSM SiP modeling information

SiP	
Size	**7 × 7 mm^2**
Main die size	**4 × 4 mm^2**
Main die thickness	**0.04 mm**
Power dissipation	**2 W (Uniform)**
Substrate	
Layers	**4 (1 + 2 + 1 laminate)**
Thickness	**0.8 mm**
JEDEC PCB	
Size	**101. 5 × 114.5 × 1.6 mm^3**
Layers	**4**

- **The square area was equivalent form the circle area**
- **The arrays and stud size were based on the conductive layer forming process (printing process)**
- **The total metal volume percentage was fixed.**

Simulation Results of Equivalent Model



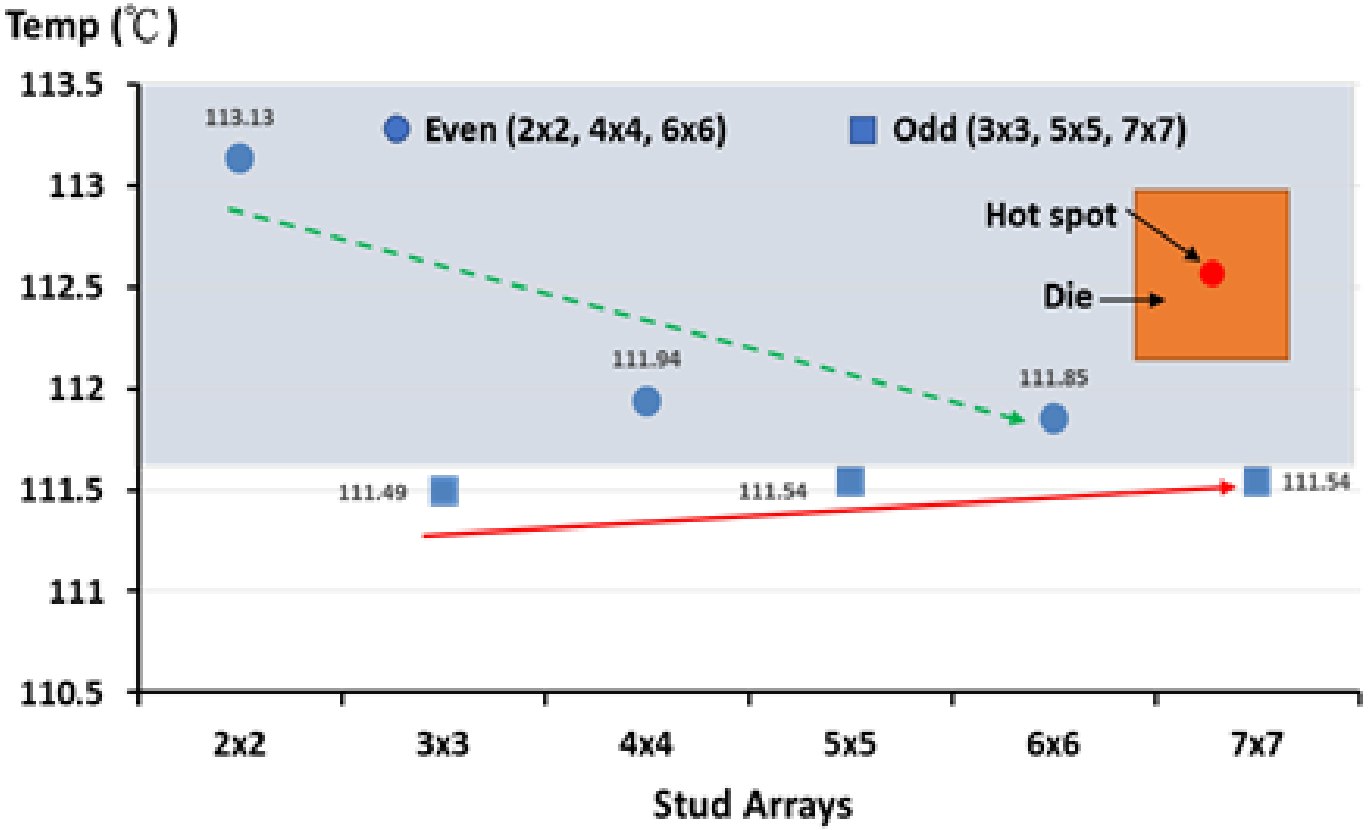


↓4%

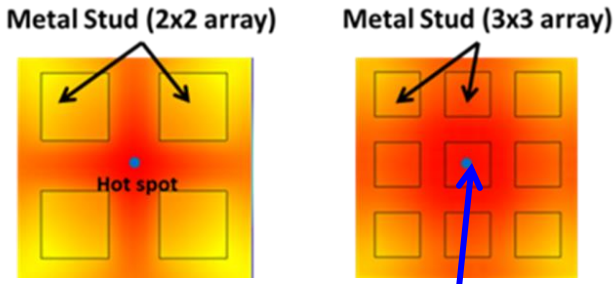
↓7.7%

- Thermal conductivity is anisotropic: Eq.(1) & (2)
- The equivalent K of different row arrays was fixed because the metal volume percentage is a constant

Thermal effect of metal studs on the detailed model



Temp. contour of2x2 & 3x3 array @ Uniform Power Dissipation



Effective heat transfer path (Metal stud on the center → Directly transfer the heat of center to PCB)

- **The improvement of thermal properties : Odd row arrays > Even row arrays**
- **Uniform power → The highest temp. located on the center of main die**
- **Need a path for effective heat transfer**

Summary

- **The thermal performance can be improved by conductive layer**
  - By mounting a metal studded layer as a thermal path at the top surface of the main die.
- **The methodology of modeling the studded layer significantly affects thermal simulation results.**
  - Well-correlated between actual failure location simulation
- **The real model that metal stud arrays with odd number of rows have a better thermal performance.**
  - Due to the fact that there is a metal stud present at the center which can act as a path for heat transfer under the hotspot (chip center).

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Thank You

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