From Technologies to Market

International Microelectronics Assembly and Packaging Society

Bringing together the entire microelectronics supply chain™

3D Packaging from Edge to the Datacenter: An Imperative for the next decade

IMAPS 2021

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YOLE Développement

SPEAKER

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Vaibhav Trivedi is a Senior Technology & Market analyst at Yole Développement (Yole) working with the Semiconductor & Software division. Based in the US, he is a member of Yole's advanced packaging team and contributes to analysis of ever-changing advanced packaging technologies. Vaibhav has 17+ years of field experience in semiconductor processing and semiconductor supply chain, specifically on memory and thermal component sourcing and advanced packaging such as SiP and WLP.

Vaibhav has held multiple technical and commercial lead roles at various semiconductor corporations prior to joining Yole.

Vaibhav holds a Bachelor of Science in Chemical Engineering, and Master of Science of Material Science from University of Florida in addition to an MBA from Arizona State University.

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PRESENTATION OUTLINE

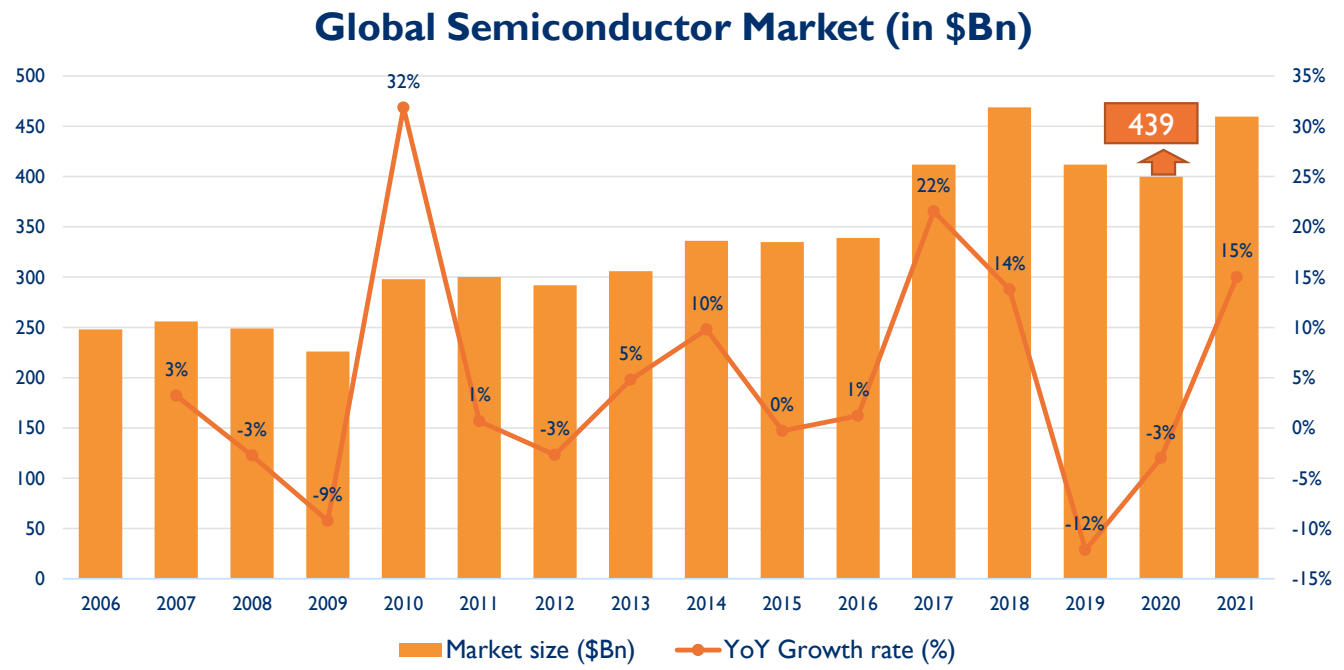
- Overview of the *Semiconductor Market* Outlook & Forecast
  - Pandemic Impact on Semiconductor Outlook and Advanced Packaging Forecast
- 3D Stacked High End Package Definition & Key Drivers
- Overview of the 3D Package Market/Forecast
- Leading 3D Packaging Form Factors
- Key Markets & Applications for 3D Package
- Ever evolving System in Package supply chain and new emerging models & future trends
- Yole Offerings in Advanced Packaging and other products

Overview of Semiconductor Market/Forecast and Effects of the Pandemic

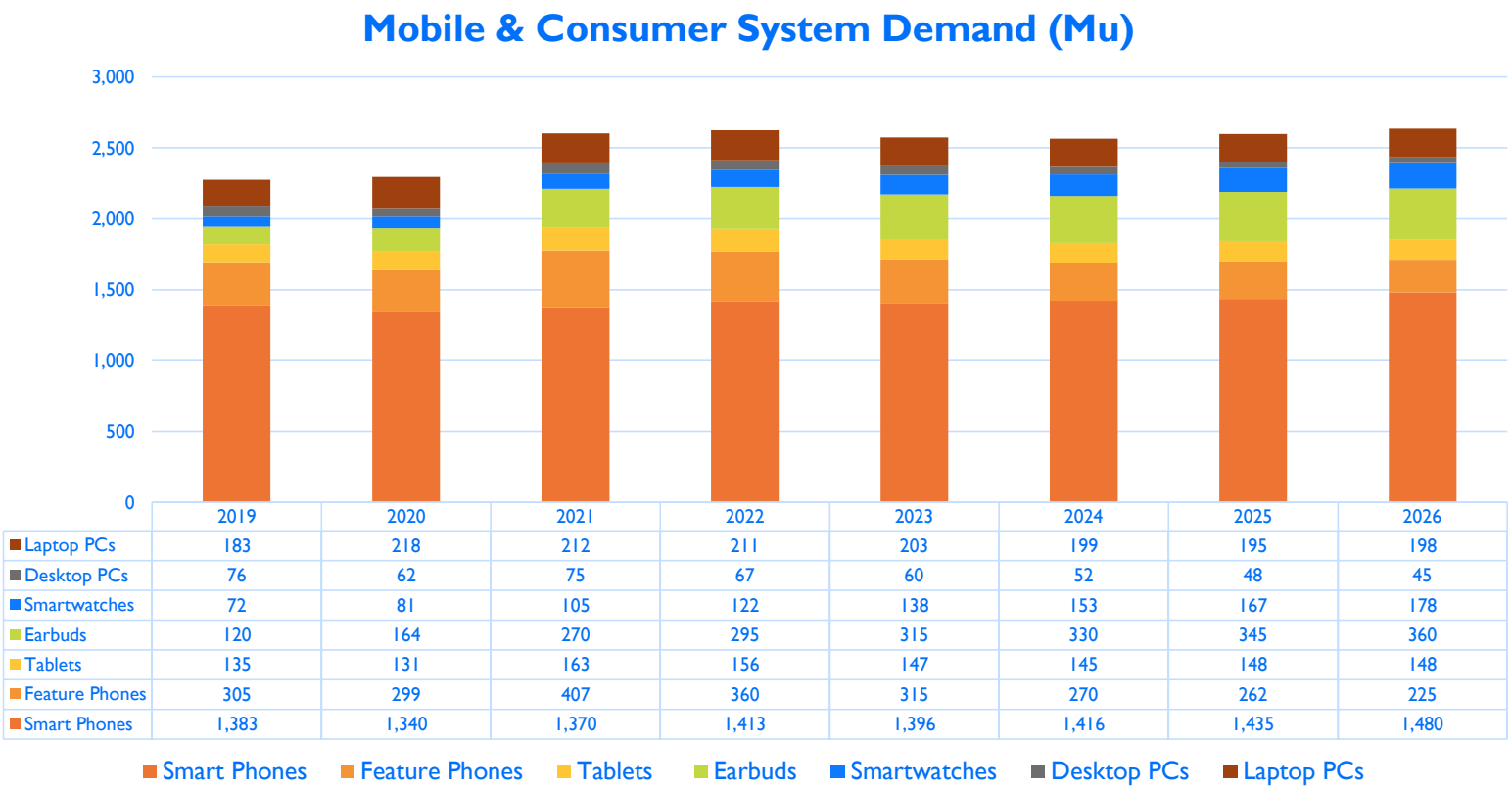
SEMICONDUCTOR BUSINESS OUTLOOK

After 2 successive high growth years, global semiconductor market growth decline 12% YoY to reach ~$412B in 2019. The decline is attributed to the cyclicality in product pricing, sluggish phone demand and global trade unrest. FY 2020 semiconductor market grew amid Coronavirus Pandemic slightly and FY 2021 expected to be another incremental growth robust year.

Semiconductor industry grew 5-6% YoY to reach ~$439B in 2020 as Coronavirus Pandemic increased consumer and infrastructure demand globally..



MOBILE & CONSUMER DEMAND (M UNITS)

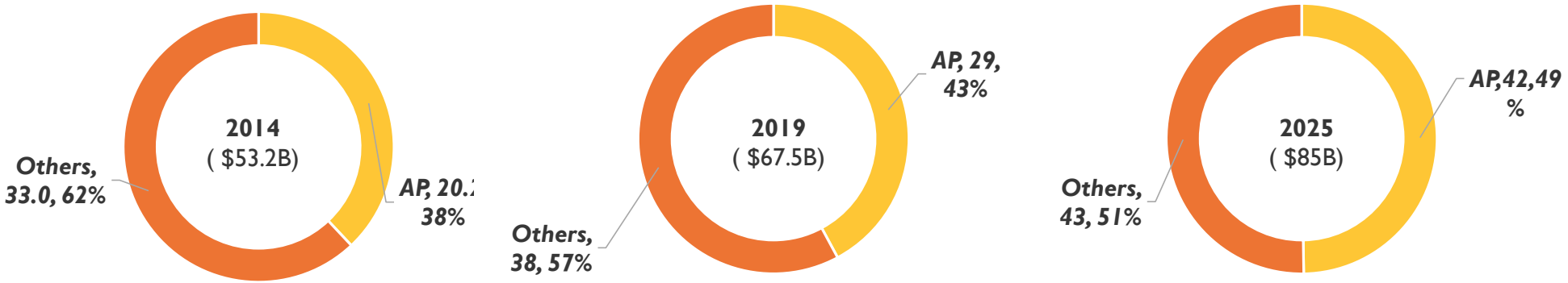


	2019	2020	2021	2022	2023	2024	2025	2026
Laptop PCs	183	218	212	211	203	199	195	198
Desktop PCs	76	62	75	67	60	52	48	45
Smartwatches	72	81	105	122	138	153	167	178
Earbuds	120	164	270	295	315	330	345	360
Tablets	135	131	163	156	147	145	148	148
Feature Phones	305	299	407	360	315	270	262	225
Smart Phones	1,383	1,340	1,370	1,413	1,396	1,416	1,435	1,480

- Smartphone and tablet demand to remain saturated over next five years with 1.3% (2020-2026) growth while wearables devices grow at ~14% (2020-2026).

ADVANCED PACKAGING OVERVIEW **2014 to 2025**

Revenue Split ($B)



- *Advanced packaging market revenue is swiftly catching up with the traditional packaging market.*
- *In 2014, advanced packaging accounted for 38% of total packaging market. However, its market share will increase to ~49% (almost half of market) in 2025 to reach ~$42B*
- *In 11 year period, advanced packaging revenue almost catch that of the traditional packaging*

3D Packaging Definition & Key Drivers

SEMICONDUCTOR INDUSTRY

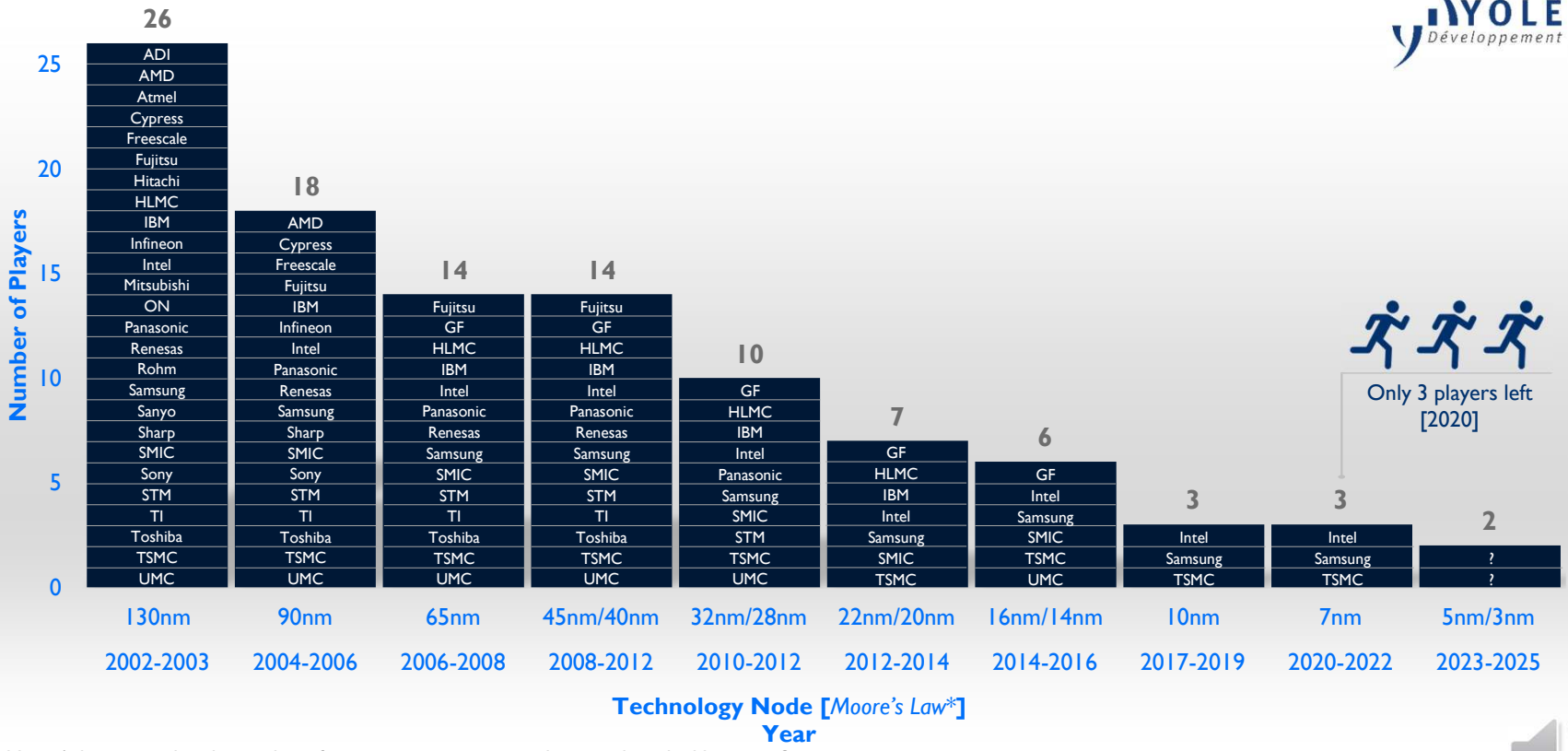
Chronological order of Players pursuing Moore's Law

Moore's law has guided the global semiconductor industry for past decades (since 1965), improving both performance and cost through node scaling.

After 2002 (130nm), the industry has been consolidating extensively. Limitations in scaling has disrupted companies competing in this business.

Presently, it is an oligopoly market, with a handful of key players remaining.

Number of Players with leading-edge manufacturing capabilities



* Moore's law states that the number of transistors in an integrated circuit chips doubles every 2 years
Data referenced from Intel and WikiChip

LEADING-EDGE NODE: STEEP INVESTMENT COST

FE investment cost is increasingly hefty – Seeks Alternative in Advanced Packaging

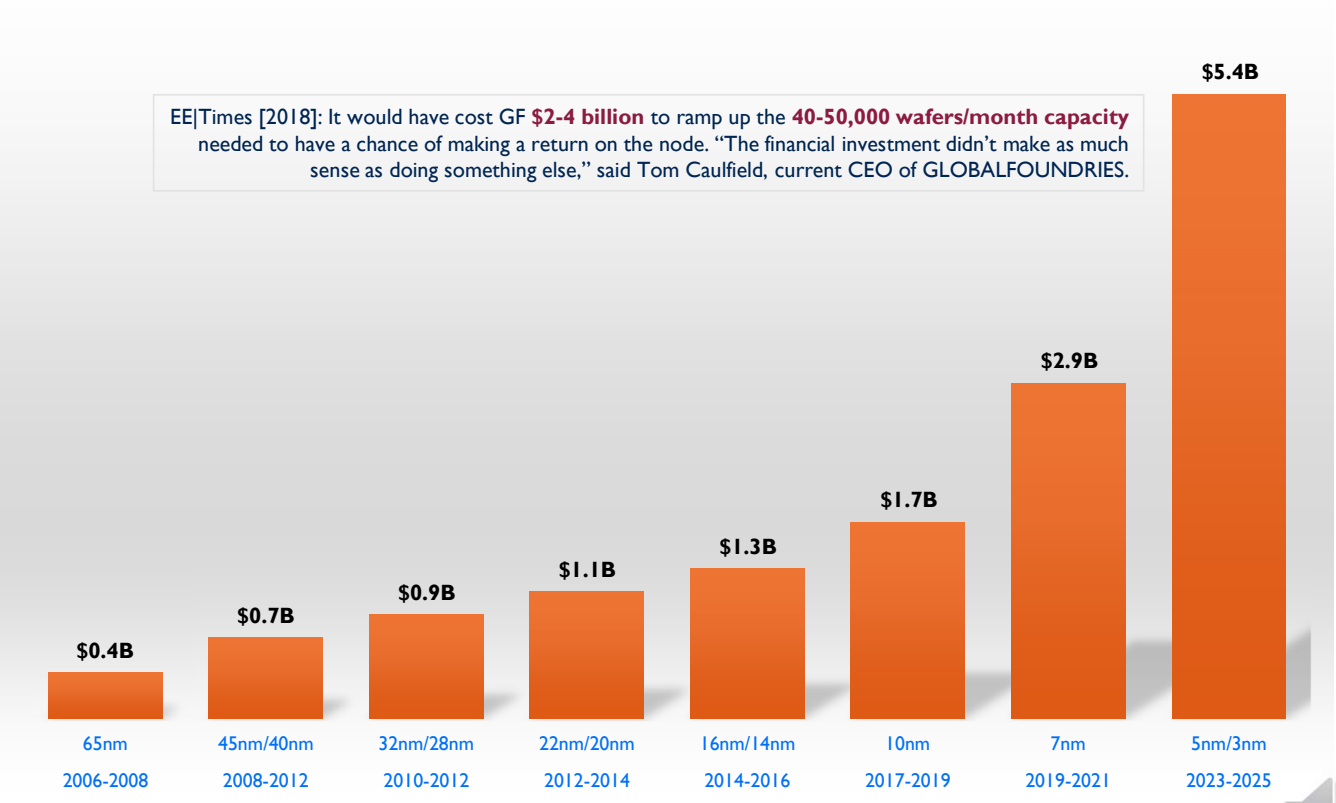
The cost of building and equipping a facility with 5 nm production lines is expected to run at $5.4 billion which is 5 times more than $1.1 billion required for a 20 nm fab production lines between in 2012-2014. Such steep investment cost is the main barrier and key reason why more semiconductor players are falling out of the technology scaling race.

Most of the increased cost is related to the greater precision in design. As the nodes get smaller, development becomes more confounding as engineers now must deal with quantum effects, minor structural variations, and factors like testing, validation and IP qualification, which only only further complicate and delay the development process.

Presently, the industry is seeking alternative to design & manufacture latest SoC using SiP and chiplet based approach by leveraging different Advanced Packaging technologies and a mix of both latest & matured nodes.

This way, cost and time-to-market can be reduced while at the same time economically enhance the system performance.

Investment cost for Leading-edge Fab and R&D



Source: McKinsey & Company; Yole Développement Analysis

HIGH-END PERFORMANCE PACKAGING DEFINITION

Yole's Definition of High-end performance Packaging

Presently, there is no acknowledged mainstream definition for High–end performance Packaging within semiconductor industry.

If distinct advanced packaging technologies, including Flip-Chip, Embedded die, 2.5D Si interposers, 3D-IC, Fan-in, Fan-out and Hybrid Bonding, are considered as High-end performance Packaging, then this will be over generalizing High–end performance Packaging.

This is because not all advanced packaging technology is high performing. For example, Flip-Chip and Fan-Out Packaging can exist both in high-end and low-end applications.

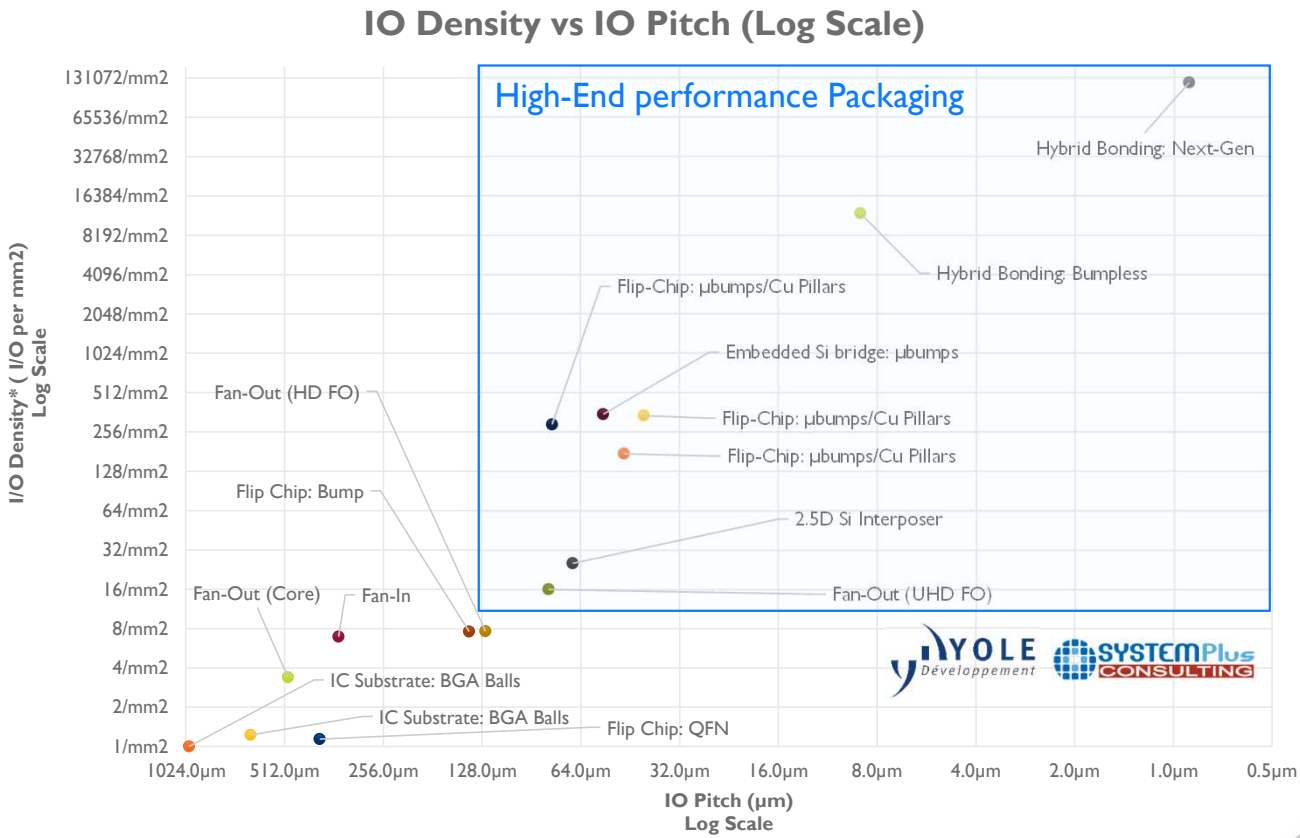
In order to prevent such confusion, Yole clearly focuses and defines High-end performance Packaging based on IO Density and IO Pitch.

--- DEFINITION ---

High-end performance Packaging is defined as a forefront packaging technology, which value-adds device performance with high IO Density (≥16/mm²) and fine IO Pitch (≤130µm)

--- TERMINOLOGY ---

In this report, "High-end performance Packaging" will be used interchangeable with "High-end Packaging" and "HEP" abbreviation



*I/O Density refers to total number of IOs per package platform area
Plot is generated based Yole Développement's and System Plus Consulting's database, with reference to industry average value and assumptions.

HIGH-END PERFORMANCE PACKAGING: INTRODUCTION

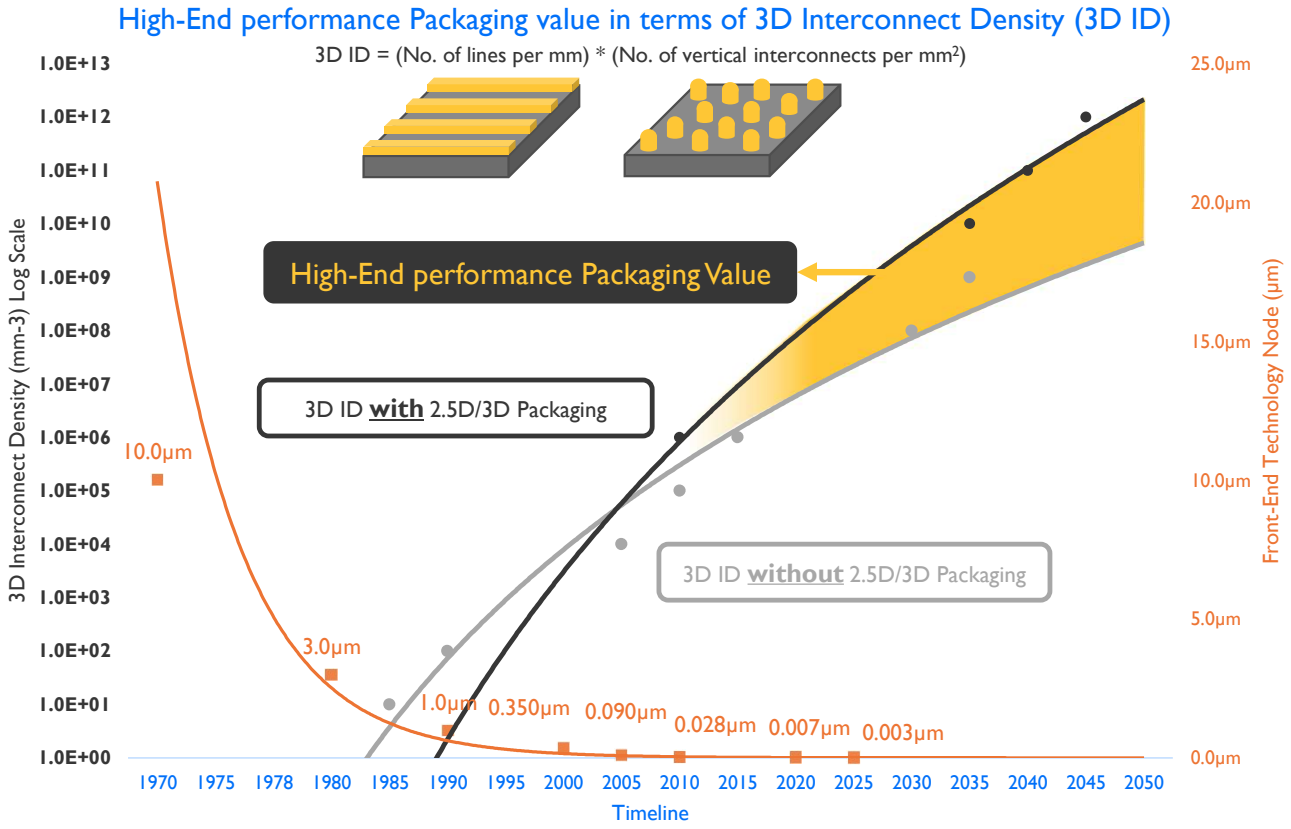
How is high-end performance packaging valuable amongst leading-edge players?

Although Moore's Law remains alive for over five decades, it is no longer cost efficient when it comes to advanced nodes and lesser manufacturers can keep up.

Traditionally, the IC industry relied on traditional chip scaling and innovative architectures for new devices. In chip scaling, the idea is to pack more transistors on a monolithic die or system-on-a-chip (SoC) at each process node, enabling faster chips with a lower cost per transistor. But traditional chip scaling is becoming more difficult and expensive at each node.

While scaling remains a work-in-progress in the background, the industry is now diligently utilizing Advanced Packaging technologies to put multiple advanced and/or matured chips in a single package, also known as heterogeneous integration -2.5D/3D Packaging, to extend 3D Interconnect Density.

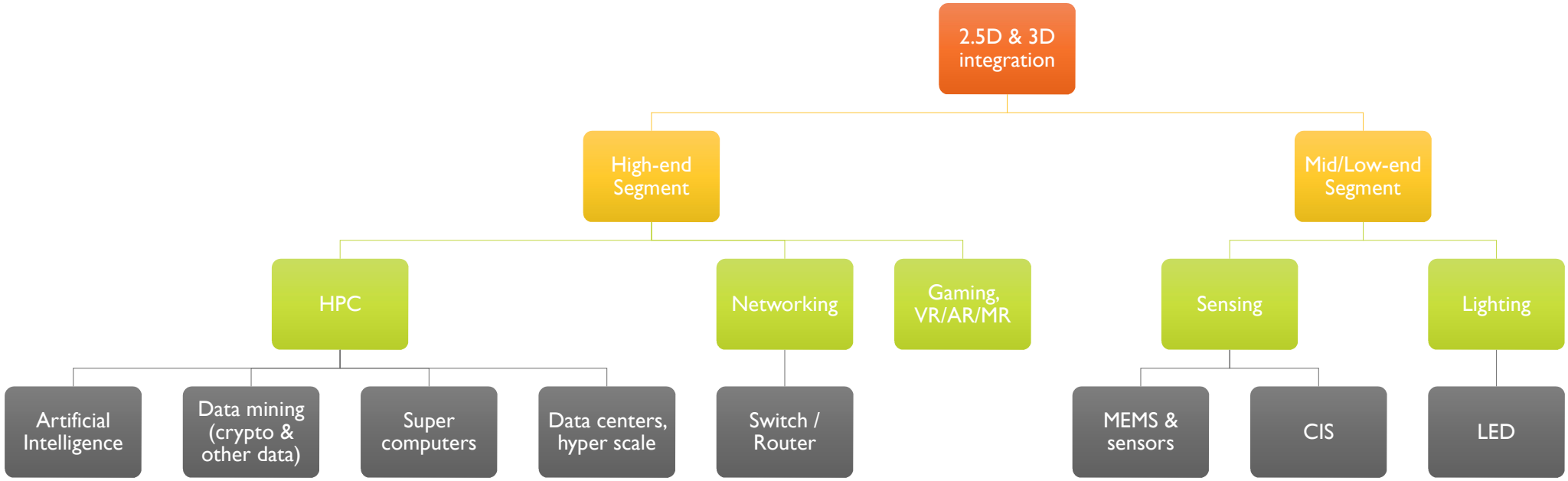
Coupled with high-end performance packaging, system-level 3D Interconnect Density (3D ID) trend is not only sustained but accelerates into new highs. Such is the value of High-end performance Packaging.



3D Interconnect Density (3D ID) data adopted from TSMC
Technology Node here refers to front-end node scaling based on the industry expected average value.

HIGH-END PERFORMANCE PACKAGING MARKET SEGMENTATION

The market is divided into High-end & Mid/Low-End Segments



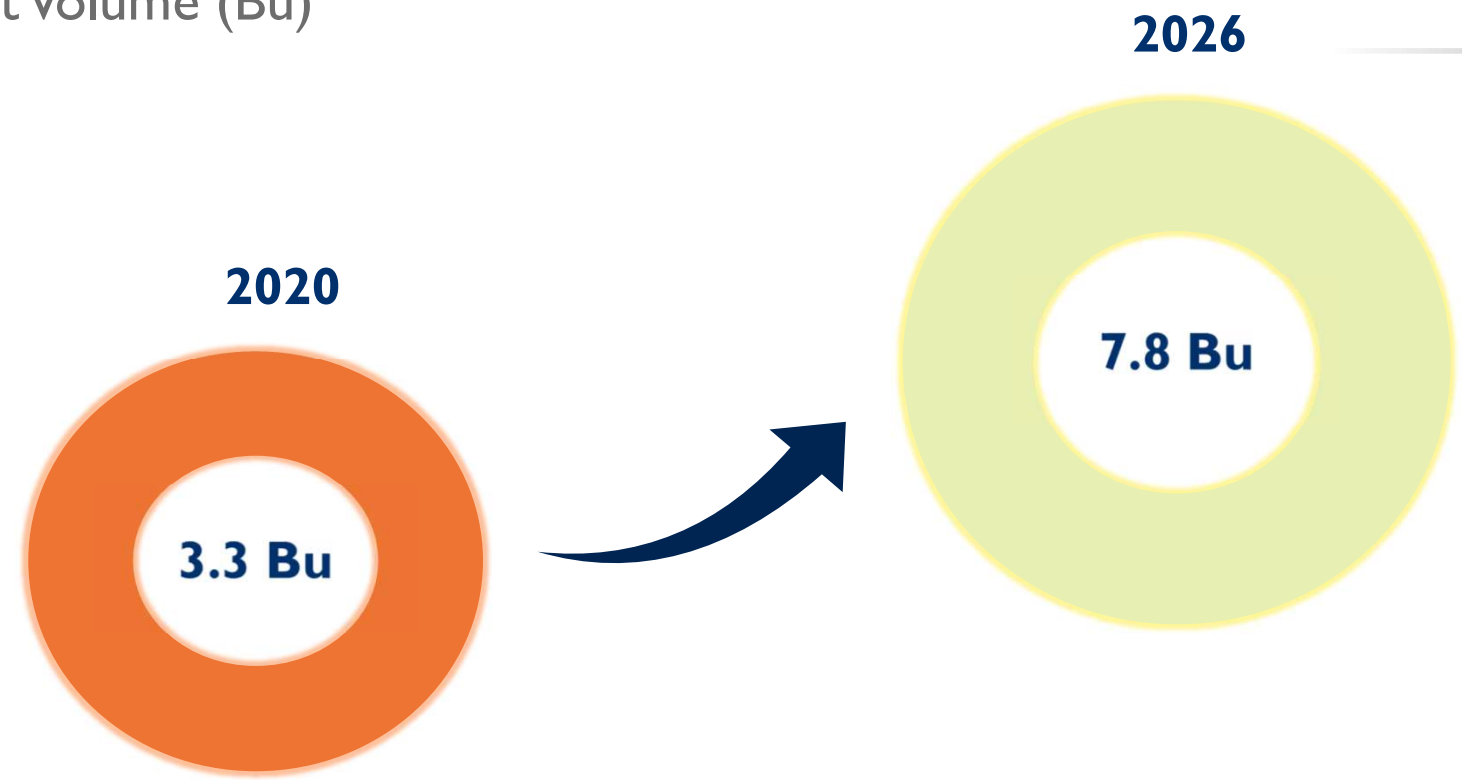
High-end segment is defined as the market where an application is less sensitive to the cost, but requires reduced footprint in addition to high performance & reliability

Mid/Low-end segment is defined by a good balance between cost sensitivity & performance

Growth Trajectory & Forecast for 3D High End Packaging

3D PACKAGE UNIT FORECAST

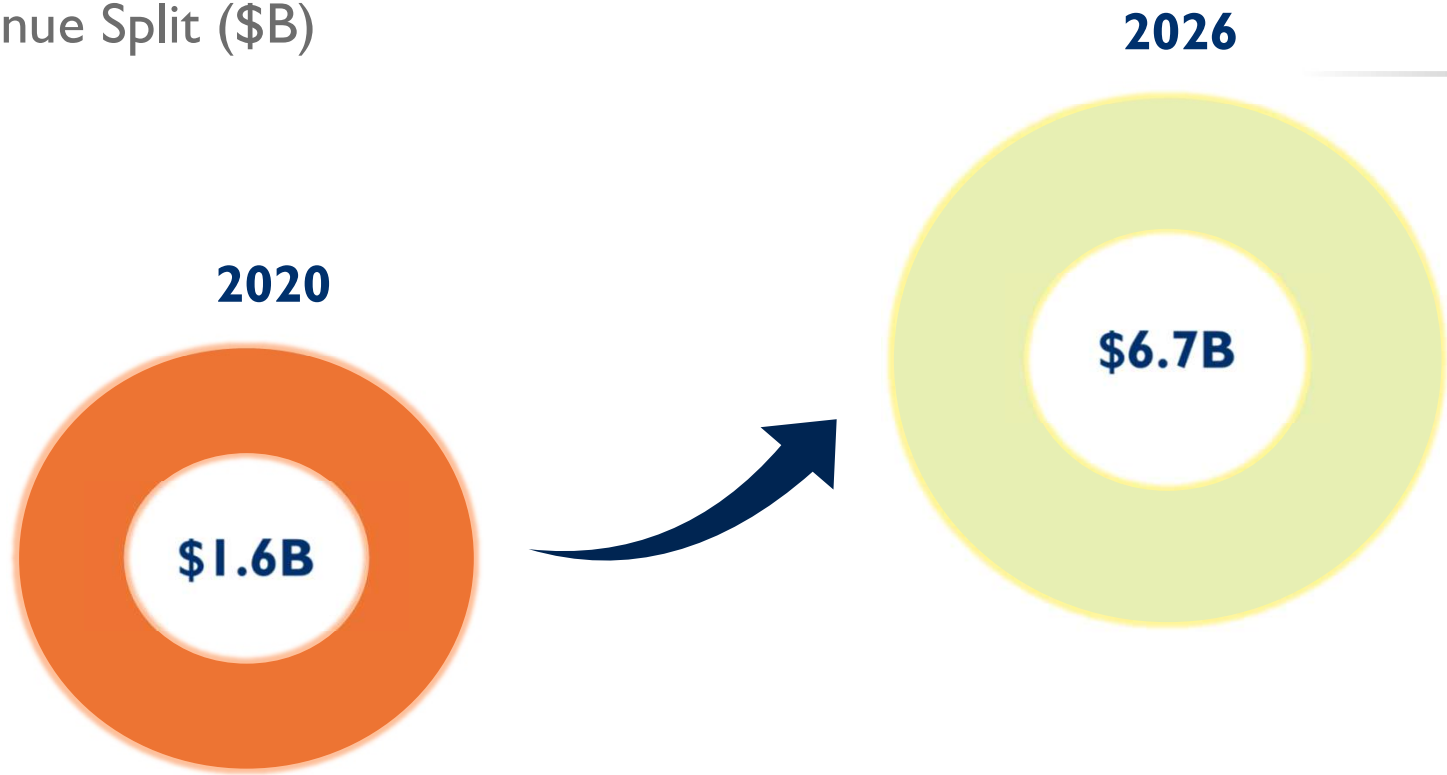
Unit Volume (Bu)



SiP's biggest market is mobile & consumer. This is not surprising, since these markets drove most of the new packages in which footprint reduction and improved performance were key parameters.

3D PACKAGE REVENUE FORECAST

Revenue Split ($B)



3D Stacked packaging revenue will exceed $6B in 2026, with a $CAGR_{2020\text{-}2026}$ of 15%.

Heterogeneous Integration & Beyond with 3D Packaging Form Factors

DIGITAL SOCIETY: NEW TRENDS & MARKET DRIVERS: EVER INCREASING INTERCONNECTEDNESS

- Audio
- Imaging
- Olfactometry
- Motion sensing

Camera

Smart camera

Smart speaker

Companion robot

Robot home

Augmented human

Smart assistant

Speaker

Wearables

Smartwatch

Smart hearables

Smart TV

Smartwatch

SMARTPHONE

Holographic interaction

Smelling

PC

Mobile

SMARTPHONE

SMARTPHONE

PC | Mobile | Smart | Robot | Augmentation

2000 | 2010 | 2020 | >2030

STANDALONE CPU, GPU, MEMORY AND CONNECTIVITY

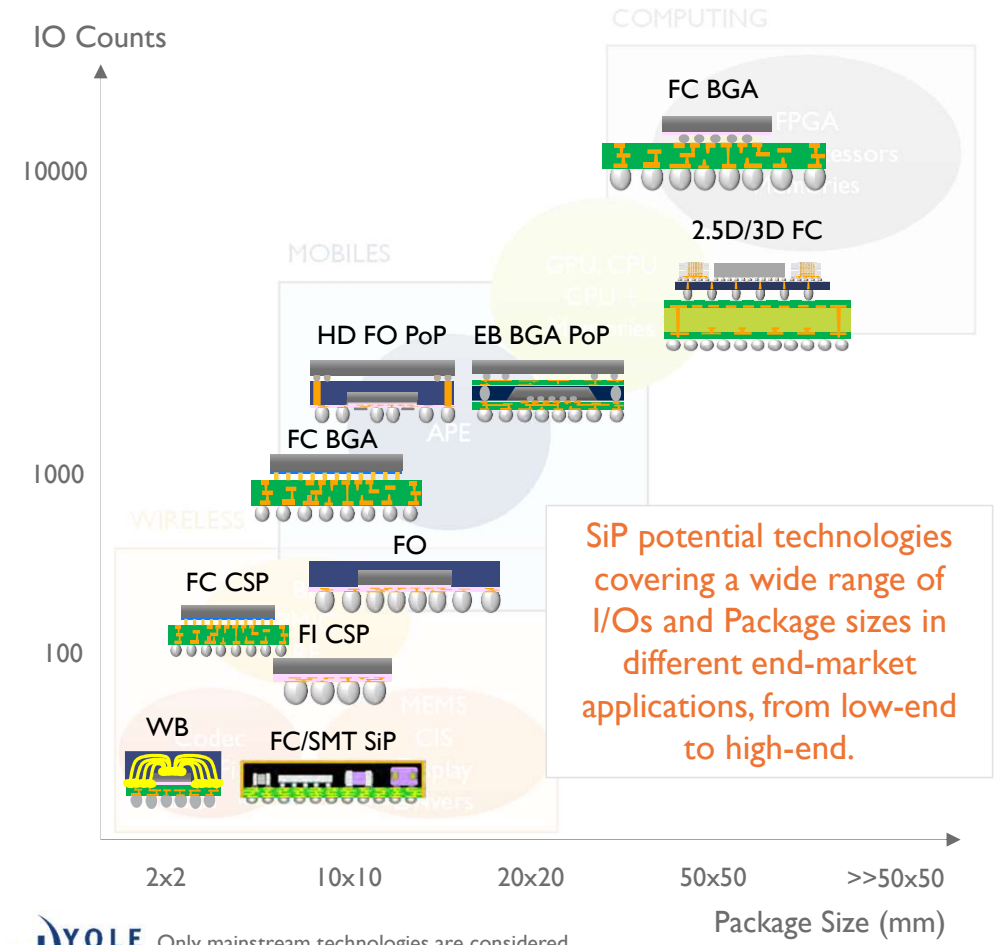
APPLICATION PROCESSOR

+ Accelerator

+ Neuromorphic

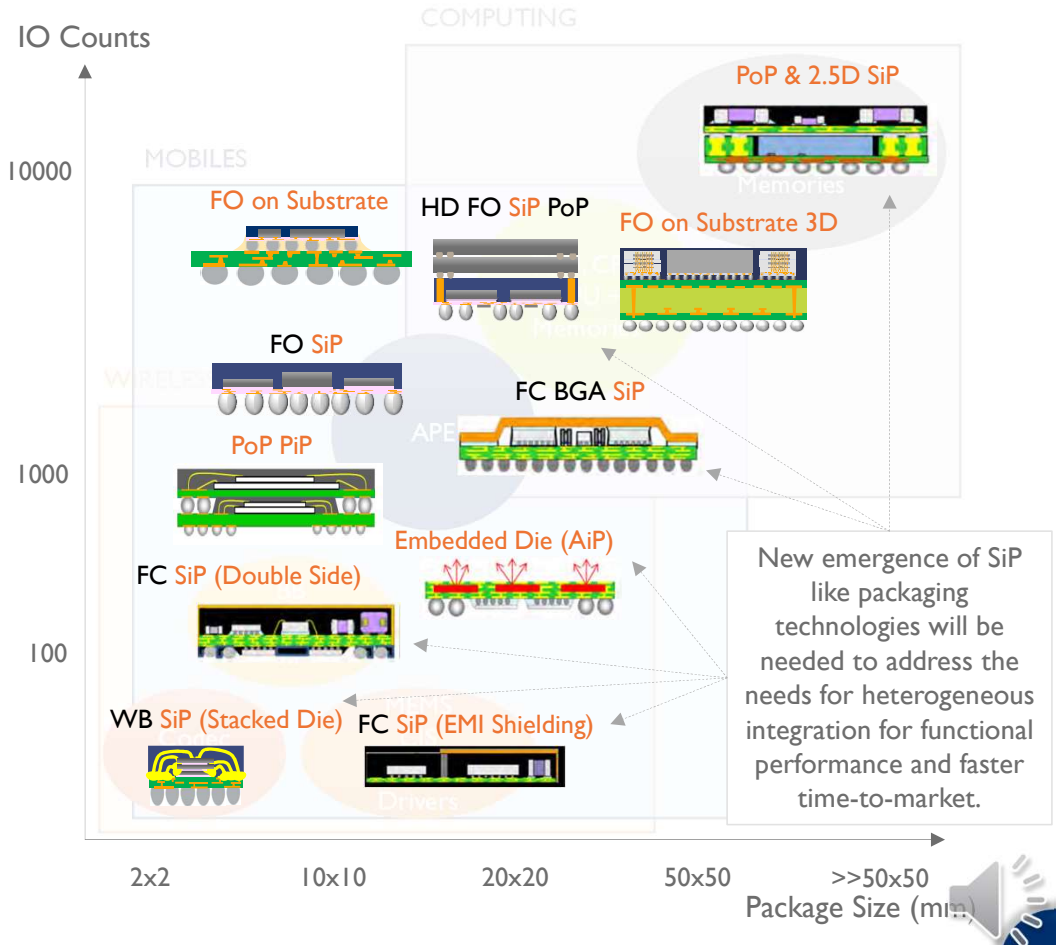
THE OLD AND THE NEW ADVANCED PACKAGING

< 2019 : Packaging Technologies



SiP potential technologies covering a wide range of I/Os and Package sizes in different end-market applications, from low-end to high-end.

2019 - 2030 : New capabilities needed for multi-die solution



New emergence of SiP like packaging technologies will be needed to address the needs for heterogeneous integration for functional performance and faster time-to-market.

YOLE Développement Only mainstream technologies are considered

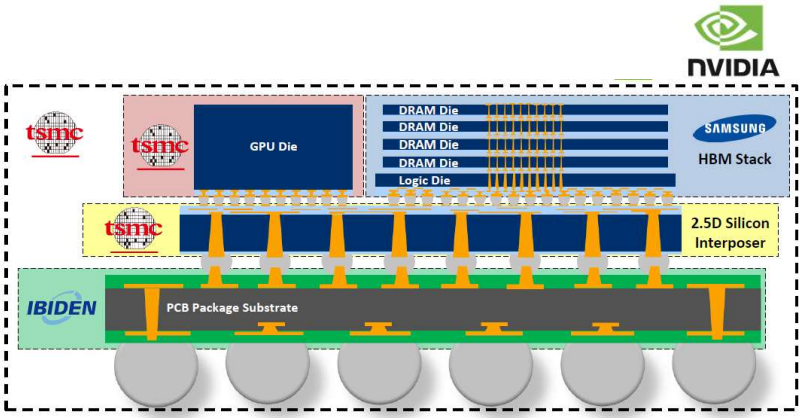
3D Packaging: Key Market Applications

GPU FOR HPC

Supply chain for AMD GPU Radeon Vega Frontier

GPU	HBM2	Interposer	Substrate
TSMC	Samsung	TSMC	Ibiden
Korea 16nm node	Korea	Taiwan	Japan

TSMC Taiwan ➔ CoWoS process



- Nvidia relies on TSMC to manufacture the P100 GPU. TSMC also provides the interposer & assembles the module using their CoWoS process

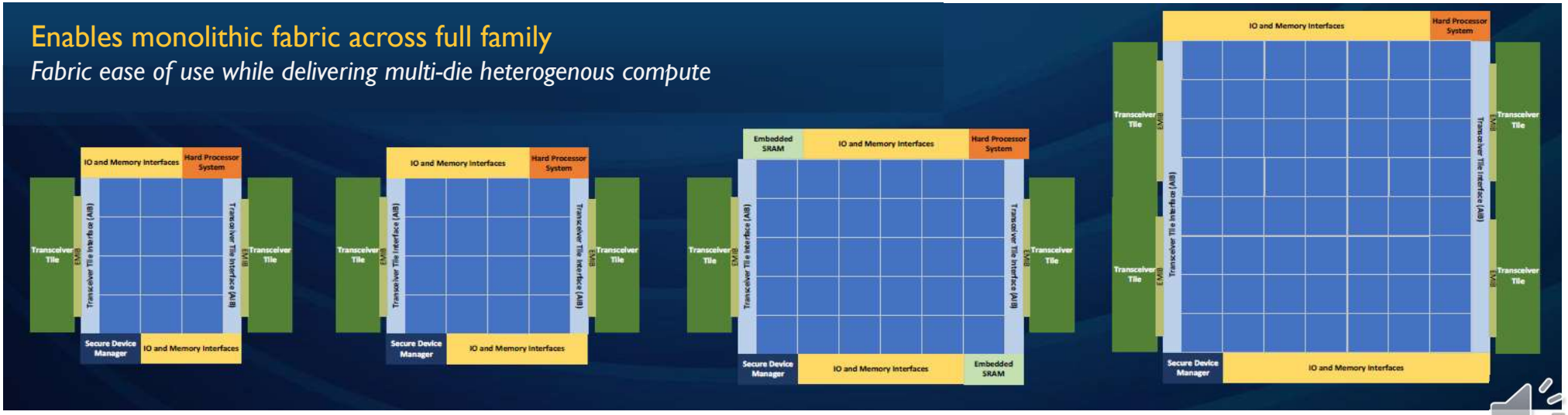
EMBEDDED SI BRDIGE: INTEL

EMIB Technology in Intel® Agilex™

Second-generation EMIB

- High-density interconnect at lower cost compared to Si-interposer
- Flexible chip combination and reuse across different nodes
- Disaggregated transceiver tiles and HBM memory

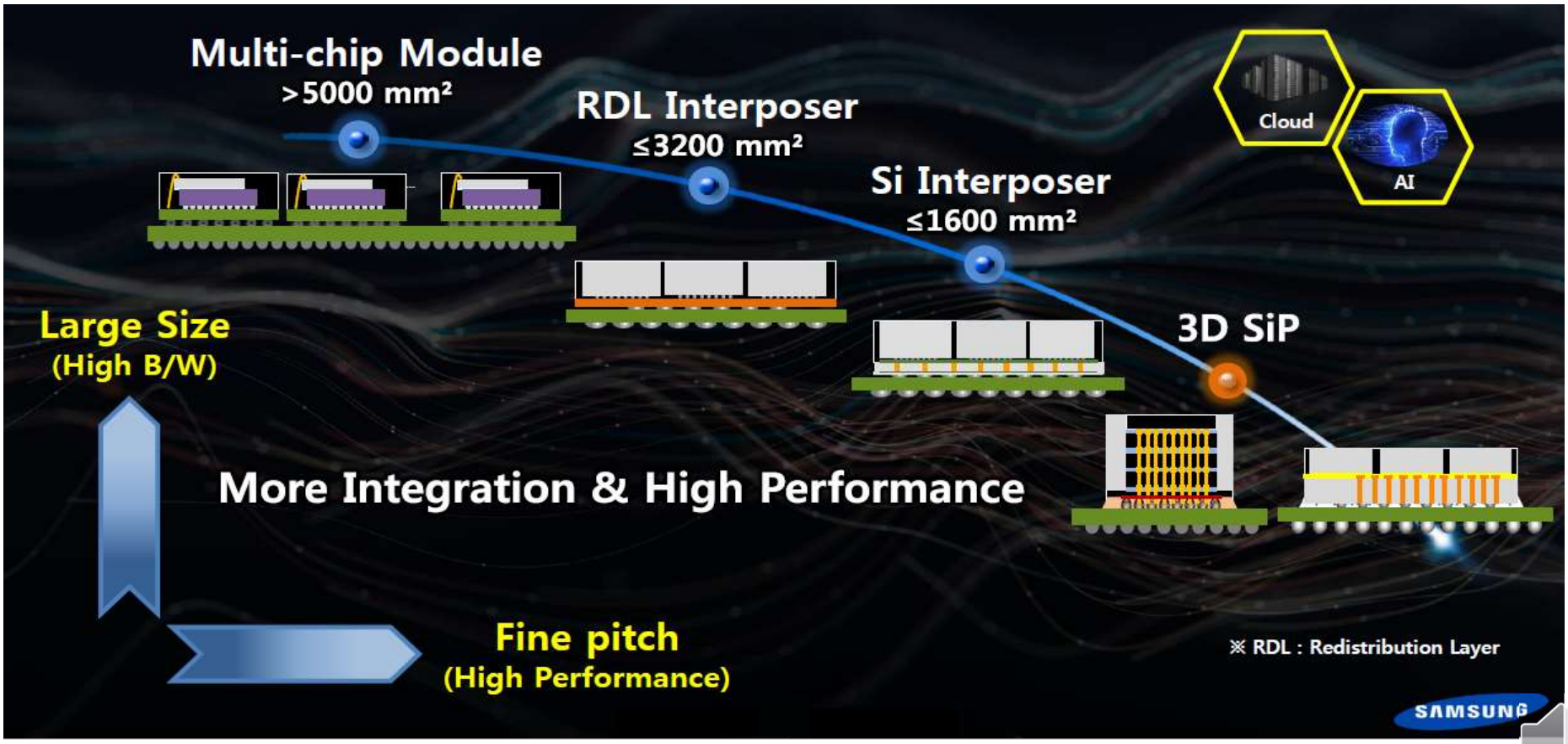
Source: Intel



Source: Intel

SAMSUNG ADVANCED PACKAGING TECHNOLOGY ROADMAP

AI/HPC/Server Platform resolves around High-End Packaging



Source: Samsung Foundry

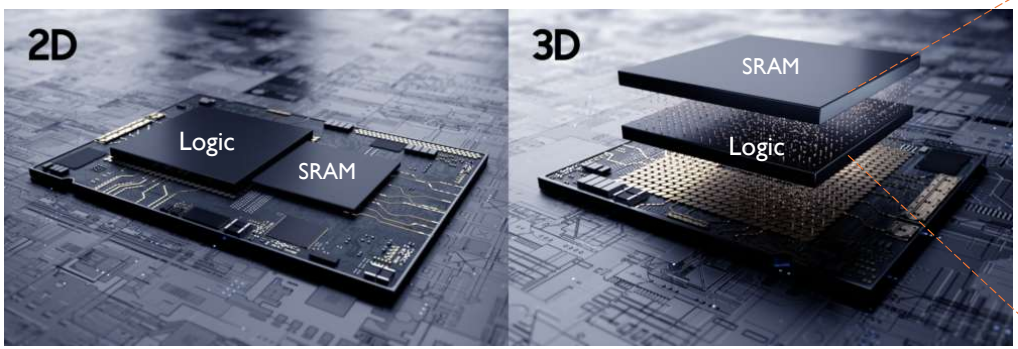
SAMSUNG'S X-CUBE

'X-Cube' is the industry-first 3D SRAM-logic working silicon at 7nm

In 2020, Samsung announces the immediate availability of its Silicon-proven 3D IC Technology, eXtended-Cube (X-Cube), for High-Performance Applications in Mobile, AR/VR, Wearable and HPC devices.

Typical Package
2D (Side by Side)

3D IC Package
3D (Stacked)



Source: Samsung

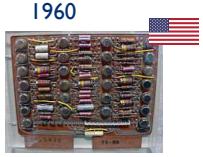
X-Cube

Source: Samsung

The X-Cube is built on 7nm uses TSV technology to stack SRAM on top of a logic die, freeing up space to pack more memory into a smaller footprint. Enabled by 3D TSV integration, the ultra-thin package design features significantly shorter signal paths between the dies for maximized data transfer speed and energy efficiency. Desired specifications of memory bandwidth and density can be scaled vertically.

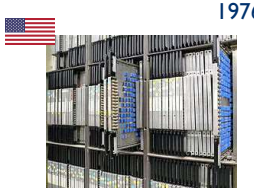
SUPERCOMPUTERS THROUGH HISTORY, RACE FOR SUPREMACY

Livermore Atomic Research Computer
1960



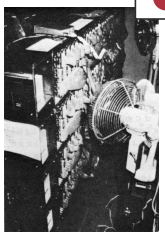
IBM 7030
1961

CDC 6600
3MFLOPS
1964



Illiac IV
200MFLOPS
1970s

Cray-1
250MFLOPS
1976



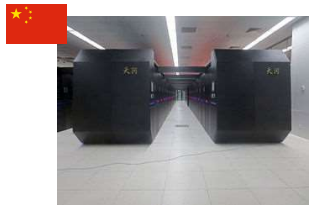
LINKS-1 Computer Graphics System
1.2GFLOPS
1982

Fujitsu's Numerical Wind Tunnel
170GFLOPS
1994

Hitachi SR2201
220GFLOPS
1996

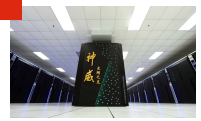
Intel Paragon
140GFLOPS
1992

Nebulae
1.271PFLOPS
2011



Tianhe-2A
101PFLOPS
2013

Summit
200PFLOPS
2018



Sunway Taihulight
105PFLOPS
2016

Transition from Germanium to Silicon transistors

Towards massively parallel computing

Custom ASICs

Use of general-purpose CPU, no more custom chips

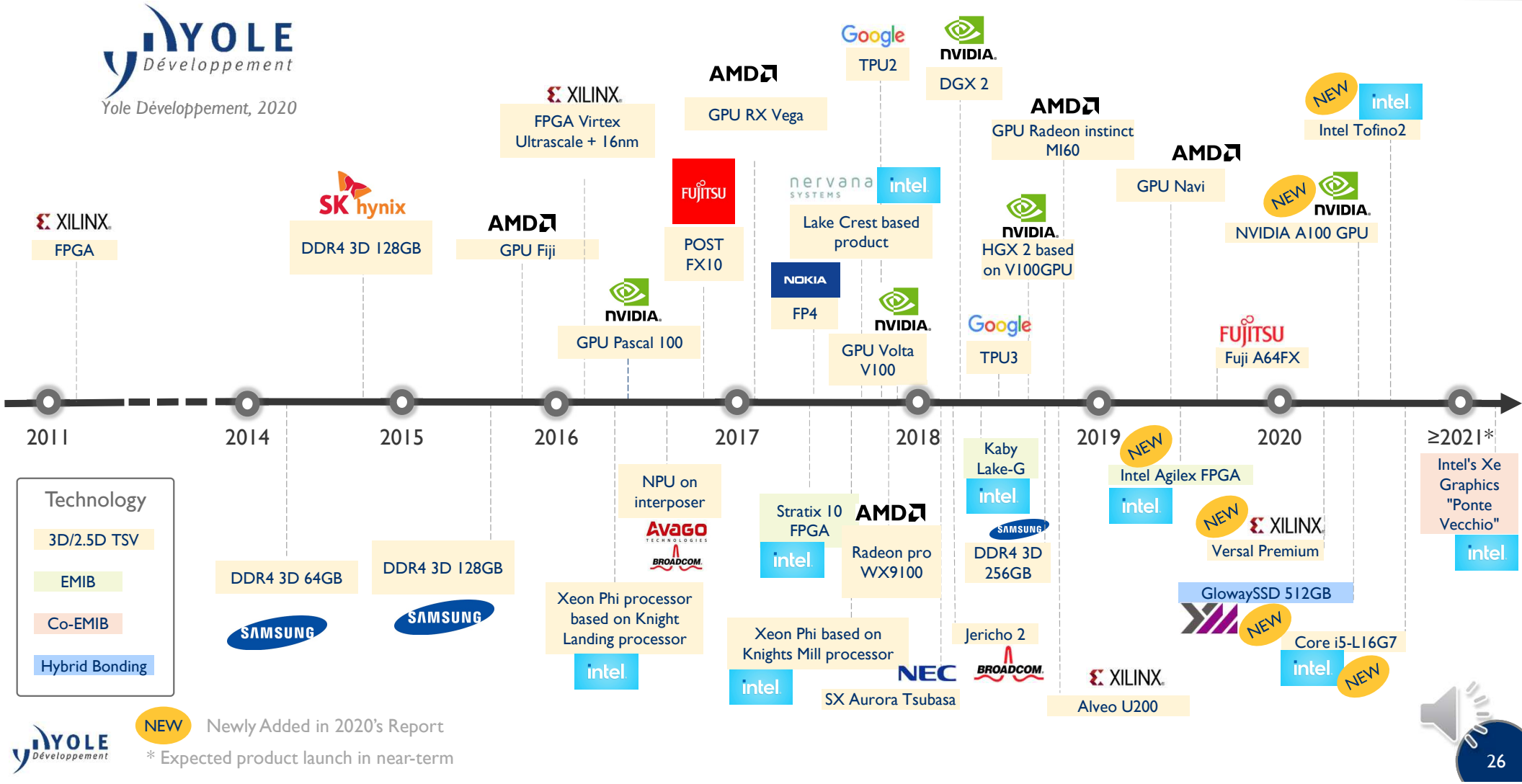
Adding GPU to the mix

Interconnection is key

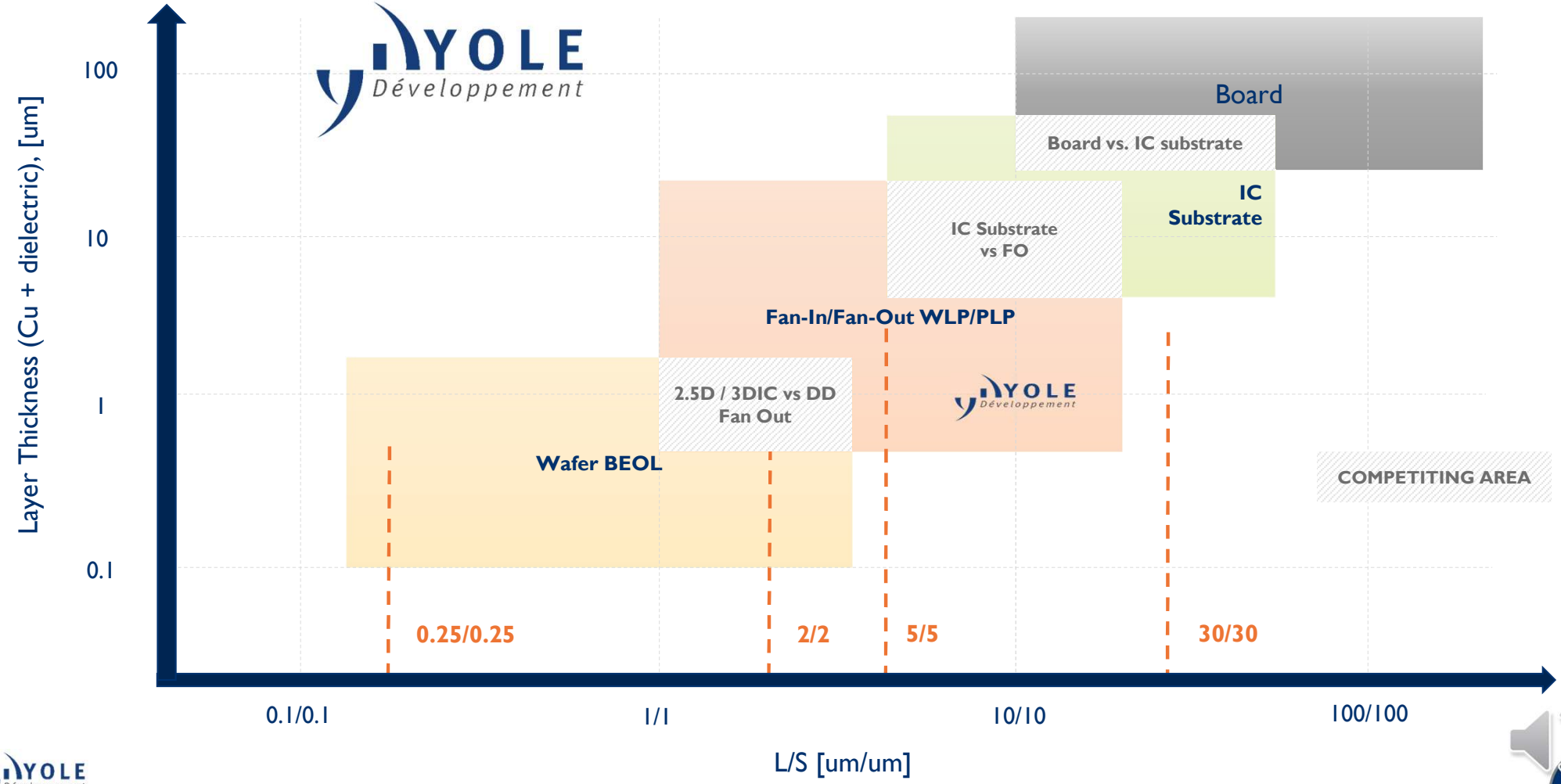
1960 1970 1980 1990 2000 2010 2020

TOP 1 supercomputers through history

HIGH-END COMMERCIAL PRODUCTS LAUNCH: STACKING TECHNOLOGY

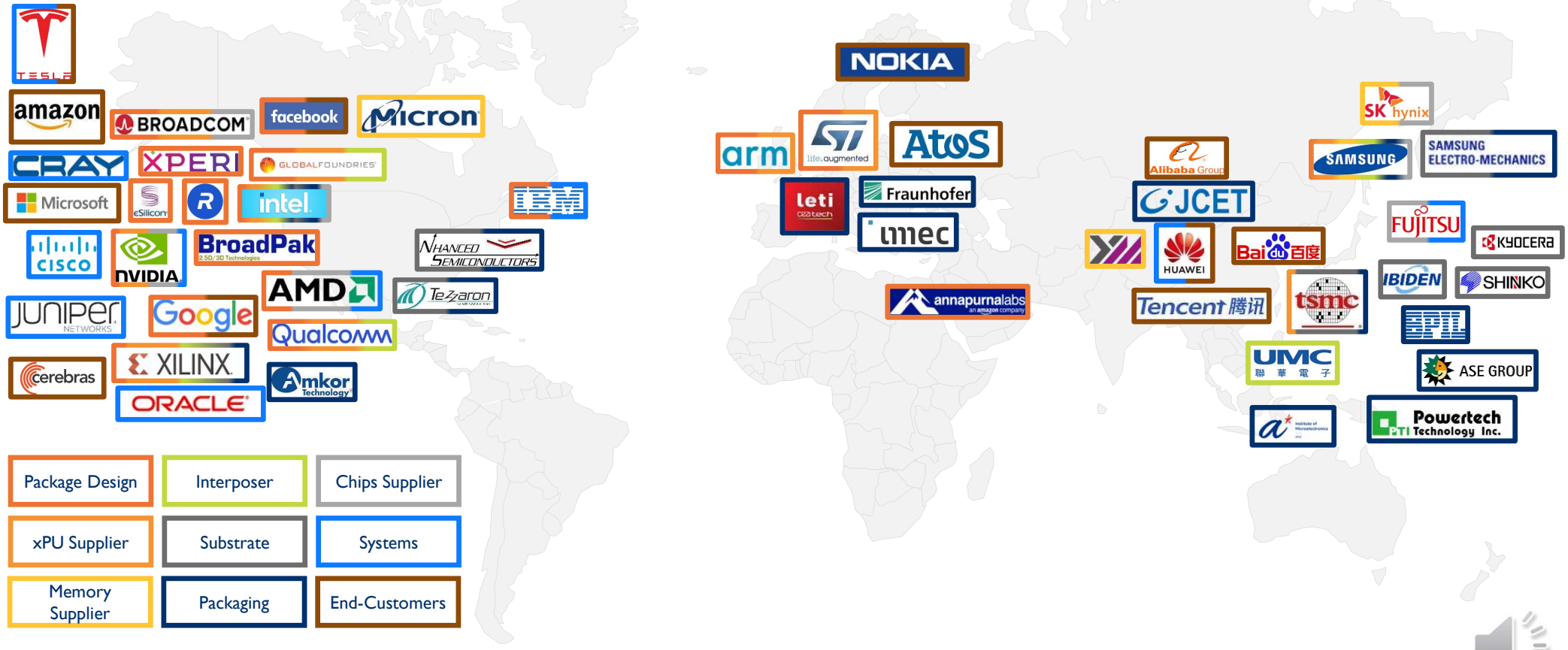


ADVANCED PACKAGING TECHNOLOGY – FUTURE



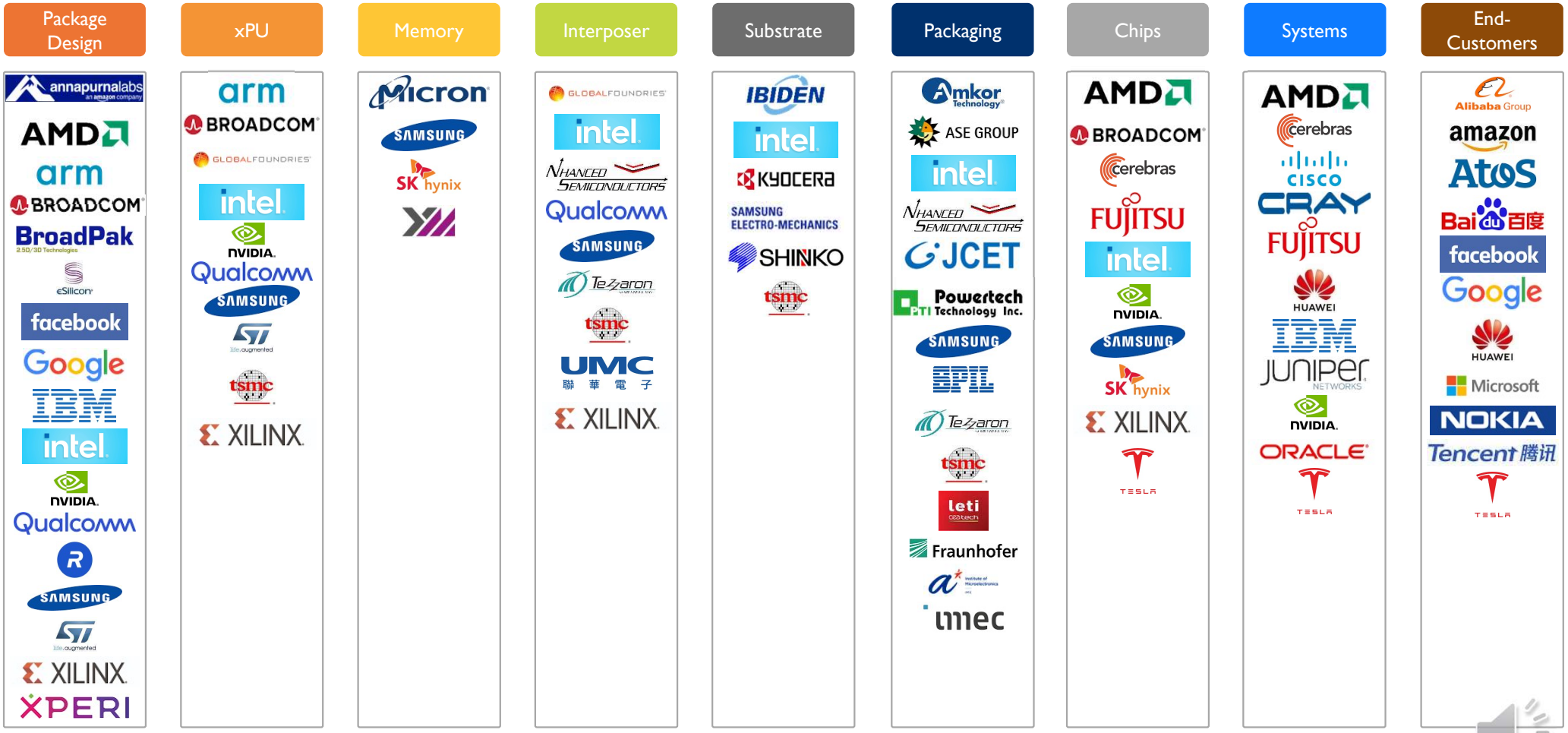
3D Packaging Supply Chain Landscape

GLOBAL MAPPING OF HIGH-END PACKAGING SUPPLY CHAIN (HQ)



YOLE Développement Non-exhaustive List of Players

HIGH-END PACKAGING – FULL SUPPLY CHAIN



YOLE Développement Non-exhaustive List of Players

SYSTEM IN PACKAGE AN IMPERATIVE FOR HETEROGENEOUS INTEGRATION….

Foundry:

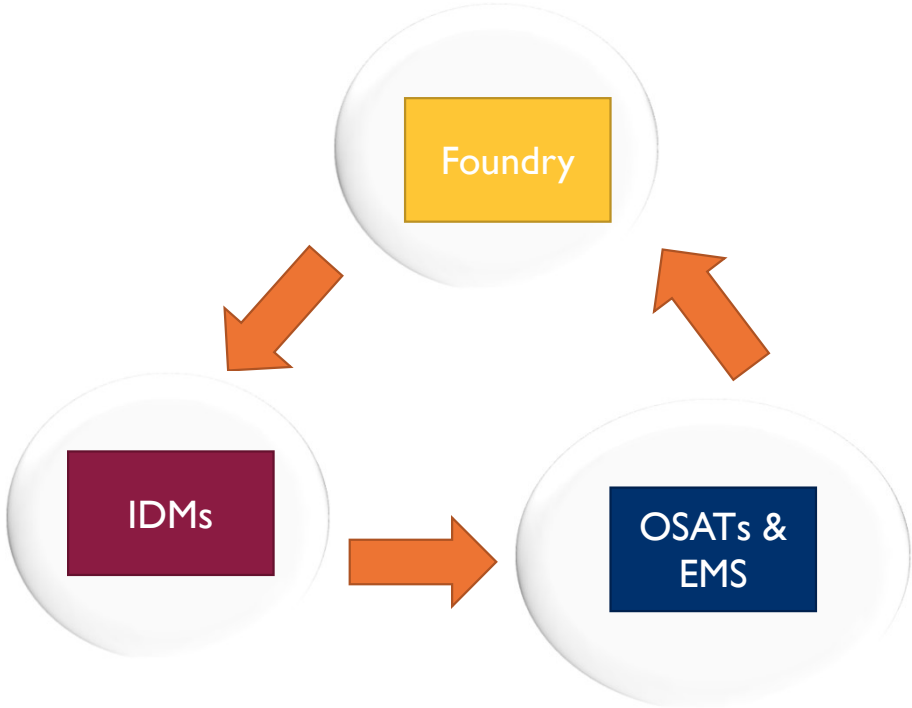
TSMC continues its advanced packaging services with proliferation of InFO based packages and developing SoIC /SoW packaging Technologies

IDMs:

Intel plans to use hybrid packaging technology to bridge the performance gap as it delays 7 nm launch until 2022.

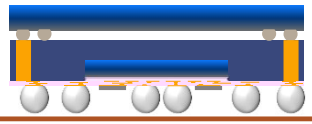
OSATs & EMS Houses:

OSATs such as ASE, Amkor, and JCET are producing highest number of SiP packages for mobile/consumer arena as ASE continues to solidify its USI/EMS business moving forward.



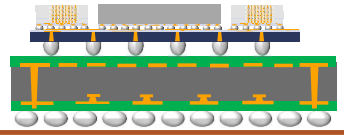
3D PACKAGING COMES IN MANY FLAVORS…..

FAN-OUT PACKAGE



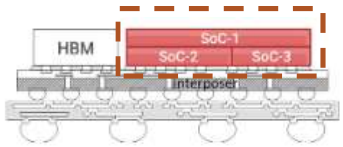
Fan out packaging continues to gain momentum and creates a niche market especially through InFO, InFO-OS, InFO-AiP applications for 5G in addition to multi-die SiP form factors

3D TSV/INTERPOSER



2.5D/3D packaging remains a niche technology for HBM solutions providing increased bandwidth for HPC and GPU applications

SOIC / CHIPLETS



SoIC (System on Integrated chips) is a chiplet based platform for next generation as Moore's law and Si scaling slows down – provides pathway to heterogeneous integration with high bandwidth and scalability

Leading Packaging Form Factors

Dual-Sided SiPs

Double sided SiPs with conformal and compartmental shieldings are providing the next 5G RF packaging solutions with increased number of components for Mobile/Consumer form factors

Summary & Conclusion

SUMMARY & CONCLUSION

- 3D Packaging Motivation
  - An Imperative for heterogeneous integration
  - Supply chain gearing up as TSMC/Intel and others explore stacked die to die interconnected SoC
  - Hybrid bonding infrastructure is slowly taking shape to enable the 3D Integration

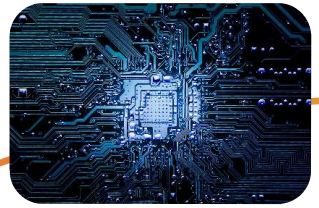
- Market Forecast
  - 3D stacked market expected to grow ~14%
  - HBM & CIS to dominate stacked packaging portfollio

- What to watch out for in next 5 years? Where are we going?
  - Adoption in High-End Server/Datacenter Application
  - Slow penetration into mid-end / high end consumer application showing technology evolution and maturity

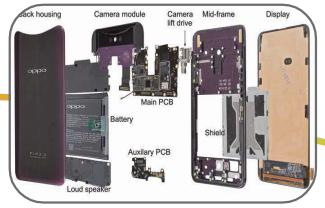
MONITORS AND TRACKS COMBINATION

From module technical content to market forecast and market shares

Advanced Packaging Quarterly Market Monitor
Packaging Service



Consumer
Smartphones, Smart Homes, Wearables



DRAM & NAND Quarterly Market Monitor
Memory Service

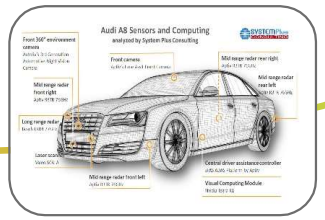
Market Monitors
by Yole Développement

› Market shares evaluation
› Market and technology forecasts

Teardown Tracks
by System Plus Consulting

› Design win identification
› Technology assessment

Application Processor Quarterly Market Monitor
Computing Service



Automotive
ADAS, Infotainment, Connectivity

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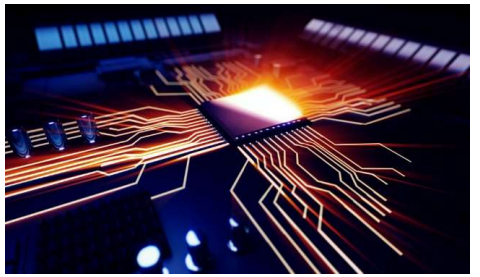
Fan-Out Packaging Technologies and Market 2020

Status of the Advanced Packaging Industry 2019

2020 update available end of July 2020



Equipment and Materials for Fan-Out Packaging 2019

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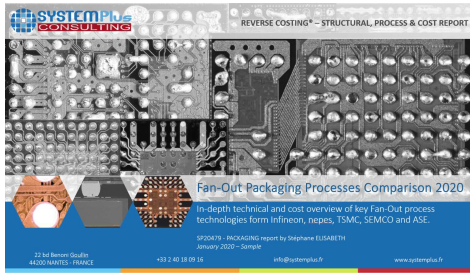
Mediatek Autus R10 (MT2706) 77/79 GHz eWLB/AiP Radar Chipset

Fan-Out Packaging Processes Comparison 2020



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We will be more than happy to give you updated data and appropriate formats.

Your contact: Sandrine Leroy, Public Relations Director – Email: sandrine.leroy@yole.fr


From Technologies to Markets
Yole Développement
Who are we?
YOLE Développement
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FIELDS OF EXPERTISE COVERING THE SEMICONDUCTOR INDUSTRY

Photonics & Sensing

- Photonics
- Lighting
- Imaging
- Sensing & Actuating
- Display

Semiconductor, Memory & Computing

- Semiconductor Packaging and Substrates
- Semiconductor Manufacturing
- Memory
- Computing and Software

Power & Wireless

- RF Devices & Technologies
- Compound Semiconductors & Emerging Materials
- Power Electronics
- Batteries & Energy Management

A COMPLETE SET OF PRODUCTS & SERVICES TO ANSWER YOUR NEEDS

YEARLY REPORTS

Insight
- Yearly reports
- Market, technology and strategy analysis
- Supply chain changes analysis
- Reverse costing and reverse engineering

Format
- PDF files with analyses
- Excel files with graphics and data

Topics
- Photonics, Imaging & Sensing
- Lighting & Displays
- Power Electronics & Battery
- Compound Semiconductors
- Semiconductor Manufacturing and Packaging
- Computing & Memory

115+ reports per year

QUARTERLY MONITORS

Insight
- Quarterly updated market data and technology trends in units, value and wafer
- Direct access to the analyst

Format
- Excel files with data
- PDF files with analyses graphs and key facts
- Web access (to be available soon)

Topics
- Advanced Packaging
- Application Processor
- DRAM
- NAND
- Compound Semiconductor
- CMOS Image Sensors
- Smartphones

7 different monitors quarterly updated

WEEKLY TRACKS

Insight
- Teardowns of phones, smart home, wearables and automotive modules and systems
- Bill-of-Materials
- Block diagrams

Format
- Web access
- PDF and Excel files
- High-resolution photos

Topics
- Consumer: Smartphones, smart home, wearables
- Automotive: Infotainment, ADAS, Telematics

175+ teardowns per year

CUSTOM SERVICE

Insight
- Specific and dedicated projects
- Strategic, financial, technical, supply chain, market and other semiconductor-related fields
- Reverse costing and reverse engineering

Format
- PDF files with analyses
- Excel files with graphics and data

Topics
- Photonics, Imaging & Sensing
- Lighting & Displays
- Power Electronics & Battery
- Compound Semiconductors
- Semiconductor Manufacturing and Packaging
- Computing & Memory

190 custom projects per year

PART OF YOLE GROUP OF COMPANIES

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