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Glass Carriers with Matched CTEs for Wafer Thinning Applications

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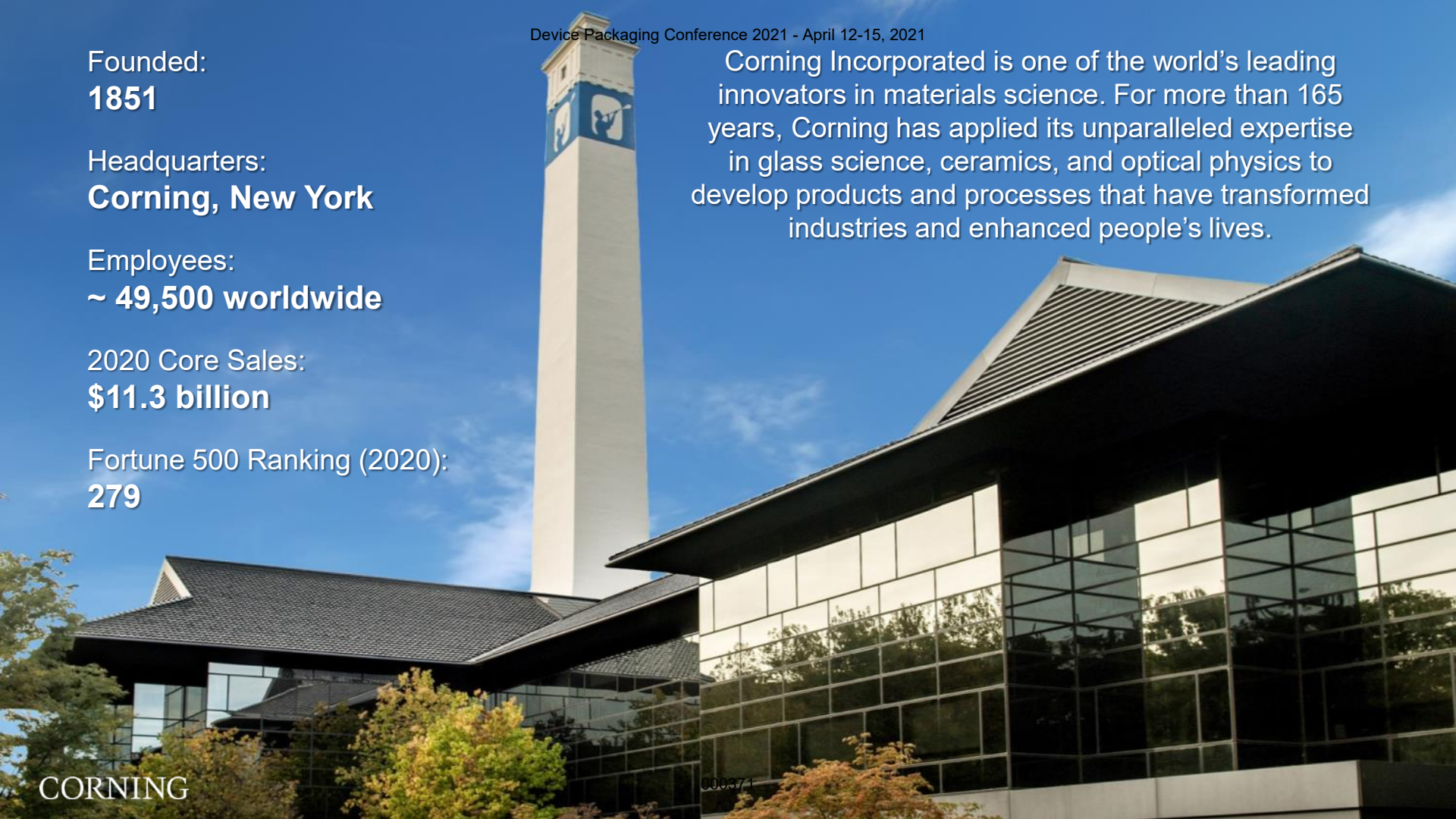

Founded:
1851

Headquarters:
Corning, New York

Employees:
~ 49,500 worldwide

2020 Core Sales:
$11.3 billion

Fortune 500 Ranking (2020):
279

Corning Incorporated is one of the world's leading innovators in materials science. For more than 165 years, Corning has applied its unparalleled expertise in glass science, ceramics, and optical physics to develop products and processes that have transformed industries and enhanced people's lives.

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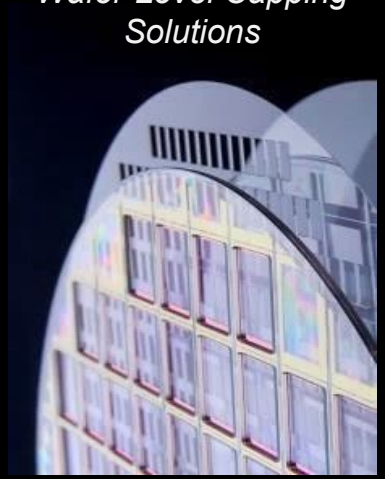
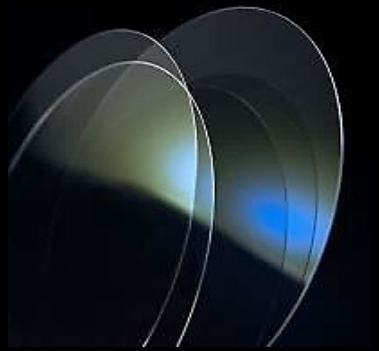
Corning Precision Glass Solutions offers industry leading wafer and panel format glass-based solutions.

Our products help customers deliver increasingly demanding functionality and form factor requirements in consumer devices and Internet of Things (IoT) applications.

Wafer-Level Capping Solutions



Wafer-Level Optic Solutions

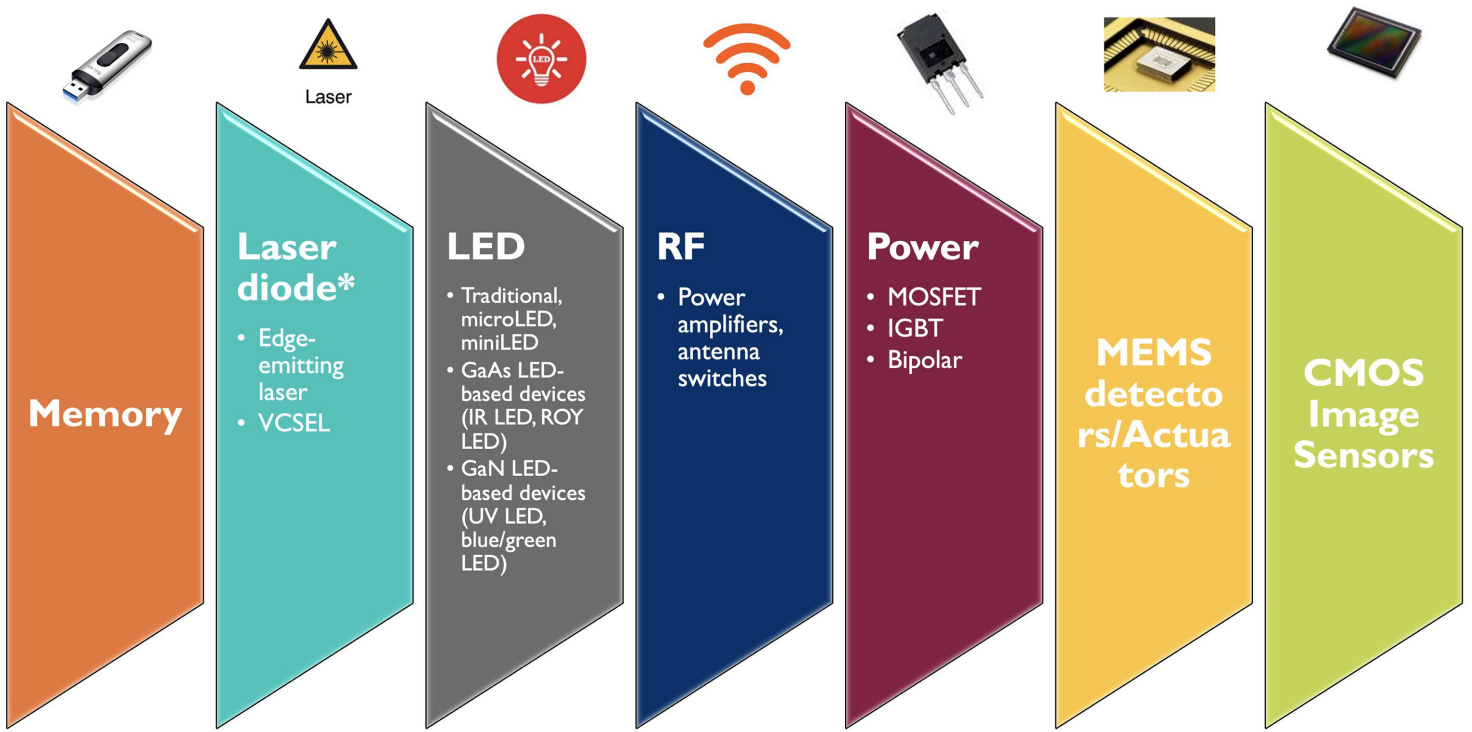


Augmented Reality Solutions

Carrier Solutions

Custom Glass Solutions

There are a Variety of Applications that Require Wafer Thinning Processes



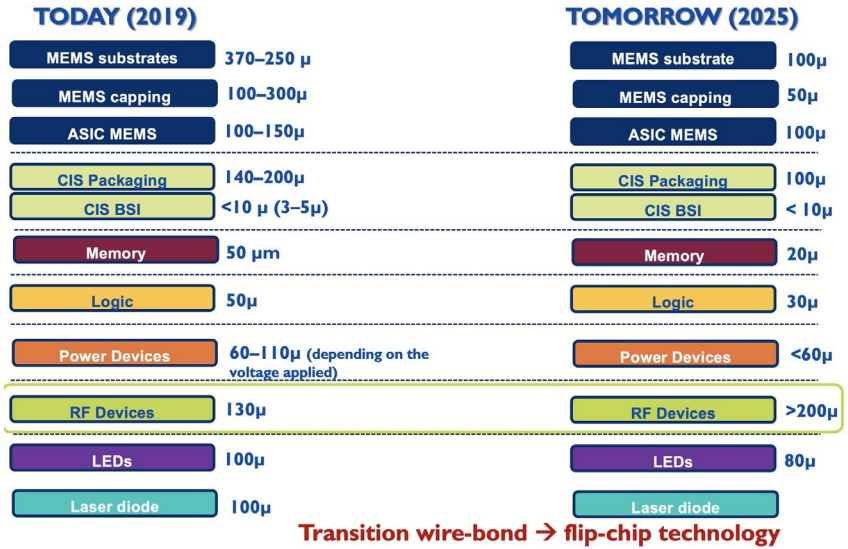
Source: Yole Development

Semiconductor Wafer size and Thickness Trends are Driving Emerging Applications

Semiconductor wafer availability and trend

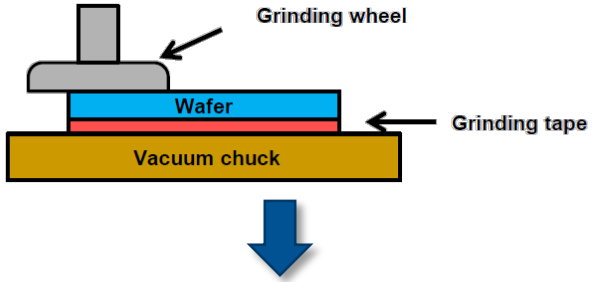
Wafer Diameter		100mm 4”	150mm 6”	200mm 8”	300mm 12”
Wafer thickness	Silicon	525 µm	675 µm	725 µm	775 µm
	SiC		350 µm →		
	GaAs	625 µm ± 25 µm	675 µm ± 25 µm →		
	Sapphire		675 µm ± 25 µm →		

Industry trends for wafer thinning based on application

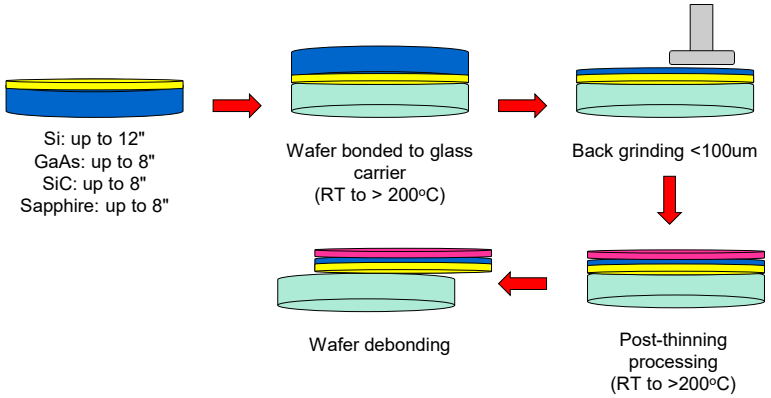


Source: Yole Development

Wafer Thinning Process and Challenges



Typical Wafer Thinning and Processing Flow



Wafer Thinning Challenges

- Grinding damage
- Wafer breakage
- Edge chipping
- Wafer warpage → Post thinning processes
- General handling

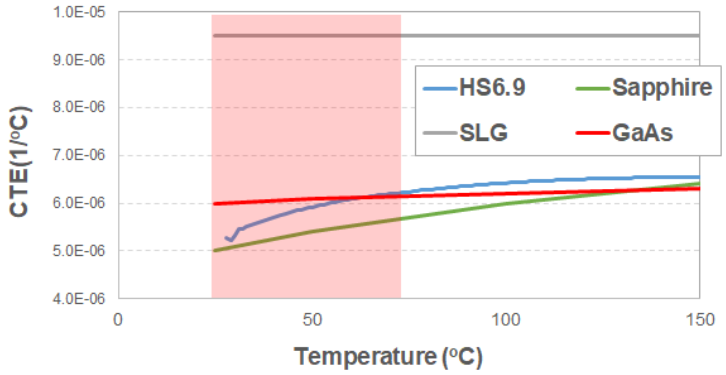
When wafers are thinned to <<100 um or require post-thinning processing, **glass carrier** is a preferred choice

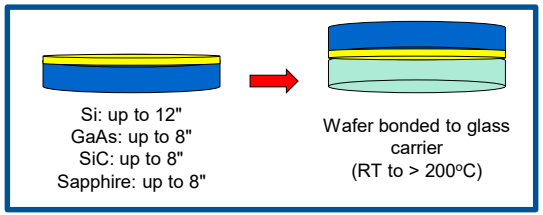
Wafer Warp During Bonding Process

Δ CTE of glass substrate, device wafer and adhesive: modeling & experimental data

Minimizing Δ CTE between carrier substrate and wafer at processing temperature is important

Glass CTE is not a constant value.
It changes as a function of temperature.

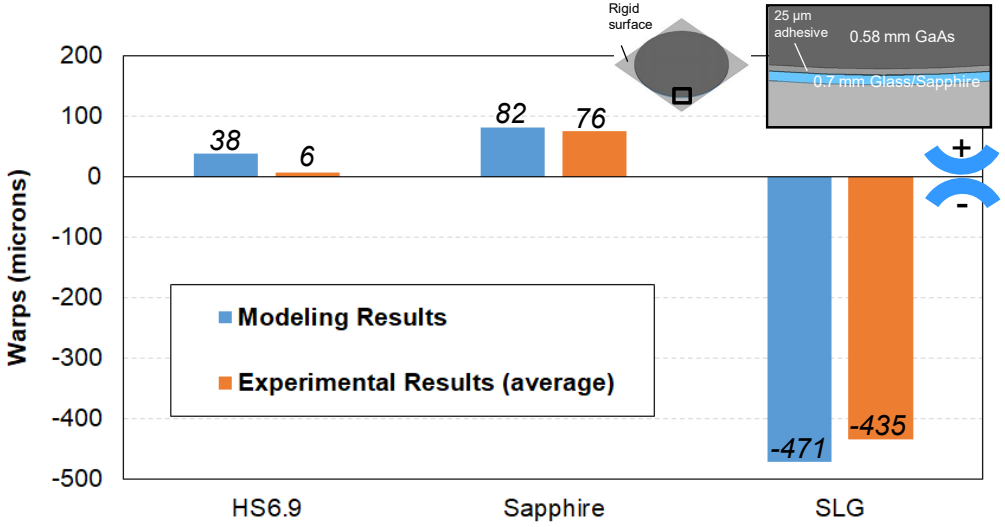




In-process warp of bonded GaAs wafers: Modeling and experimental data

Modelling assumption:

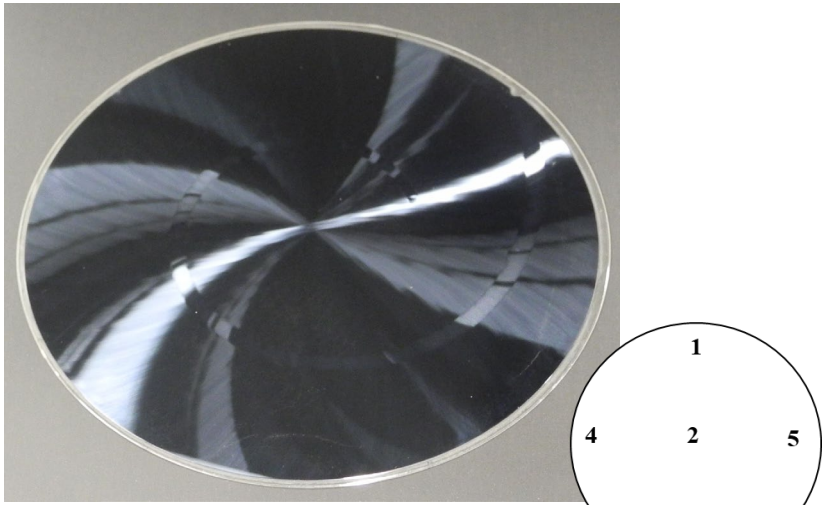
- high temperature GaAs wafer bonding with different substrate
- Substrate thickness 0.7mm and adhesive thickness 25um
- Intial GaAs wafer thickness 580µm
- Wafer diameter 150mm (6")
- Stress-free temp: 70°C (adhesive Tg)



Bonded Wafer after Back Grinding

HS6.9 successfully support wafer thinning: experimental result

Bonded GaAs on HS6.9 after back grinding



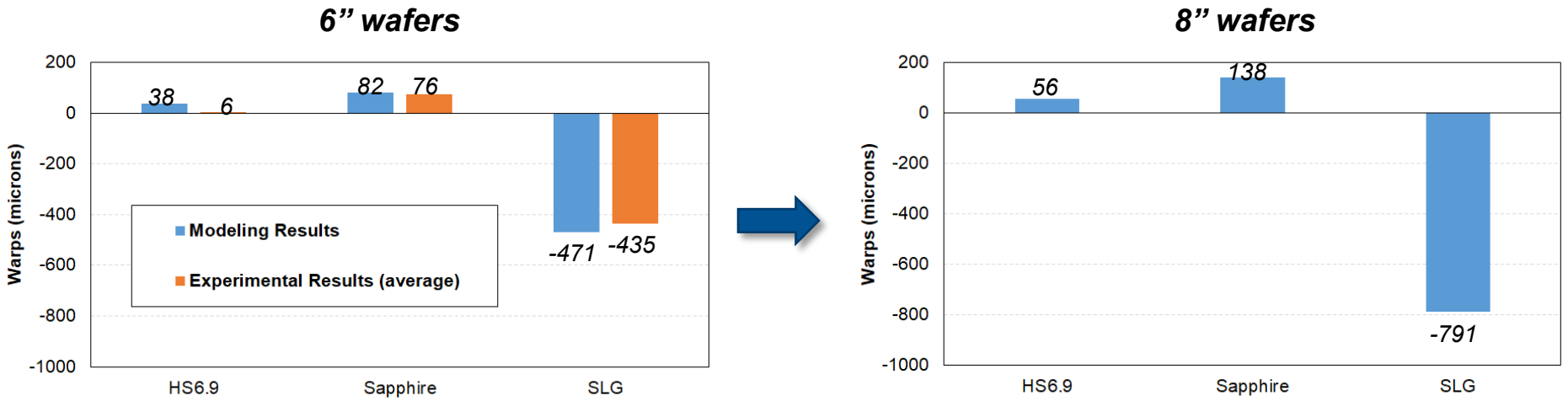
Carrier		Org.	Final Thickness (um) (Measurement points)						
Material	Thickness (um)	thickness	1	2	3	4	5	Ave	TTV
HS6.9	700	1383	824.8	825.3	824.9	824.7	825.0	824.9	0.6

- *Corning HS6.9 showed no process damage during thinning process*
- Bonded GaAs wafer was ground to ~125µm using Disco DAG810 automatic surface grinder

Wafer Warp During Bonding Process

In-process warp becomes bigger issue as device size increases from 6” to 8”

In-process warp of bonded GaAs wafers: Effect of substrate diameter



Modelling assumption:

- high temperature GaAs wafer bonding with different substrate
- Substrate thickness 0.7mm and adhesive thickness 25um
- Intial GaAs wafer thickness 580μm
- Wafer diameters 6” (150mm) and 8” (200mm)
- Stress-free temp: 70°C (adhesive Tg)

Glass Substrate is the Material of Choice

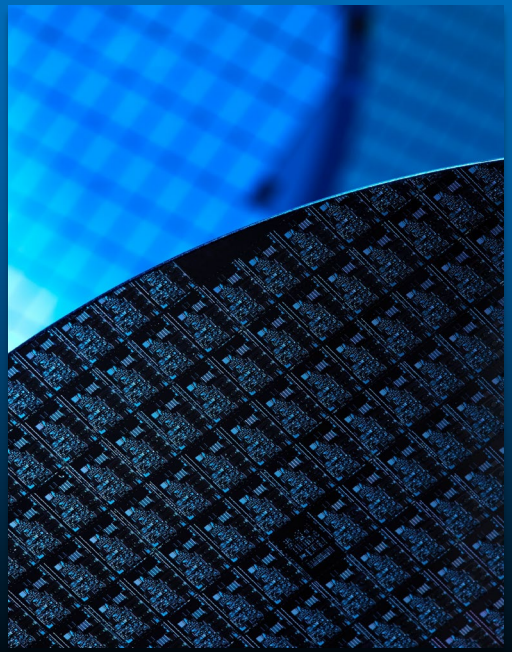
Inherent properties of glass mitigates industry challenges in wafer thinning

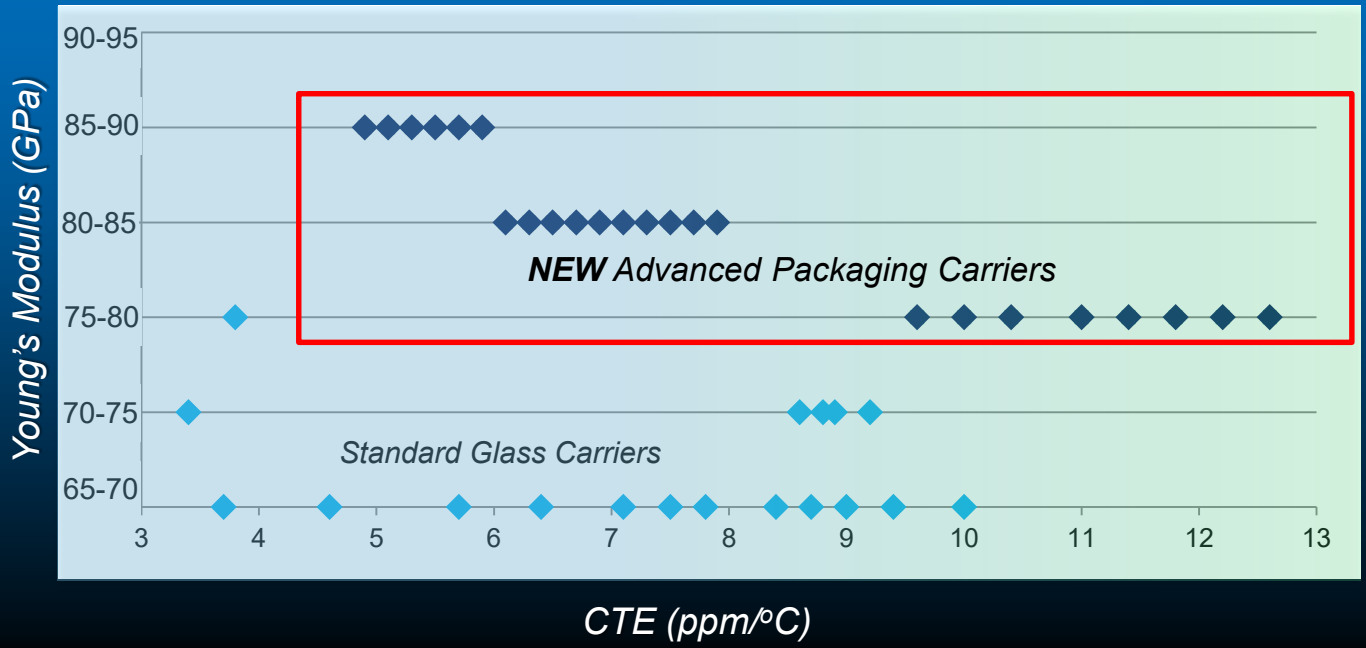
Properties of Glass	Benefits of Wafer Thinning
Range of CTEs in fine granularity	↓ ΔCTE → ↓warp
Optical transparency	Enables light based bonding/debonding
Flatness & smoothness	Enables thinner device wafer <<50 µm
High stiffness	↓warp
Size of glass substrates	↓cost + ↓handling damage
Variety of thicknesses	↓warp + ↓handling damage
Manufacturing scalability	Enables R&D + ↓ cost

Corning Carrier Solutions

Ideally suited for wafer thinning applications

Corning has tailored its glass carriers by Young's Modulus, CTE, and freedom of wafer thickness to enable wafer thinning industry challenges





Corning Advanced Packaging Carriers (APC)

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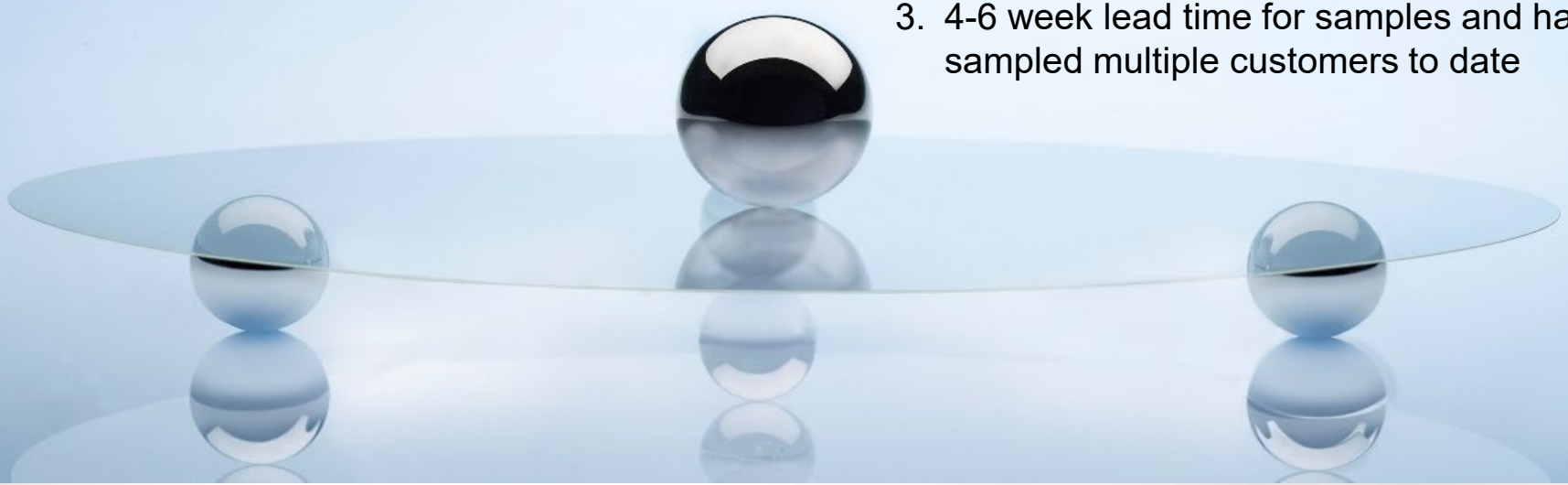
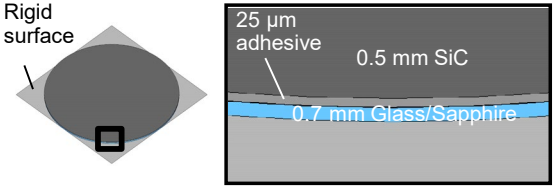
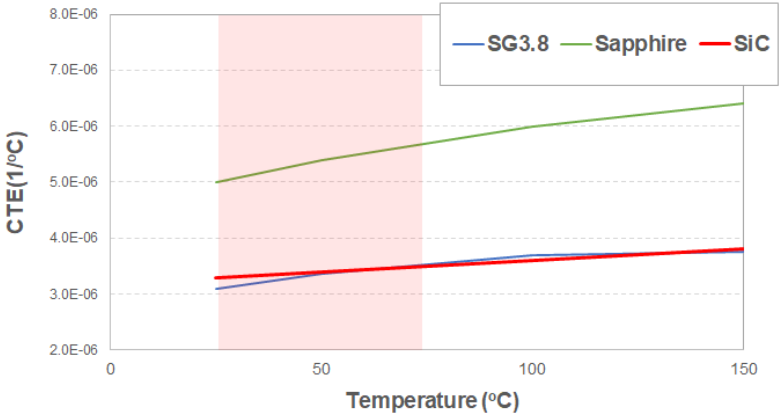
1. Fine granularity of CTE's-minimize Δ CTE
2. High Stiffness: Increased YM & optimized thickness
3. 4-6 week lead time for samples and have sampled multiple customers to date

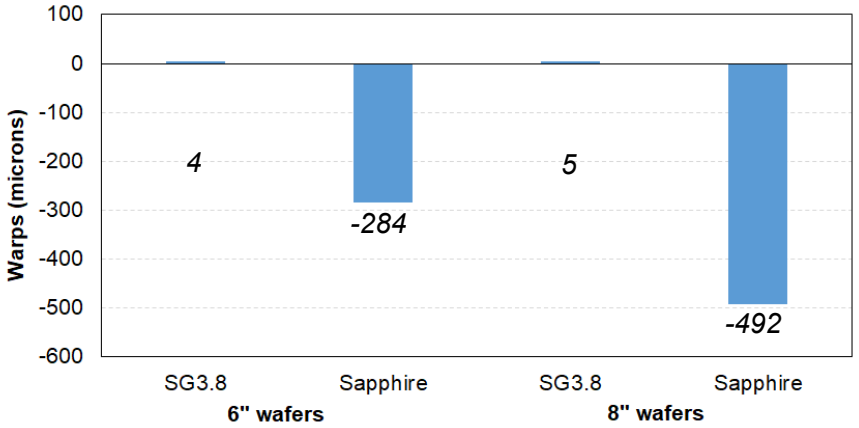


Wafer Bow During Thinning and Post Processing

Corning APC can address a very wide range of market needs







Modelled warps of bonded SiC wafers at 6” and 8” diameter; Stress-free temp: 70°C (adhesive Tg)

Summary

- Wafer thinning is the industry trend due to 1) miniaturization, 2) better thermal management and 3) higher device performance
- CTE matching between device wafer and carrier at the processing temperature is imperative to minimize warp
- Glass can support CTE matching for any known wafer material
- Glass is the material of choice for growing device wafer form factor
- Corning is ready to support wafer thinning industry from R&D to high volume manufacturing

Acknowledgement

- ITRI in Taiwan for providing temporary bonding service
- Disco in Japan for back-grinding service
- MK Cornfield and Brooke Sinko of Corning for editorial assistance

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Thank You

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