Flexibility of System Technology Co-Optimization (STCO) demands a Shift Left process and methodology.

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17TH INTERNATIONAL CONFERENCE ON • APRIL 12-15, 2021
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Who's that guy?

My name is Per Viklund

I have been in the electronic industry in different positions for over 40 years and have been in the EDA industry mainly working with IC Packaging since the late 1980-ies

I am Director of Systems Architecture with Siemens EDA* since 2003

Responsible for our IC Packaging and RF/Microwave design solutions

*) Former "Mentor Graphics Corp."

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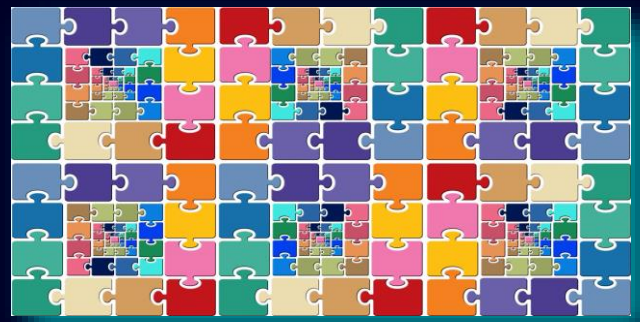
Introduction

WHAT is STCO?

- It's methodology!
- **Methodology to disaggregate complex SoC into smaller partitions**
  - That can be designed asynchronously
  - That can be designed concurrently
  - **That can be individually processed with for each, optimal process**

…and put back together again through 2.5/3D IC Packaging



Introduction

WHY STCO?

- Very interesting question and there are indeed many benefits

…..but it is beyond the scope of this presentation

Introduction

If THAT is STCO, what have we been doing this far?

- DTCO: Design Technology Co Optimization
- From DEVICE scaling
- To SYSTEM scaling

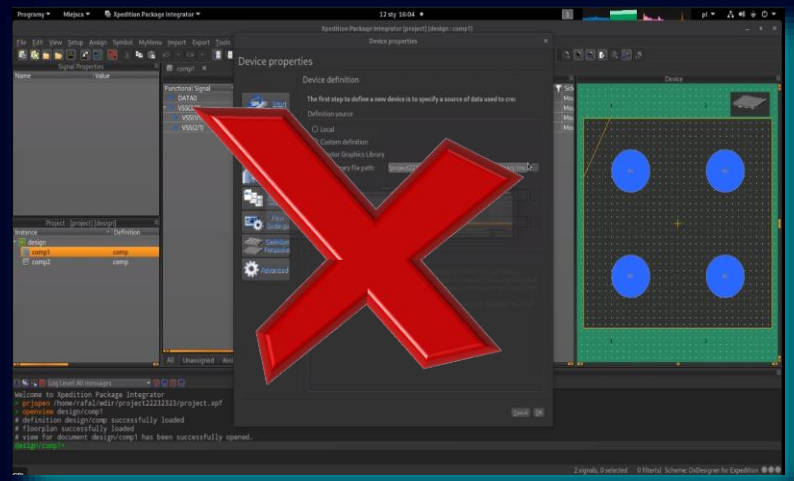
- From DEVICE Packaging
- To SYSTEM Packaging

A transition from **DTCO** to **STCO**

Introduction

Is STCO a tool or product?

- NOT tools from EDA vendor or in house development
- **It's methodology!**
- Both DTCO and STCO are methodologies
- STCO starts at a higher level
  - Focus on:
    Disaggregating a system so the pieces can be built to lower cost and be put together in a way that support high performance.



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Introduction

DTCO and STCO corner stones

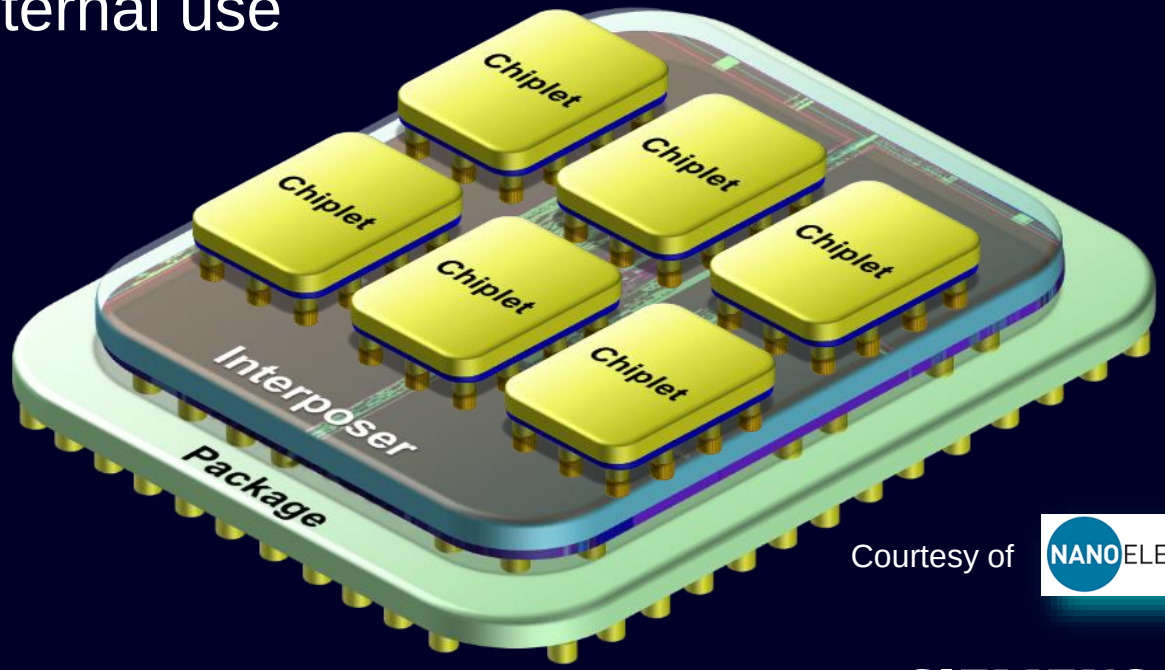
- **Making educated design decisions very early**

- DTCO: Utilize knowledge from both Design and Technology
- STCO: SAME –but include knowledge about the System
- Gain: **P** ^{3} I.e.: **P**erformance, **P**ower and **P**rice (cost)

Introduction

Are Chiplets and STCO the same?

- Not necessarily
- Chiplets are typically off the shelf blocks with a standard interface
- In STCO a module might be for one off internal use and might not have a standard interface
- But can absolutely be a reusable chiplet



Courtesy of NANOELEC.

Early multi physics analysis for STCO

Challenges

- **Working in an asynchronous manner but still concurrent**
- **Bringing together design fractions from multiple teams at some point**

- **This "point" is Package Planning and Prototyping**
  - Put back disaggregated SoC blocks (chiplets)
  - Examine Packaging options

- Partitioning made at system level impact our ability to:
  - Build a working package with desired performance at optimal cost

Early multi physics analysis for STCO

Disaggregation

- Clearly critical to success HOW partitioning is made

- Partitioning is made by teams:
  - That are lacking downstream insight (not by skills but by process)
  - That don’t have the means to consider packaging impact of their decisions

Early multi physics analysis for STCO

Main Challenge to Solve

- **HOW to re-integrate design fractions into**
  - **An early package prototype that**
    - **Has enough information to drive the analysis needed to make efficient partitioning decisions**

- Analysis give us knowledge that we feed back to the silicon team
- Now the silicon team has invaluable information to help reconsider the partitioning

Early multi physics analysis for STCO

Why is partitioning such a challenge?

- We can't just look at logical function blocks
- We must also consider:
  - Performance of each fraction
  - How a fraction communicates with other fractions
  - How to manage power
  - ……

- If I take this block and stack it 3D on top of this other block…
  ….can I shorten connectivity enough to gain performance and save power?

Early multi physics analysis for STCO

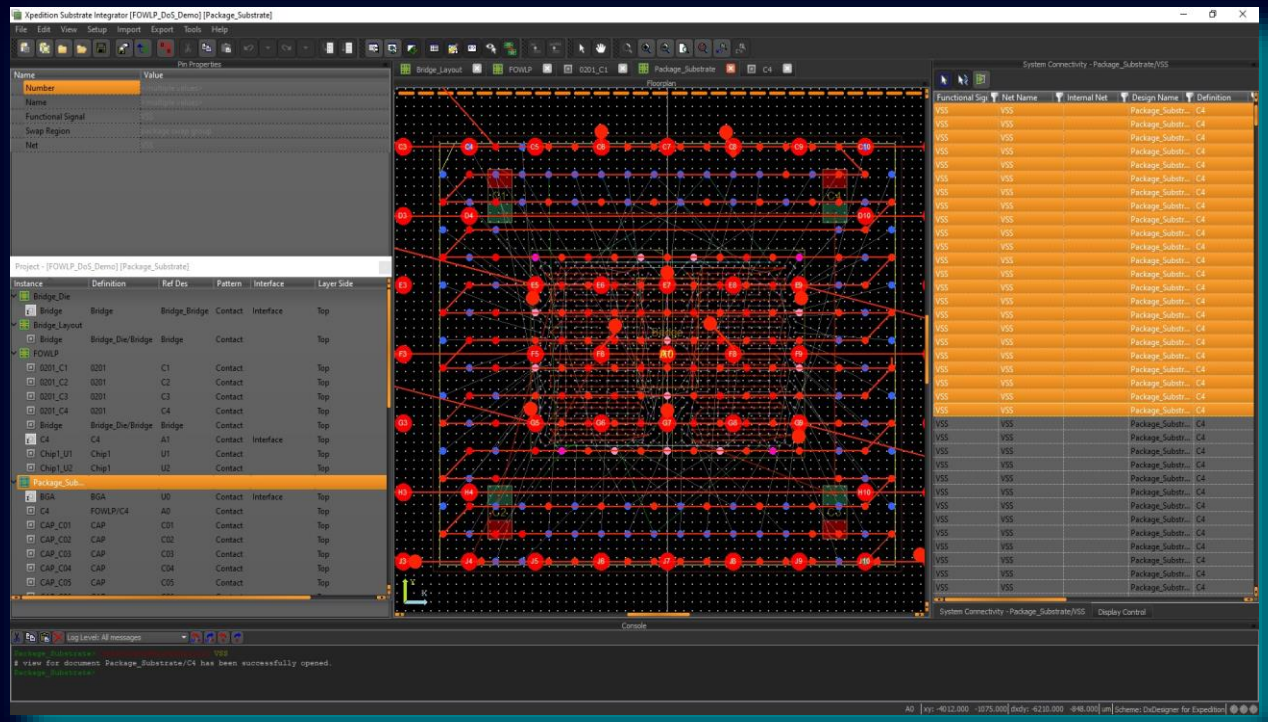
Multiple valid partitioning options?

- There are usually several valid partitioning solutions
- **Finding the right one is STCO**

Early multi physics analysis for STCO

Package Prototyping

- To find the right solution:
  - **Build an early package prototype Using early preliminary data**
- We simulate
  - **Simulation results help us make educated decisions!**

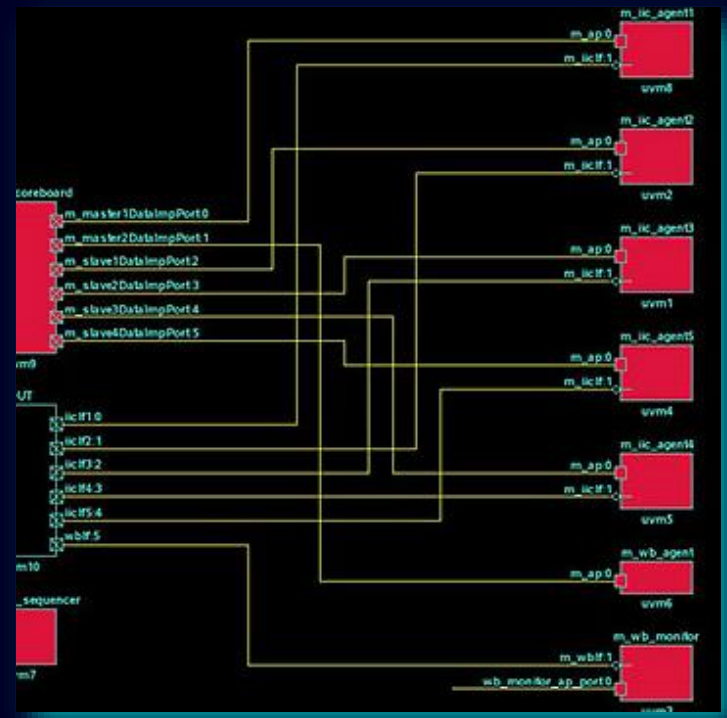


Early package prototype to drive analysis

Early multi physics analysis for STCO

Step 1

- We know which functions/chiplets to use
- We MAY have LEF/DEF of some detail that we can use
- We know their signals
- From System Verilog we know how they are intended to connect
- Estimate needed number of pwr/gnd bumps
- Create preliminary bump map



Visualizing System Verilog in graphic form help you understand connectivity

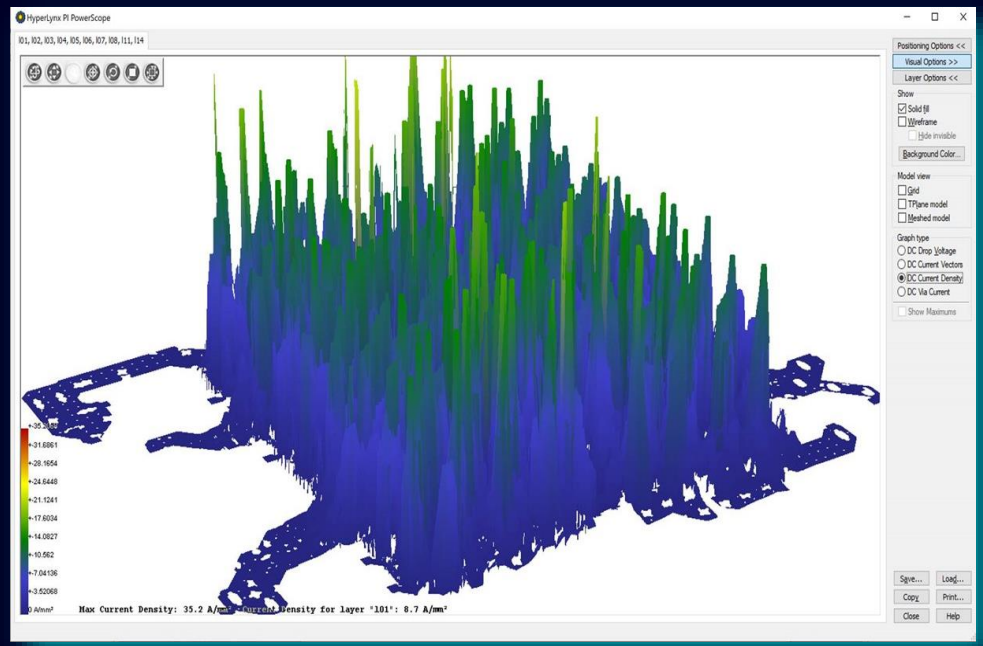
This is not a detailed implementation –It's a high level model of our intent

With the model in place we can move to action

Early multi physics analysis for STCO

Power Integrity (PI)

- Feeding the Package Prototype to a PI simulator let you
  - Find potential trouble areas of various degree
  - Use this information to
    - Re-arrange Pwr/Gnd assignments locally
- **Feed gained knowledge back to silicon teams for reconsideration**

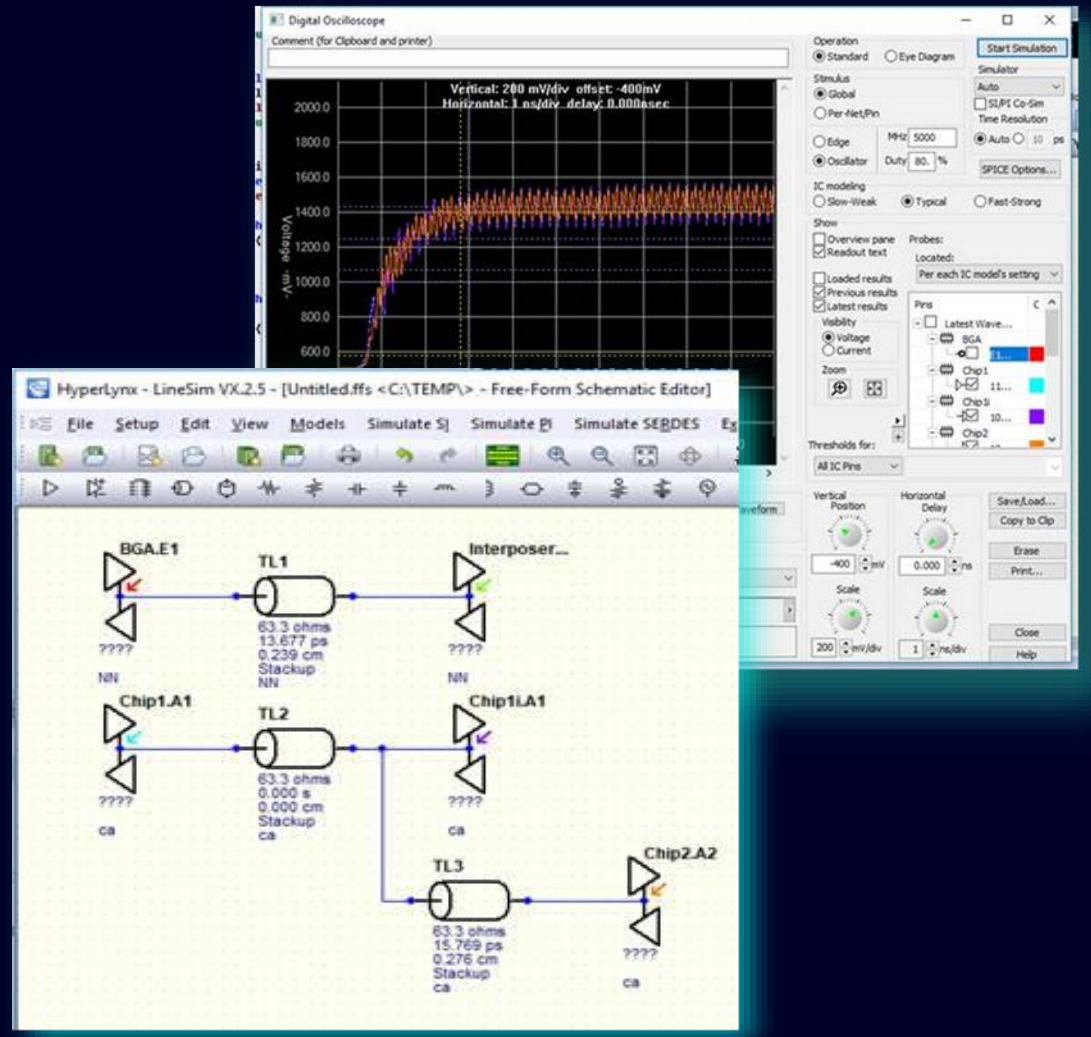


Example of Early Power Integrity Estimation

Early multi physics analysis for STCO

Signal Integrity (SI)

- Same as with PI: Feed model to simulator
  - Evaluate if the 2.5D/3D packaging scenario can meet required performance **based on preliminary input!**
  - Use this information to
    - Re-arrange signal assignments locally
  - **Feed information back to silicon teams for reconsideration**



Example of Early Signal Integrity Estimation

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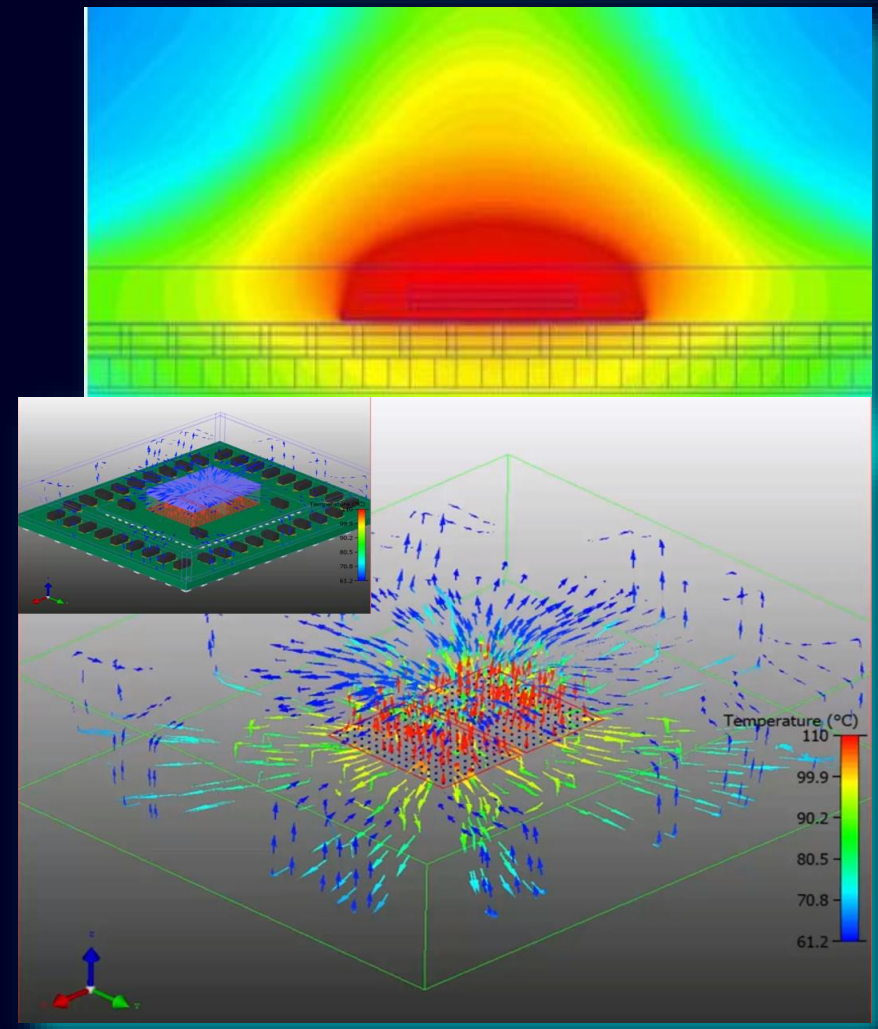
Early multi physics analysis for STCO

Thermal Integrity

- The more we integrate into a small volume
  - The larger the risk of a major thermal issue
- Package Prototype has enough detail for an early thermal investigation
- Need 3D Thermal for 3D packaging
- **Thermal issues probably requires re-partitioning**



Example of Early 3D Thermal Integrity Estimation

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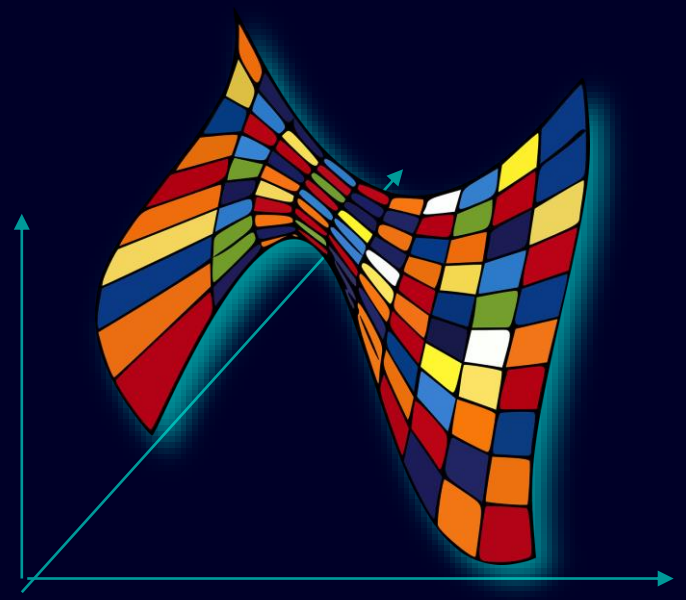
Early multi physics analysis for STCO

Multi physics?

- **Our Package Prototype is a "Digital Twin"**
  - Depending on requirements, we can apply
    - Mechanical stress analysis
    - Package warping analysis
    - Other multi physics evaluations ….



And use this data up front to help drive design partitioning and package configurations

Early multi physics analysis for STCO

Can we replace assembly verification?

- STCO and early analysis does not replace:
  - More accurate simulations
  - Functional verification at design and package level
  - Package and 3D assembly verification

- Nothing prevents verification runs on partially completed designs
  - Discover potentially costly issues earlier than at tape out

Conclusion

Early system partitioning and integration planning

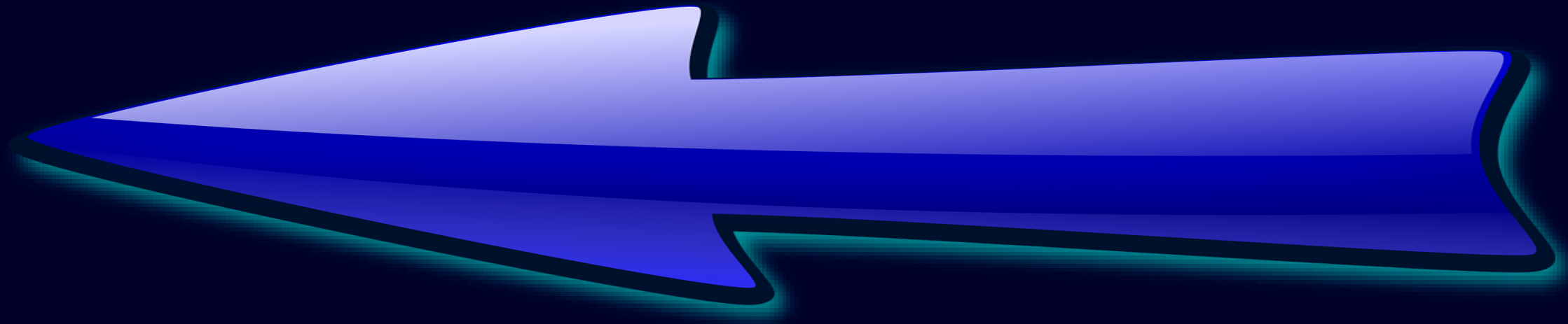
- **Can have a profound impact on physical implementation areas:**
  - Power Integrity
  - Signal Integrity
  - Thermal performance
  - Package Warping
  - Mechanical stress

- **If not properly managed, the entire product might fail!**

Conclusion

At partitioning, we can't see the physical consequences of our decisions

- Not enough is known at this stage for detailed simulations
- **Enough is known to make fast approximate analysis and use this up front to make better decisions; Shift Left!**



Conclusion

Shift Left

- **Start early to feed partitioning to package prototyping**
- Build a package prototype
- Perform multi physics analysis

- **Knowledge and solutions found through early analysis is used**
  - **To help drive IP partitioning**
  - **Enable silicon teams to make better and educated decisions**
  - **Help converge to an optimal package design faster**

Before cost of change becomes prohibitive:

Move decisions up early: Shift Left!

Thank You!

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