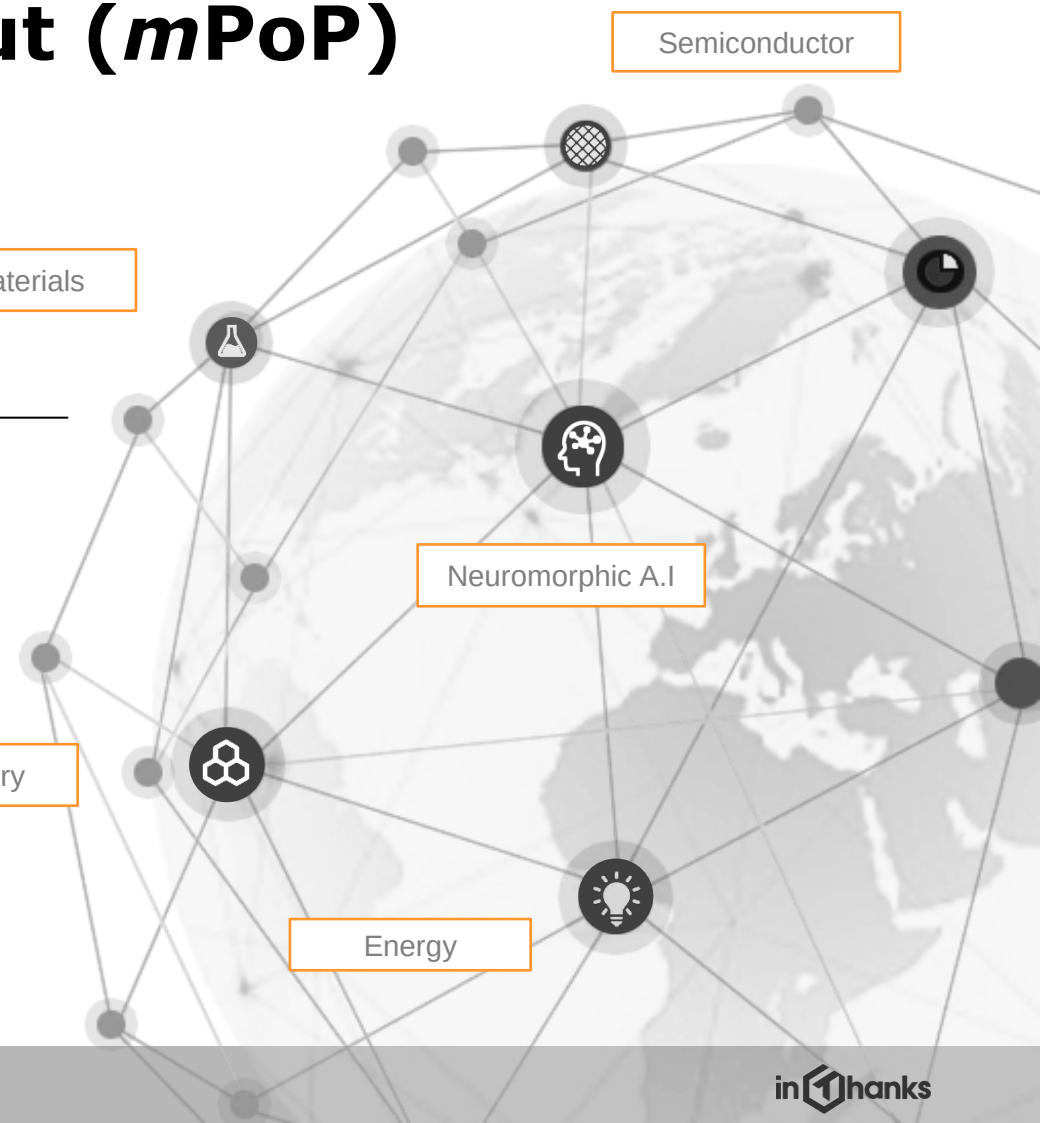
nepes corporation

Innovative Package on Package Solution: M-Series Fan-Out (*m*PoP)



Corporate CTO Unit

Byung Cheol, Kim

April 07, 2021

Bio

Director of RnD, Design and NPI for nepes hayyim

1996 – 2008	*Amkor Technology*
2008 – 2009	*Cypress Manufacturing*
2009 – 2020	*Deca Technologies*
2020 - current	*nepes hayyim corporation*

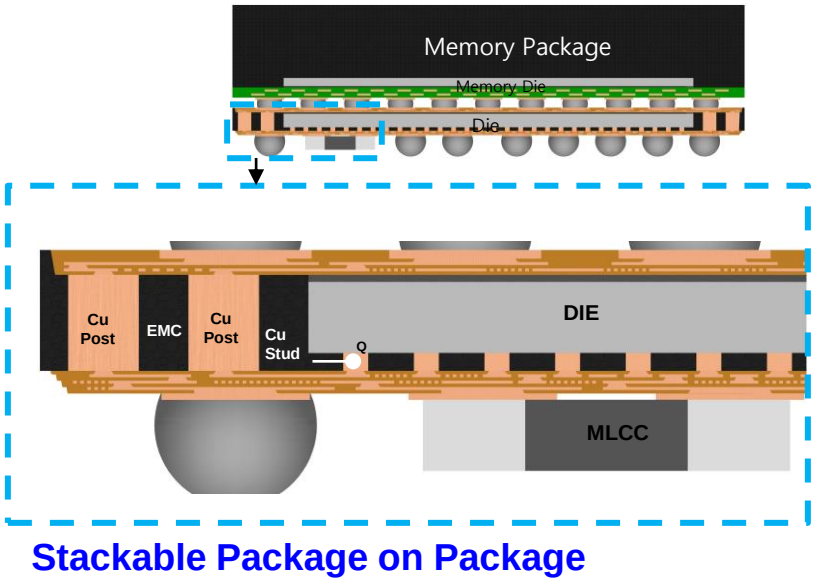
25 years of Semiconductor experience

Contents

Introduction

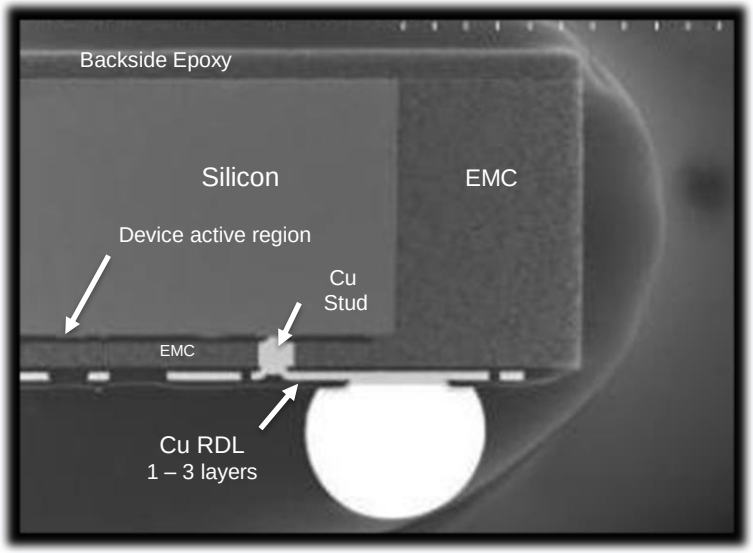
*m*PoP, the stackable package on package structure to provide competitive integration solution of application processor (AP) and memory device based on M-Series™ technology.

***m*PoP**(M-Series stackable Package on Package)



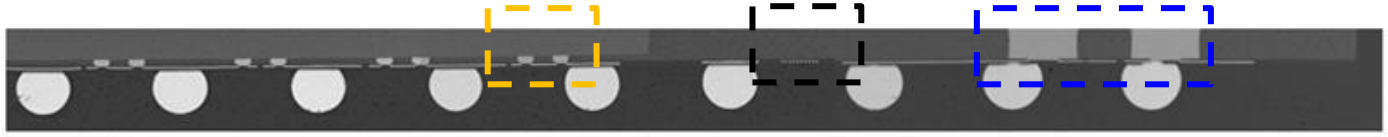
Stackable Package on Package

Standard M-Series (non-stackable package)

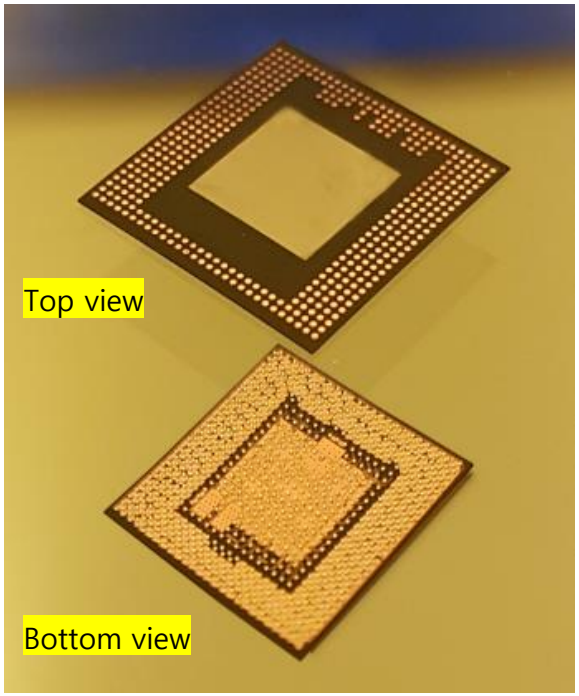


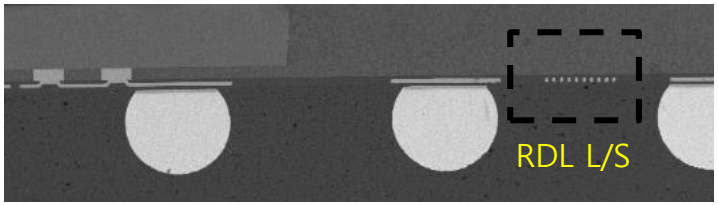
Introduction

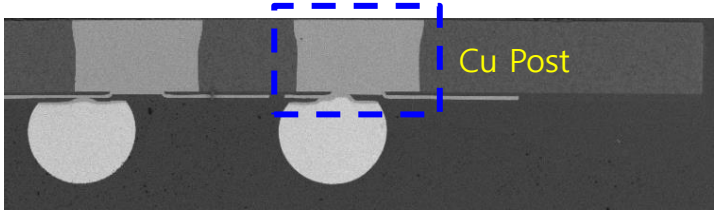
A solution with copper post interconnection structure with thinner profile

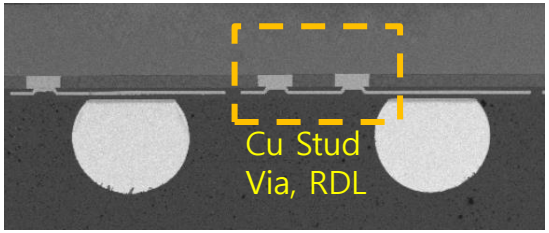


Thin Profile (<0.4mm)







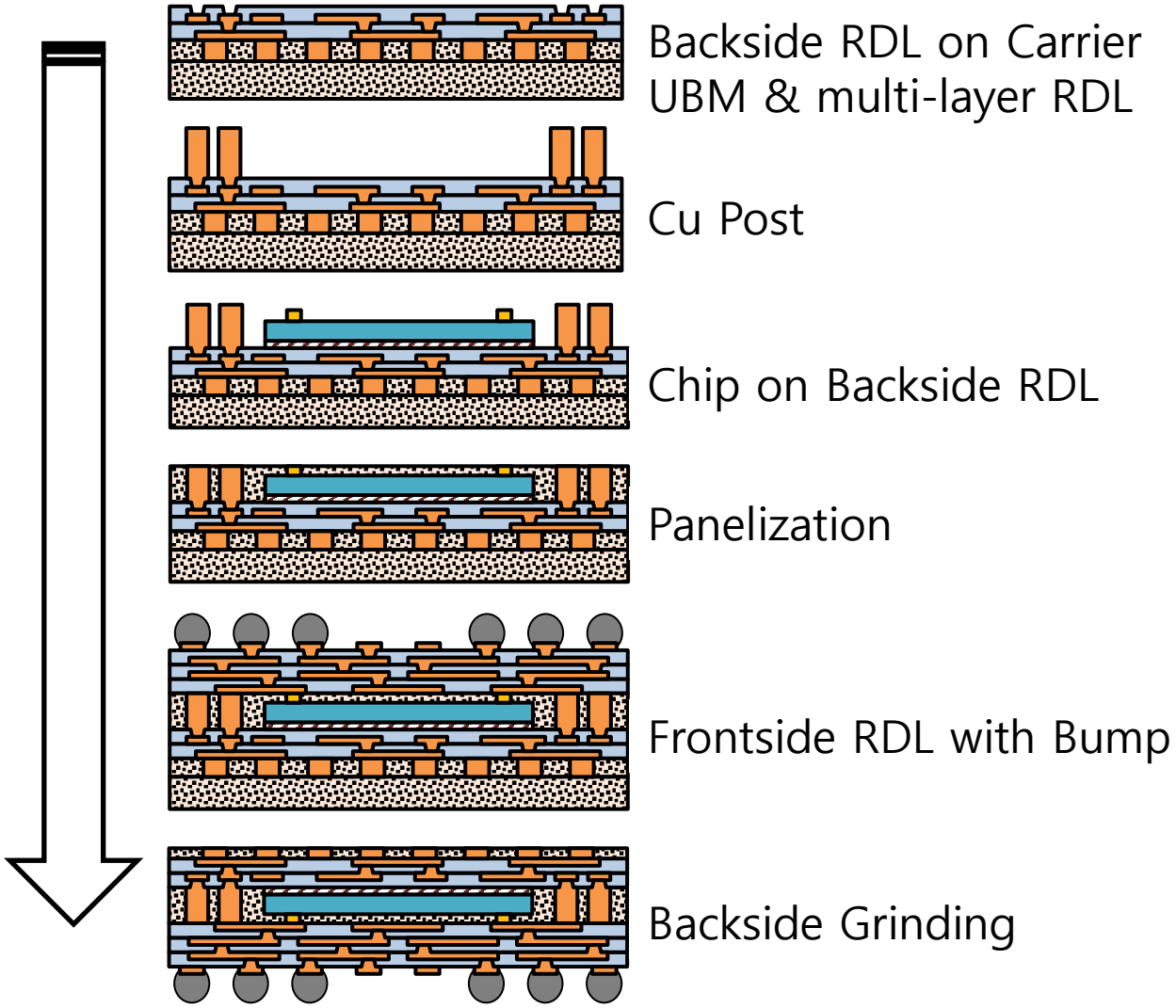


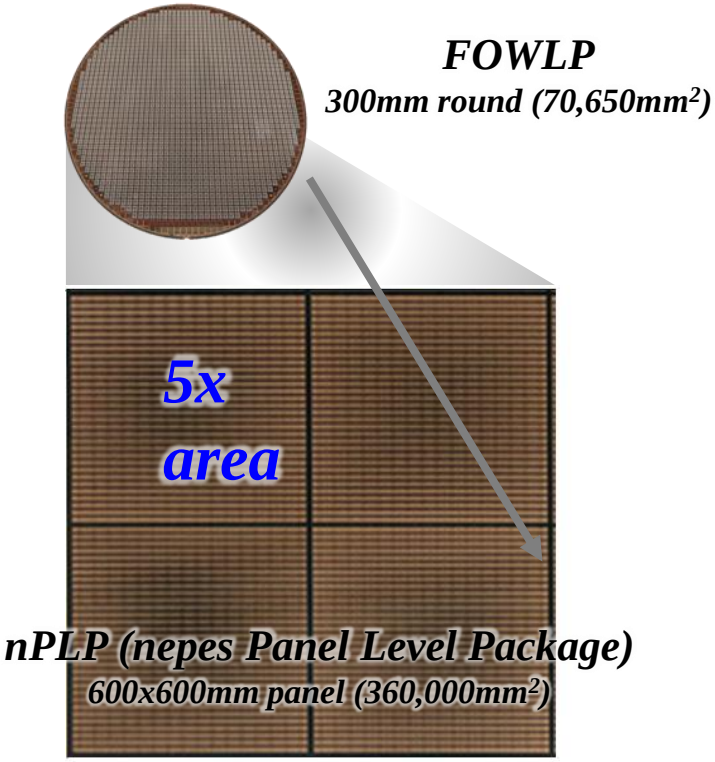
Cu Post as the key interconnection solution

nepes *m*PoP with low profile (1-layer RDL and 8um L/S)

Process Flow

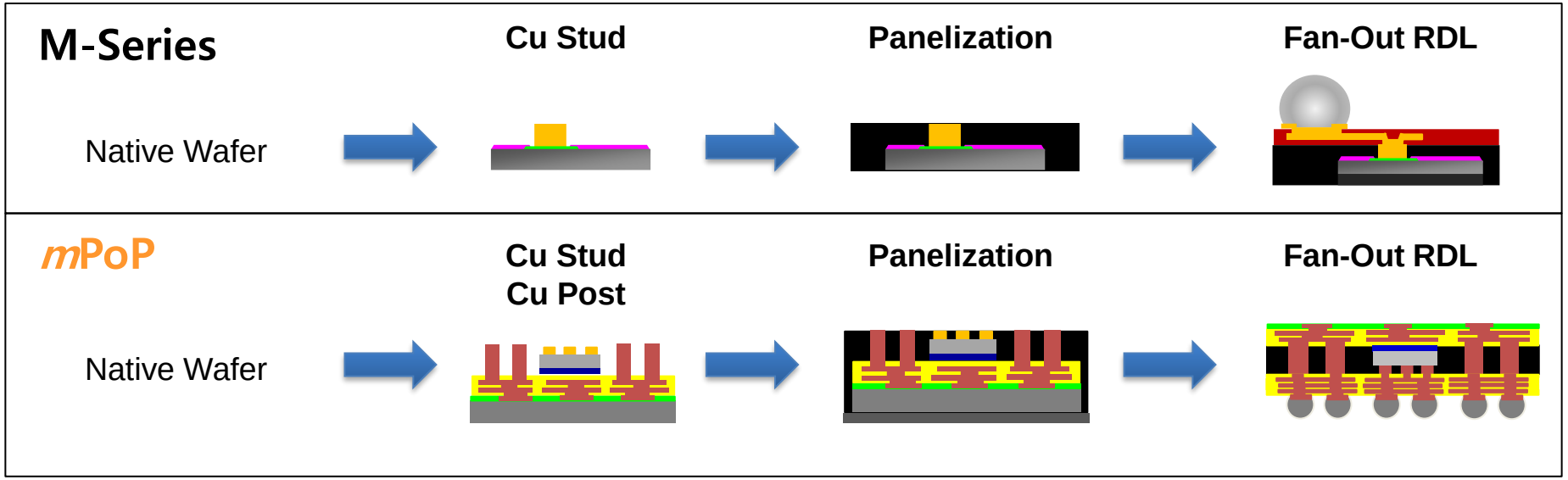
Nepes mPoP standard process flow for both 300mm round & 600mm square panel

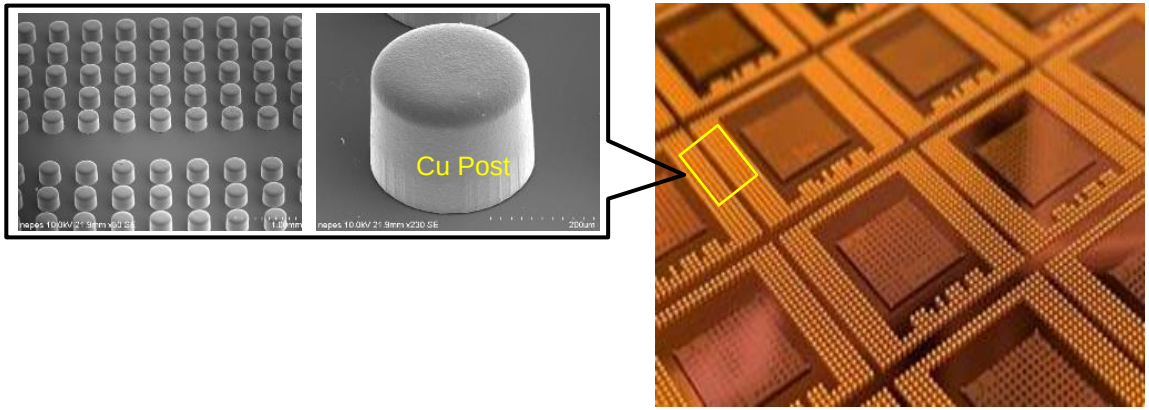




Process Flow

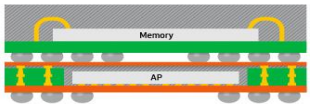
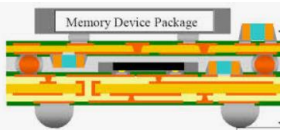
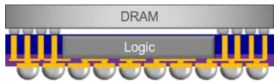
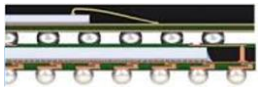
Comparison of standard M-Series process with mPoP process.
- Cu Stud die stack with DAF (Die Attach Film) prior panelization process





High density limitations and Solutions

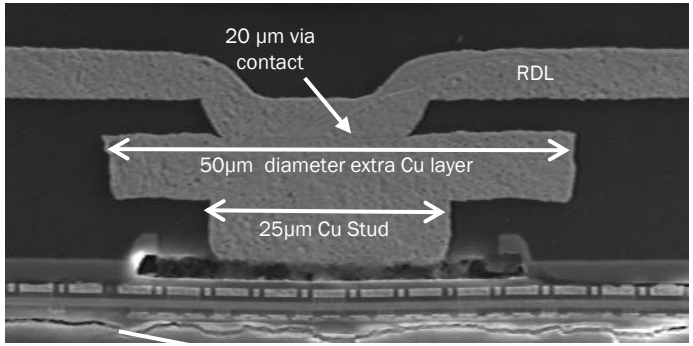
Minimum 5um RDL Line/Spacing plays a major role by the leading companies' PoP packages.
- nepes provides high density, 600mm PLP and Adaptive Patterning discreet options

Company					nepes corporation
Technology	Non M-Series based				M-Series based
	FCBGA / LDPPOP	**MCEP**	**InFO-POP**	**SWIFT™**	***m*PoP**
L/S	11μm/11μm	10/10um	5μm/8μm	5μm/5μm	5μm/5μm
Character	• Embedded passive device • RDL on organic substrate • Solder bump interconnect	• Coreless substrate • Copper core solder balls • Flip-chip with copper pillars	• Info-R (RDL) • Cu post & multi-layer RDL • IPD integration	• Chip Last • Wafer Carrier Technology	• Thinner & High performance • Chip First/Last Combination • Adaptive Patterning • 600mm PLP Technology
Status	• HVM	• Since 2017 HVM	• Since 2016 HVM	• Initial Promotion	• Development Stage
Structure					

High Density Solutions

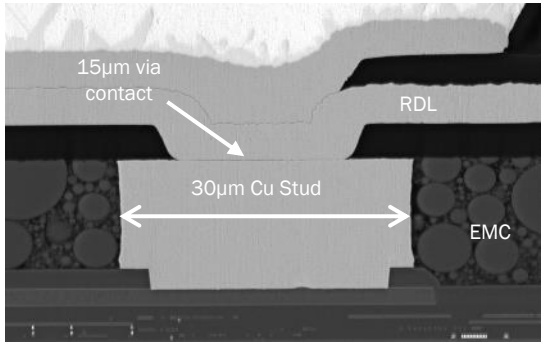
M-Series PoP (*m*PoP) has the capability of 45um Bond Pad Pitch with 15um Via
- nepes provides solution with Adaptive Patterning™

InFO™ without Adaptive Patterning (Latest Gen – iPhone 12)



Source: Prismark – Apple A14 in iPhone 12

M-Series™ with Adaptive Patterning (Gen 1)



Source: Deca – Customer PMIC

InFO via connection without Adaptive Patterning (Latest Gen – iPhone 12)

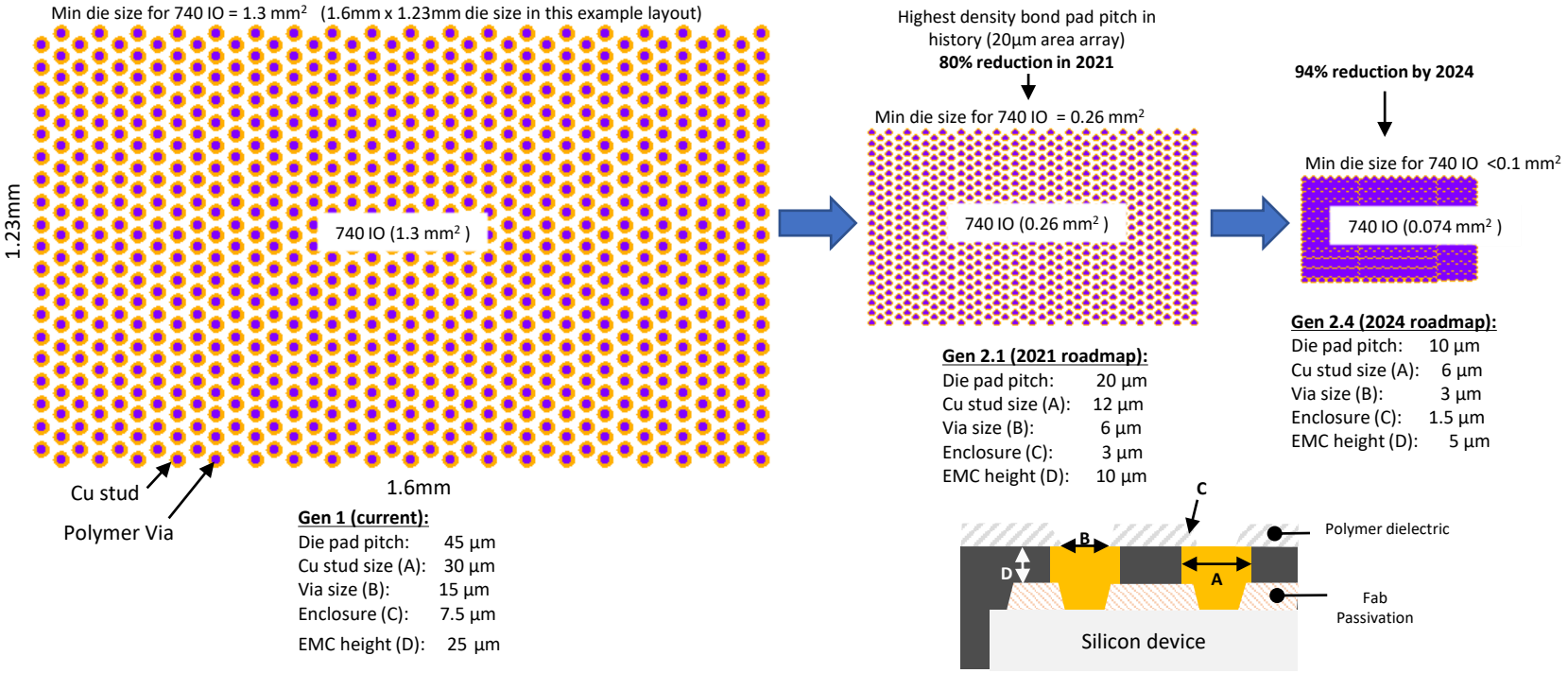
75µm capable Bond Pad Pitch

M-Series via connection with Adaptive Patterning (Gen 1)

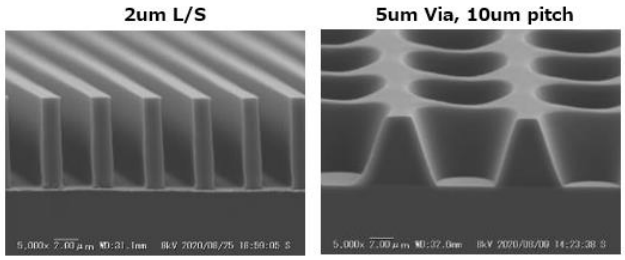
45µm capable Bond Pad Pitch

High Density Solutions

Ultra high density capability with 2um Line/Spacing & 5um Via
- nepes provides solution with Gen2 Adaptive Patterning™ and laser direct imaging from current 45um die pad pitch down to 20um

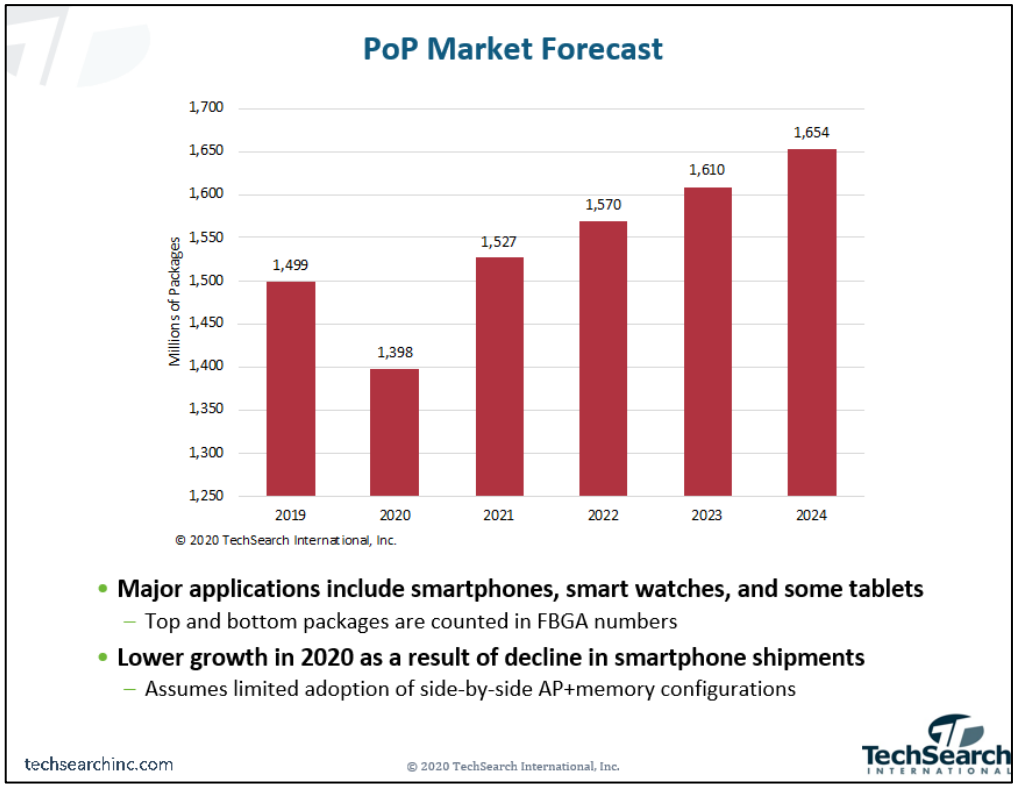


80% reduction in die size possible based bond pad area required
(From current design rule of 45µm BPP to 20µm BPP in 2021)

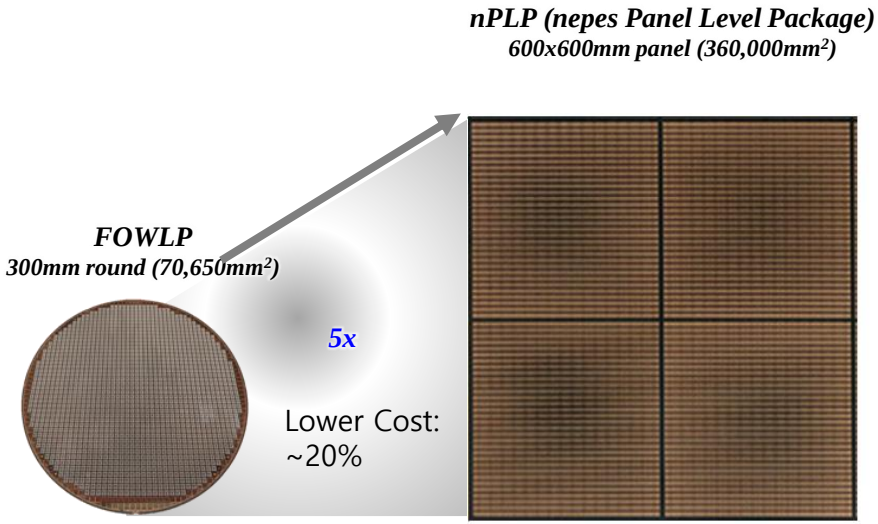


PoP Market & Cost Competitiveness

In 2021, market forecast showed significant growth from 2020 and continues to be stronger for succeeding years. It is critical to find a solution for the PoP market with a cost-effective platform. 600mm PLP is an attractive solution with 5X increase in usable area in comparison to 300mm round panel.



Source: TechSearch International, 2020



Conclusion

The *m*PoP has high density capability with 5um L/S & 15um Via and will have 2um L/S & 5um Via for Ultra-high density through Adaptive Patterning™ technology.

Due to larger die size ($>10\text{mm}^2$) requirements for certain applications, 600mm PLP will be the better solution in terms of cost in comparison to conventional PCB based packaging technologies.