Heterogeneous Packaging Optimizing Performance and Cost

Mike Kelly | VP, Advanced Package & Technology

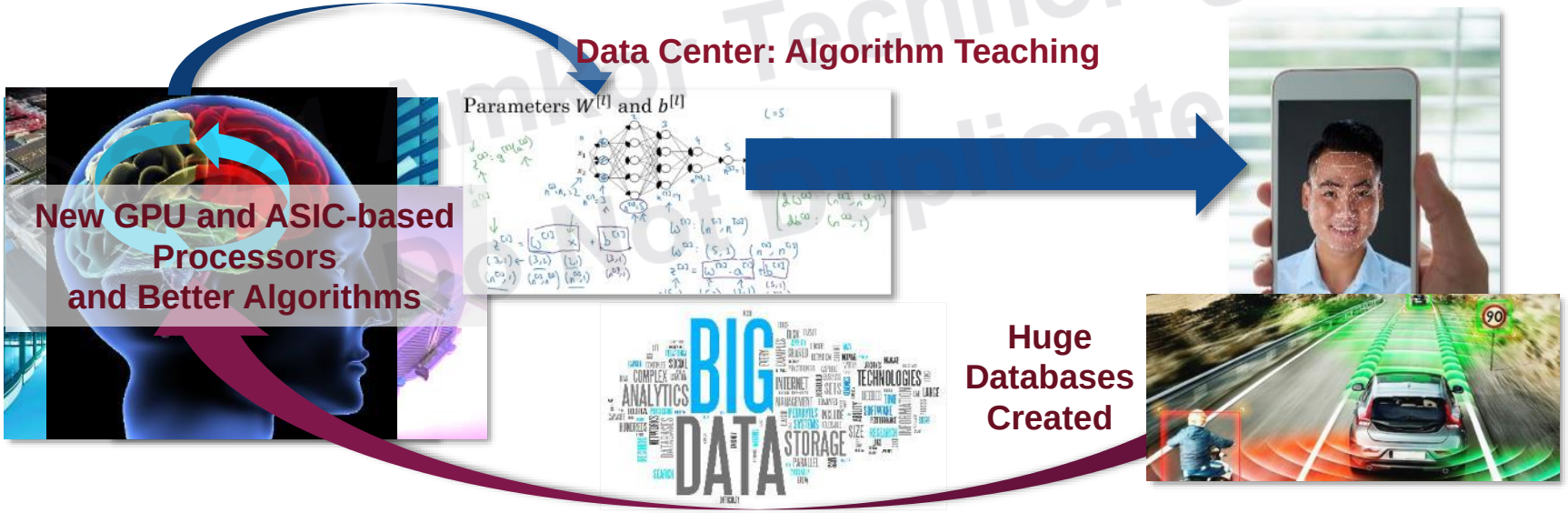
April 2021

Agenda

1. Silicon Trends
2. IC Packaging Trends
3. Heterogeneous Solutions

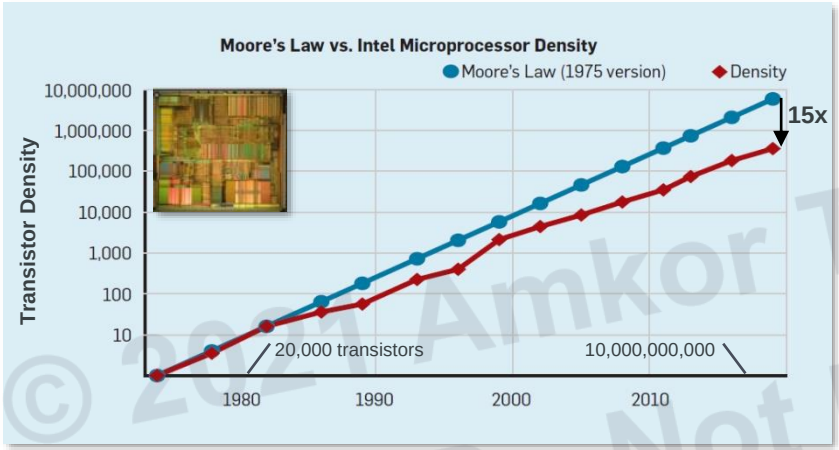
Heterogeneous IC Packaging

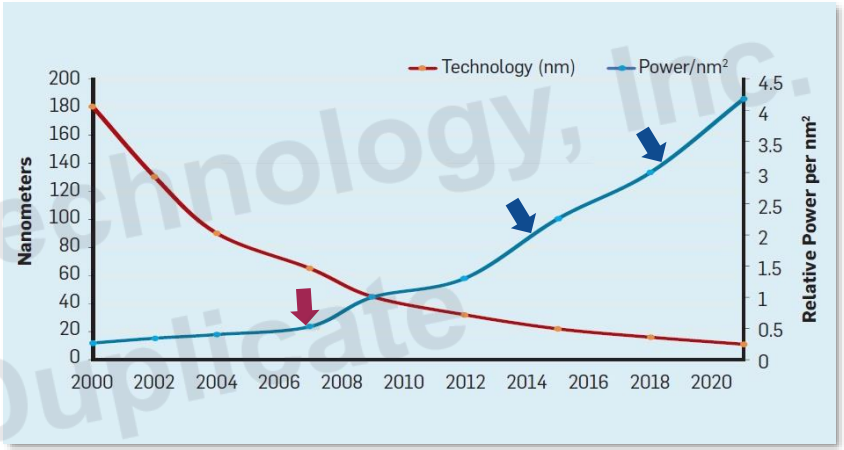
Data Centers | Edge IT | Internet Gateways | Connected Devices



Silicon Trends

Silicon Trends: Transistor Density Increasing

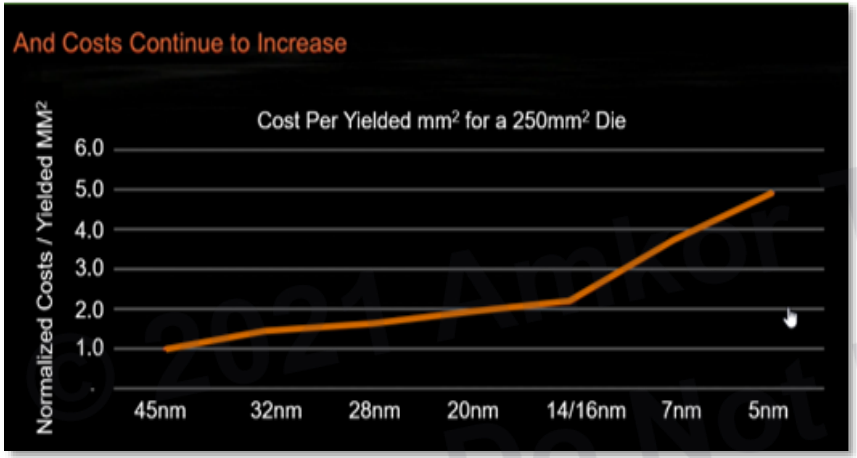




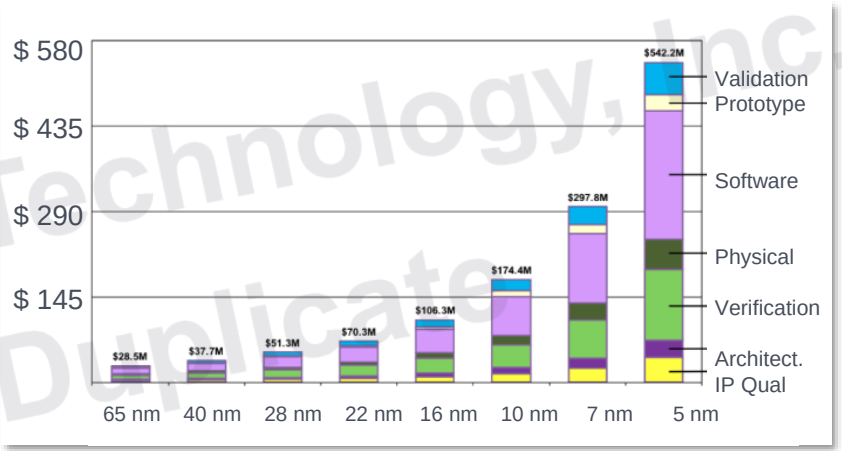
Source: Communications of the ACM, February 2019

- Transistor density continues to increase, but well behind the Moore's Law of doubling every 2 years
- Moore's Law is NOT dead, **but slowing**
- **Power density is still increasing**

Silicon Trends: Dramatic Cost Increases



Source: Lisa Su, AMD CEO, CES 2020



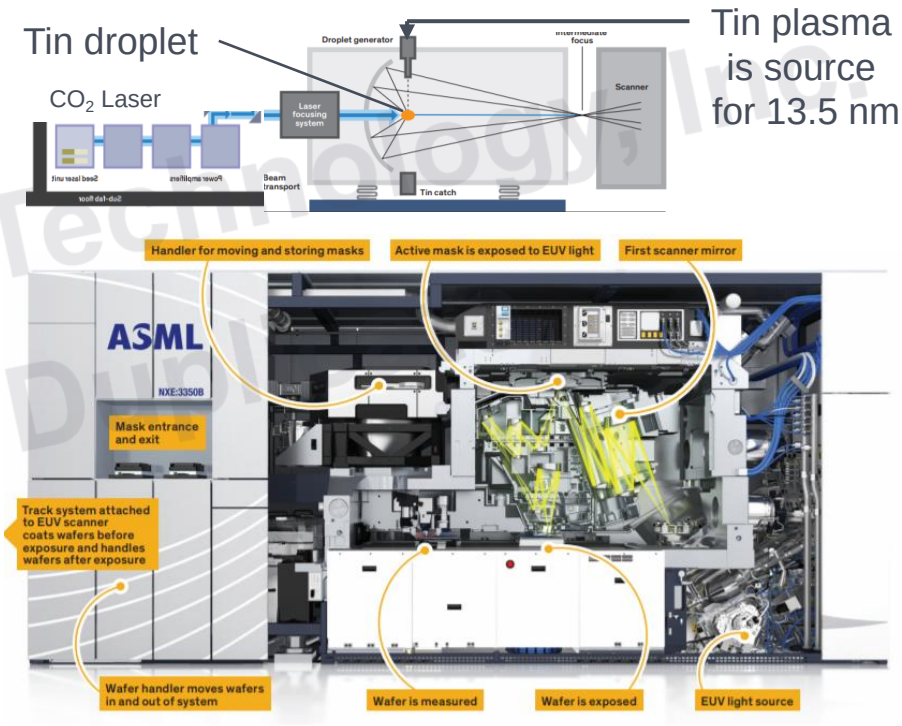
Source: IBS

- Yielded Cost: 1.8x 16 nm → 7 nm

  250 mm² die

- Wafer Cost: $20-25K (7 nm)
- Design Cost: ~$500M

Silicon Trends: EUV for 7 nm and Beyond



IC Packaging Trends

HPC Product Trends and IC Package Implications

Power

Higher memory BW
at **low power**

- Memory co-located in package or on chip (data locality)

High wafer costs
Higher I/O Count

- Chiplets: Move IP blocks like SerDes I/O drivers to older silicon nodes

Better PDN required

- Ultra low ESR caps, IPDs, VRMs (Voltage Regulator Modules)

Increasing dissipated power

- Improve thermal power dissipation solution for the package

Heterogeneous Integration

Wafer Costs

Design Costs

Power Increases

IP Reuse

TTM

Better Power Dissip.

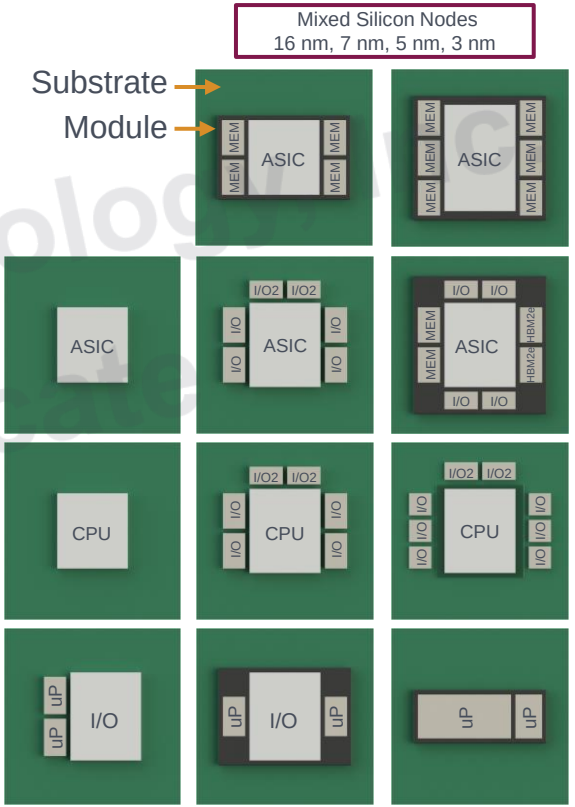
Better PDN

Deep Learn/AI Training
- Memory BW
- Lower power

NW Switch/Router
- Increase I/O count
- More gates

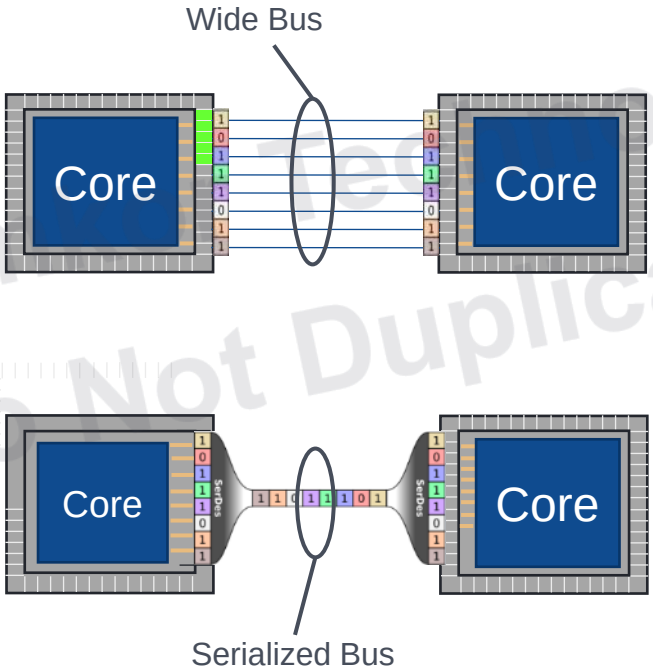
CPU, Server
- Address more DRAM
- Client PC

PC CPU/GPU
- Lower cost



Die-to-Die Interface: Package Differentiation

- Parallel interfaces
  - More physical wires
  - **Lower latency**
  - Lower power



- One physical wire/bit
- Each I/O driver is small

- Serial interfaces
  - Fewer physical wires
  - Higher latency
  - Higher power

- Many bits per wire pair
- Large I/O driver area

Bus Type – Package Influence

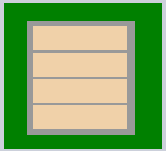
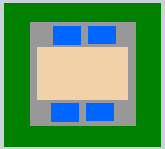
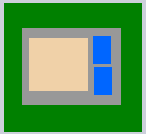
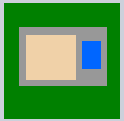
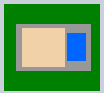
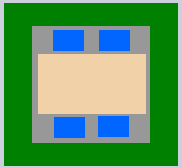
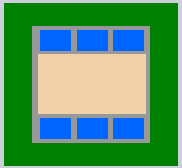
- More chiplet products coming
- Parallel interfaces
  - More physical wires
  - Lower latency
  - Lower power
- Serial interfaces
  - Fewer physical wires
  - Higher latency
  - Higher power
  - Mostly memory interfaces

7 nm/5 nm Implementations

- **FCBGA with modules**
  - 2.5D TSV – HVM dominated by AI and HBM
  - S-SWIFT® – High density fan-out
  - S-Connect – Sub 2 µm L/S
- **FCBGA MCM**
  - Core + ABF – incrementally improve
  - Coreless
  - Hybrid coreless substrates
- **fcCSP IP PoP**

2.5D TSV (CoW)

2.5D TSV Product Experience

Application	FPGA	GPU	GPU	Networking	GPU	GPU	GPU
Configuration	4-ASIC	ASIC + 4HBM	ASIC + 2HBM	ASIC + HBM	ASIC + HBM	ASIC + 4HBM	ASIC + 6HBM
Assembly	CoS	CoS	CoS	CoS	CoW	CoW	CoW
PKG	45 x 45 mm	55 x 55 mm	47.5 x 47.5 mm	42.5 x 42.5 mm	41 x 31 mm	55 x 55 mm	55 x 55 mm
Interposer	31 x 25 mm	36 x 28 mm	30 x 28 mm	30 x 19 mm	27 x 15 mm	43 x 34 mm	47 x 36 mm
ASIC	24 x 7 mm (x4)	26 x 22 mm	26 x 19 mm	18 x 16 mm	17 x 13 mm	32 x 26 mm	33 x 26 mm
Si node	28 nm	28 nm	14 nm	14 nm	14 nm	12 nm	7 nm
Memory	–	HBM	HBM2	HBM2	HBM2	HBM2	HBM2E
Status	Demonstrated 2013	Qualified/ LVM 2016	Qualified 2016 HVM 2017	Qualified 2018	Qualified HVM Q3'2019	Qualified HVM Q1'2019	Development HVM 2H2020
Floor plan							

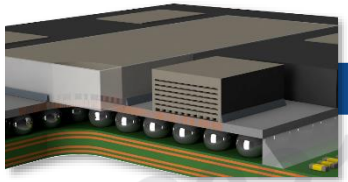
Floor plan
- Substrate
- Si interposer
- Logic
- Memory/ Small logic

S-SWIFT®

Advanced Modules

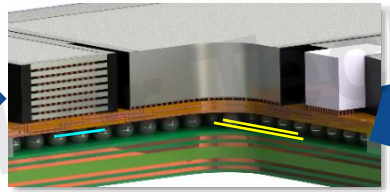
High Density Fan-out Evolution

2.5D TSV



RDL Interposer

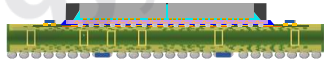
HDFO on substrate

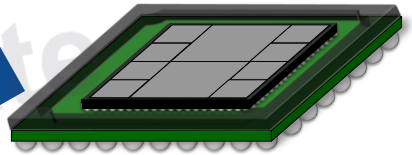


Diversification

More Diversification

Smaller with cost emphasis
Large with more integration





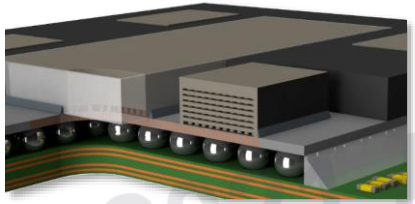
- Mostly logic + HBM2/2E

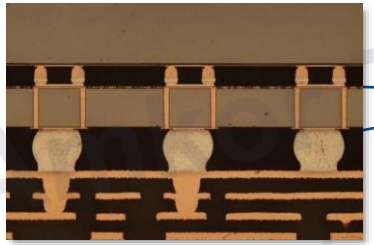
- Logic + HBM2/2E/3
- IO die chiplets

- **Cost emphasis**
  - Lower layer count
  - Die first and Die last
- **Module size → 3x reticle area**
  - Better PDN solutions

2.5D Heterogeneous Interposer Options

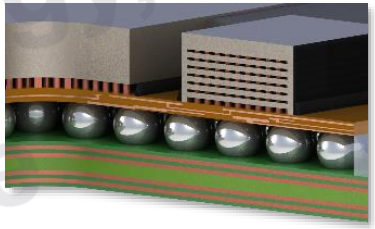
TSV Interposer





- HVM ongoing (2x reticle interposer)
- Flexible prototype
- >99% yield (TSV finishing and assembly)
- 3x interposer qualification in 2021

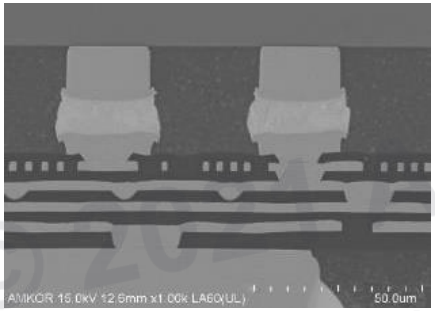
RDL Interposer (S-SWIFT®)



- Qualified Si-Si and Si-HBM2 qual in Q1'21
- Flexible prototype
- ~99% yield (2 µm L/S RDL and assembly)
- 3x reticle development in 2021
- RDL L/S down to 1.5 µm in 2021

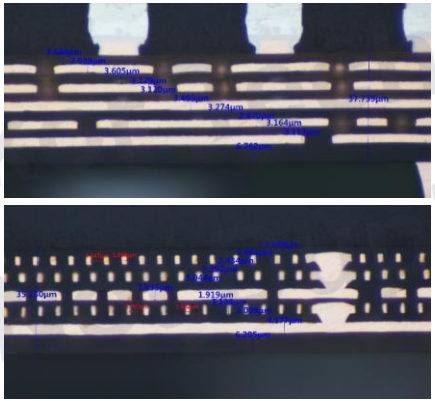
RDL Fabrication Capability

2 µm L/S, 4 Layer



- ~99% RDL yield
- Stacked vias with minimized dimple
- Reliable screen through AOI and in-line test

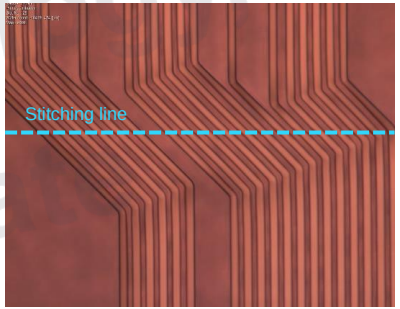
2 µm L/S, 6 Layer



5L successfully demonstrated

- 6L build ongoing

Larger Area, 3x Reticle

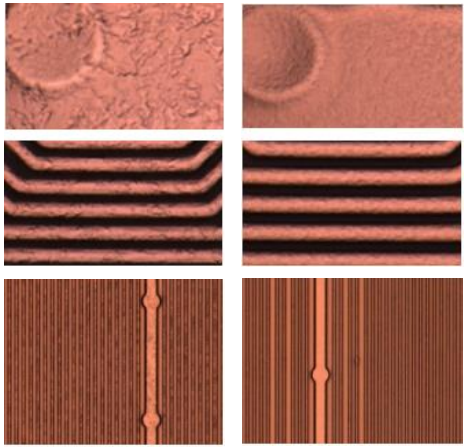


- Development ongoing

Detectability Enhancement

Process Improvement

Before | After



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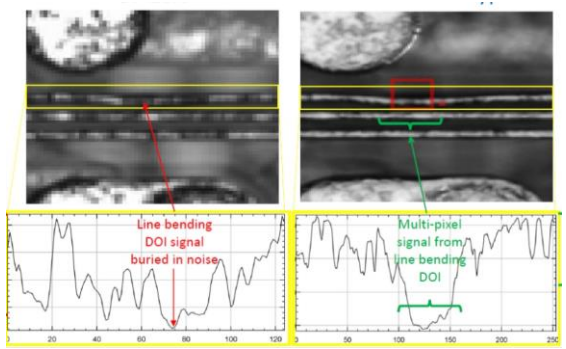
AOI Detectability Improvement

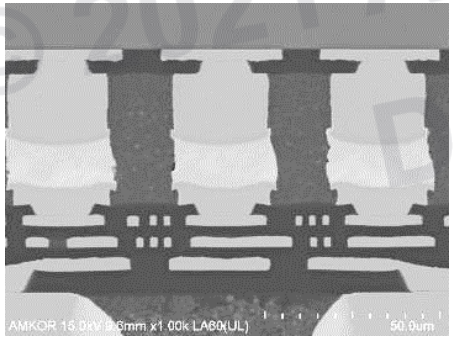
Before | After



S-SWIFT®: Package Development Status

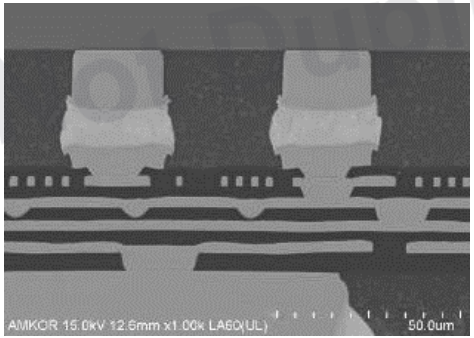
Multi Logics

- Large ASIC die-split (2 ASICs)
- 3 Layers of 2 µm RDL
- **Package qual pass**



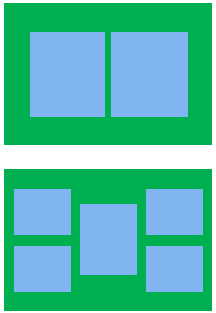
Logic-HBM2 (Daisy Chain)

- 2.5D product re-design
- ASIC + daisy chain 2 HBM2
- 4 Layers total; 3 layers of 2/2 µm
- **Package qual pass**

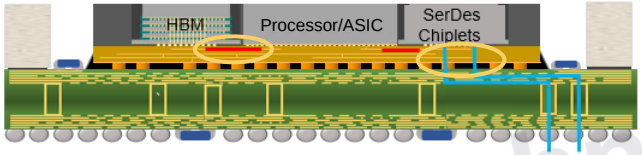


Chiplets

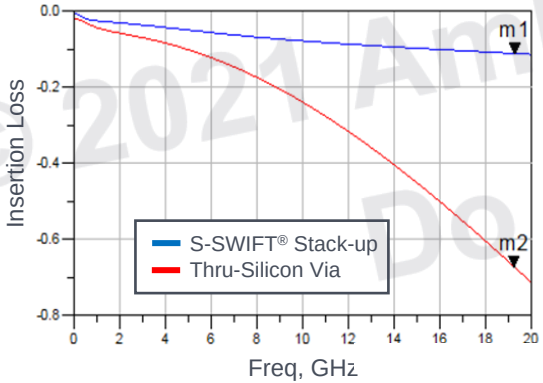
- Strong current trend, 2-8 die
- 1-3 Layers
- Tight bump pitch (35-50 µm)
- **Prototyping**



S-SWIFT®, 2.5D TSV Electrical Simulation

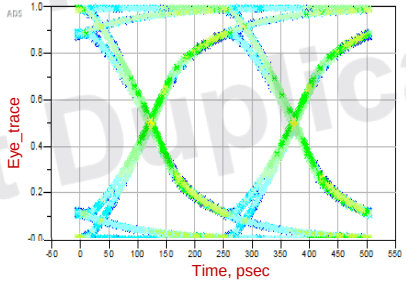


Z-direction, Through Interposer and Off Package

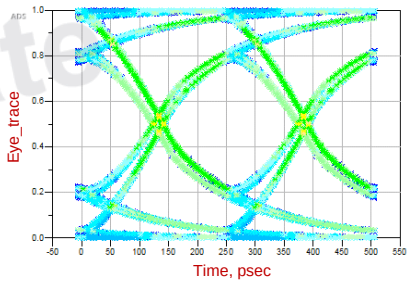


- S-SWIFT®: 4 RDL and vias
- Silicon Interposer: BEOL + TSV

X-Y Routing, 50 ohms

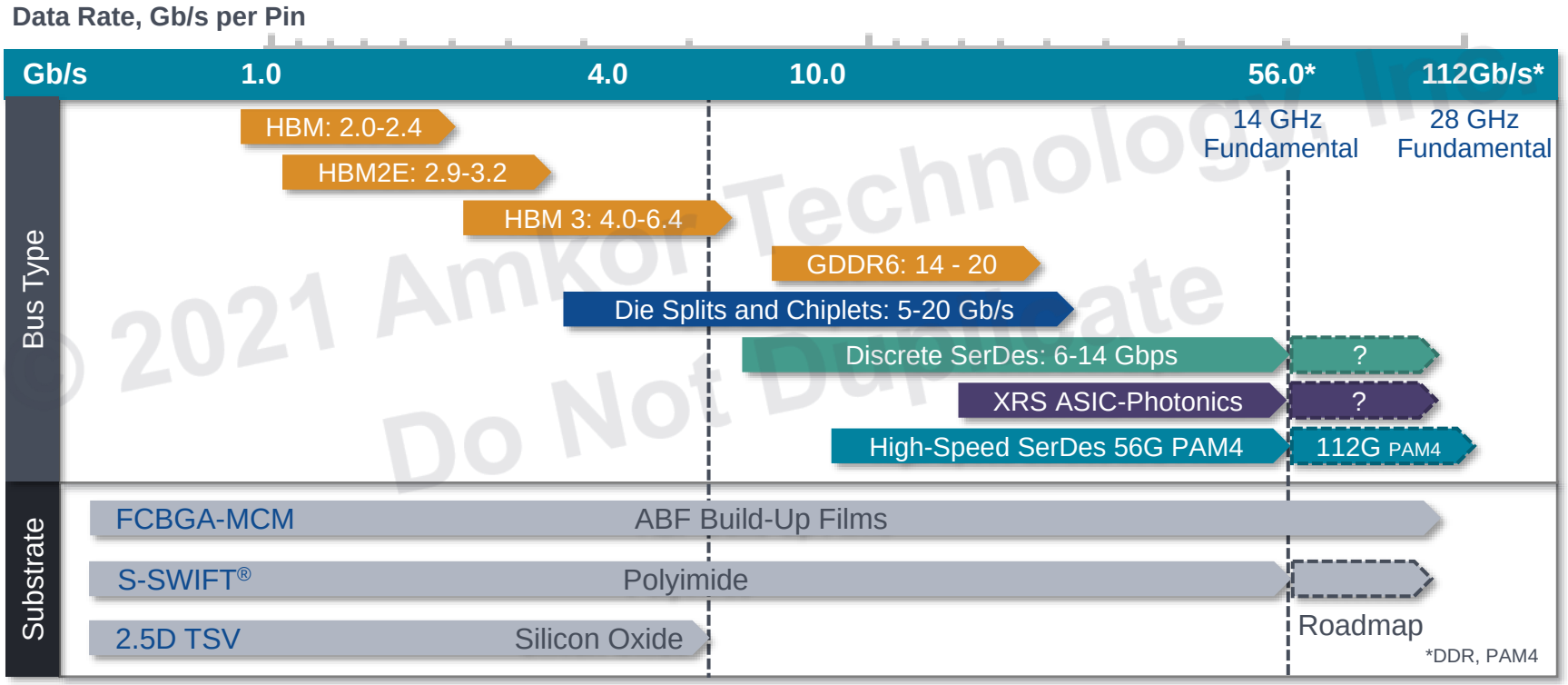


S-SWIFT®
Data rate 4 Gbps
Level zero 0.076 mv
Level one 0.93 mv
Eye height 0.67 mv
Eye width 239 ps
Jitter(pp) 11 ps

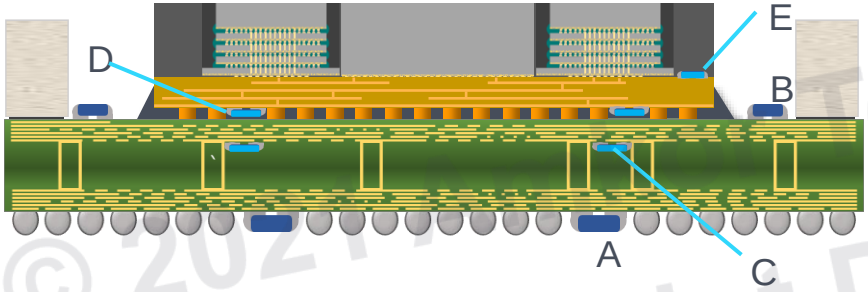


2.5D TSV
Data rate 4 Gbps
Level zero 0.13mv
Level one 0.88mv
Eye height 0.49 mv
Eye width 229 ps
Jitter(pp) 22 ps

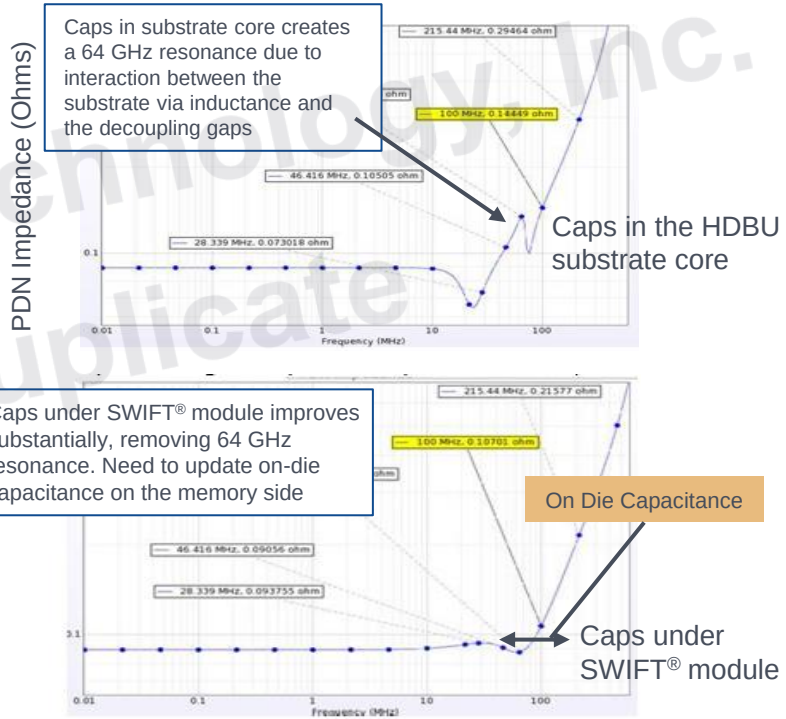
Heterogeneous: Electrical Performance



S-SWIFT® Power Bypass Location Consideration



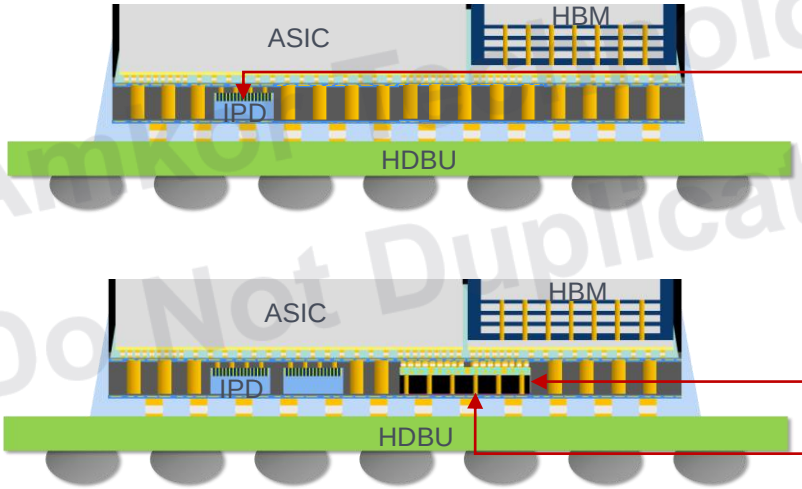
A – BGA side of substrate
B – Top side of substrate
C – In the substrate core
D – Bottom side of the SWIFT® module
E – Top side of the SWIFT® module



S-Connect Development Items

Key Features

- Target application
  - Multi-die applications
- Milestones
  - Dev: 2Q 2021
  - Qual: 2021 end
  - Bridge with TSV: TBD



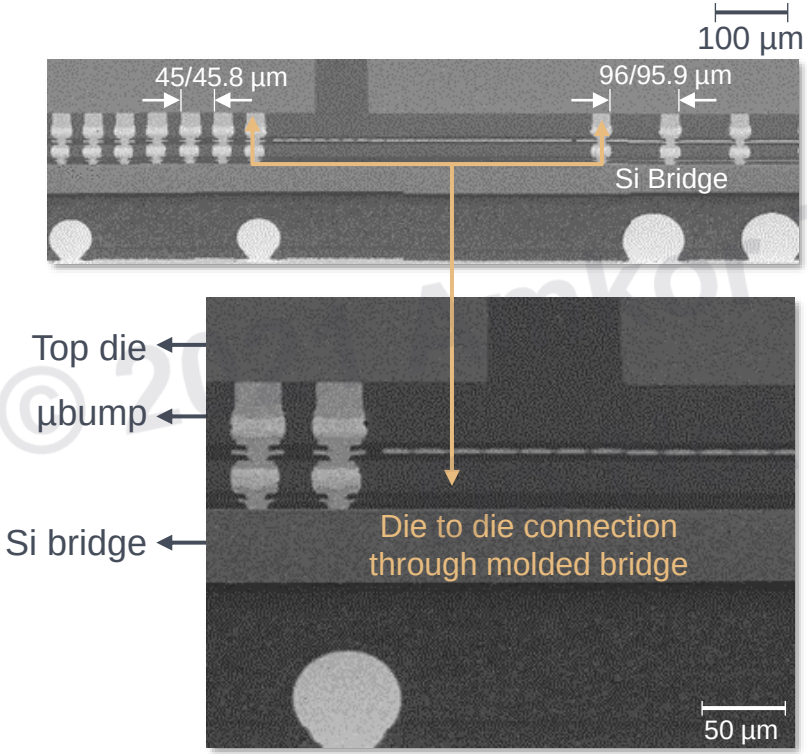
Key Dev. Items

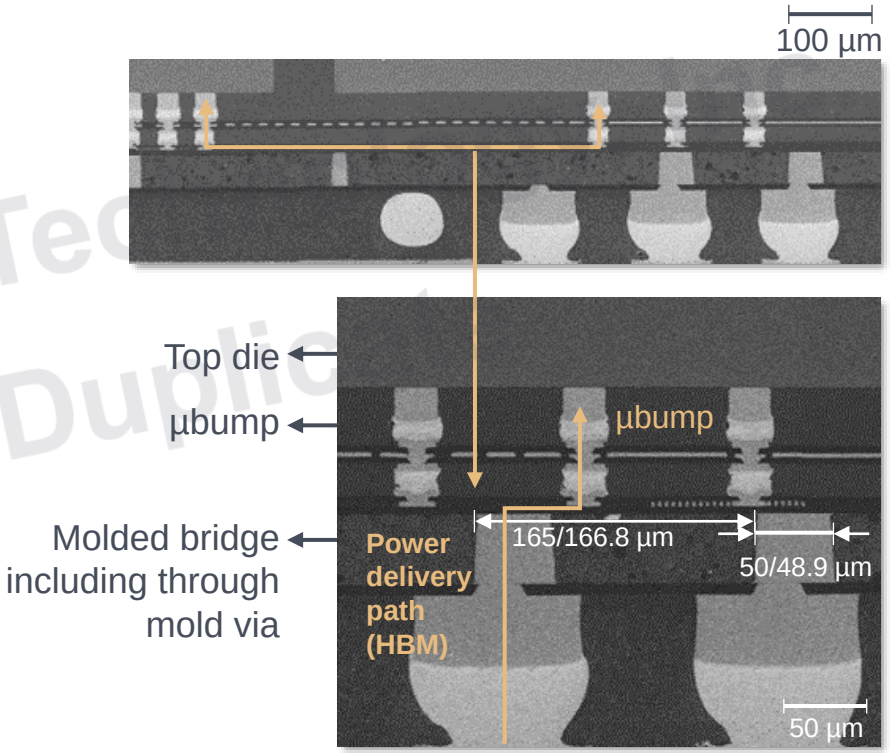
- IPD for power supply

Key Dev. Items

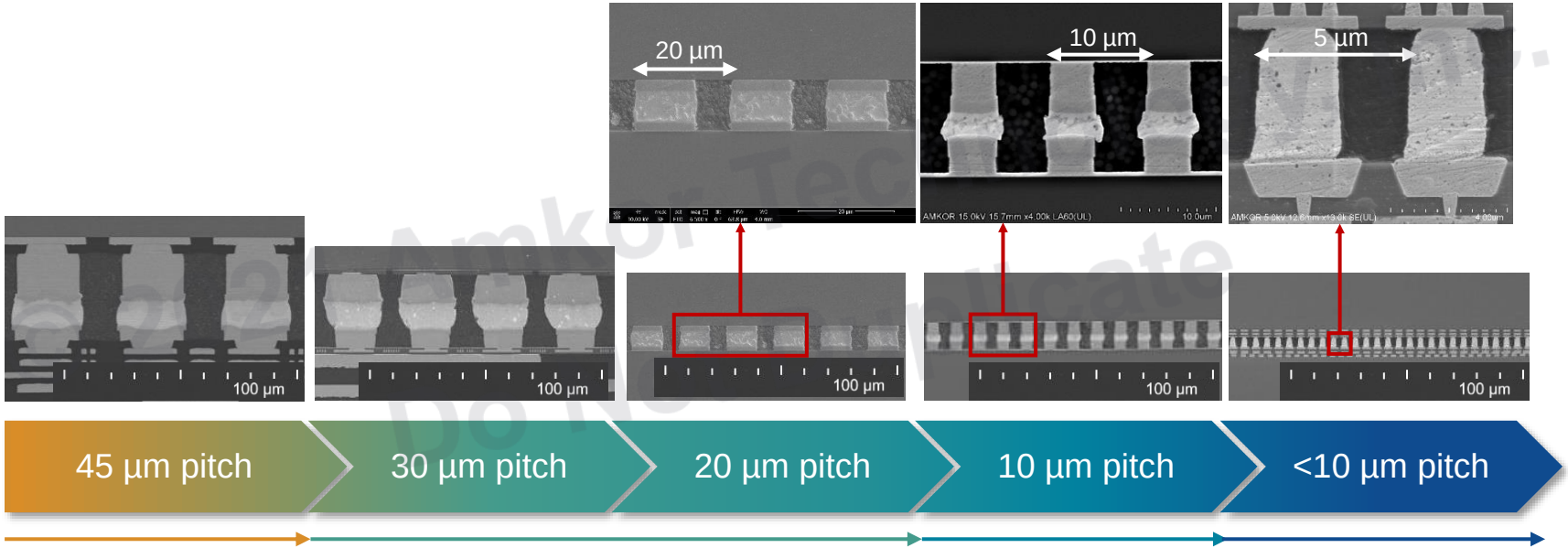
- Bridge die type: RDL on mold w/ tall pillar, RDL on Si, TSV
- Tall Cu pillar

S-Connect with Molded & Si RDL Bridge





Ultra Fine Pitch Bump Interconnection



Conclusions

- Silicon costs and complexity are forcing a re-evaluation of physical architectures across the industry
- Chiplet-based designs are here now in both MCM and HDFO
- We expect this trend to intensify for 5 nm-3 nm transition
- Amkor is developing a suite of solutions to continue to address and enable this important product/packaging trend: Heterogeneous Packaging

Thank You

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