Glass-Core Substrates for RF Heterogeneous Integrated Packages

Andrew Ketterson. Shuoqi Chen, Rajanish Pandey, Anthony Chiu, Lidia El Bouanani, John Hitt,
Yanghun Yun, Yi Ram Kim, Kevin Anderson, and Kirk Ashby
Qorvo
500 W. Renner Road
Richardson, Texas 75080 USA
Ph: 972-994-3685; Fax: 972-994-8498
Email: andrew.ketterson@qorvo.com

Abstract

Glass-core substrates with low-loss organic build-up layers are an attractive alternative to conventional multi-layer organic laminates and ceramic substrates for millimeter-wave integrated circuit (IC) packages. Under the Department of Defense (DoD) State of the Art (SOTA) Heterogeneous Integrated Packaging (SHIP) Radio Frequency (RF) program, Qorvo and our partners are exploring panel-sized glass-core substrates with fine-pitch multi-layer interconnects on low-loss buildup dielectrics and embedded in-core components for compact RF and mixed-signal microsystems. The suitability of this substrate technology is being evaluated through a series of test vehicles designed to characterize the process capability, RF behavior, and package reliability.

Key words

glass substrates, heterogenous integration, RDL insertion loss, RF multi-chip packages, substrates.

I. Introduction

Perhaps the most important part of any electrical heterogeneous integrated circuit packaging solution is the selection of the substrate technology that facilitates both the 2-D in-plane interconnects and the 3-D vertical interconnects between components. Microsystems that target RF and mixed-signal applications require substrates capable of supporting the low-loss transmission of high-power RF signals and bias voltages (<0.2 dB/mm, >50V) along with high-density chip-to-chip low-voltage digital signals and power (>200 IO/mm, <5V). Substrates based on 1) organic buildup dielectrics and 2) copper interconnects using additive thin-film processes borrowed from the semiconductor industry are the trend today. The design of compact low-loss controlled-impedance transmission lines requires careful trades between size reduction against the need for thicker dielectrics and smooth metal traces with larger cross-sectional areas [1]. This conflict drives the need for dielectric materials with lower dielectric constant (Dk) and dissipation factor (Df) values (Dk <3, Df <0.008). Metal traces with finer lines, spaces, and dimensional tolerances require planar substrates and drive the need for more expensive lithography and via drill capabilities. Achieving this with more cost-effective larger panel and wafer sizes is another part of the trade space and is a challenge especially at lower unit volumes. To this end, as part of the Department of Defense-funded State-of-the-art Heterogeneous Integration Packaging for RF (SHIP-RF) program, Qorvo and our partners are maturing panel-sized glass-core substrates with fine-pitch interconnects on organic buildup dielectrics and embedded in-core components for compact RF and mixed-signal microsystems.

II. Glass-Core Substrate Capabilities

The incumbent substrate technology for high-volume wireless commercial markets (e.g., handsets) is High-Density Interconnect (HDI) organic substrates, an extension of printed circuit board (PCB) substrate technology, consists of laminated “prepreg” layers on either a resin-glass core or more recently in coreless versions. Through improved lithograph and laser drill tools and with additive copper plating processes, HDI substrates allow tighter design rules compared to PCB technology. High-Density Buildup (HDBU) substrates represent an advancement over HDI for some applications. Originally developed for FC-BGA packages used for CPU cores, it replaces the “prepreg” layers with newer composite materials consisting of advanced resins blended with micron and nanometer-sized silica particles for a more homogeneous and planar dielectric capable of finer trace and via dimensions [3]. Material

advancements have focused on reducing the Dk and Df with the newer materials being an excellent choice for RF packaging applications [4], [5]. Replacing the epoxy resin and glass fiber core, a solid glass core with symmetric dielectric buildup layers provides additional dimensional stability and planarity that is essential for high-fidelity lithography. Glass is a good RF material that is available in variety of formats up to large panel sizes [6]– [9]. The coefficient of thermal expansion (CTE) can be tailored for improved reliability, which is especially important with larger body size packages attached to organic PCBs. Importantly, the glass core is an ideal host for embedded active and passive components sandwiched between other components that are flip chip attached to the top and bottom of the substrate. For example, bypass capacitors, power management, acoustic filters, magnetic circulators, photonic waveguides, etc. could all be candidates for embedding into the glass core.

Table I lists the high-level construction capabilities for the current generation of glass-core substrates and the roadmap capabilities for the next generation (ca. 2025). The substrates are fabricated using panel-level processes on 515 x 510 mm^2 glass cores. An aluminosilicate glass was selected with a CTE (7.8 ppm/°C) intermediate between the flip-chip components and PCB based on reliability considerations [10]. The reported Dk and Df of the glass at 30 GHz are 6.9 and 0.044, respectively. The laminate buildup layers that serve as the dielectric for the RF transmission lines have a reported Dk and Df of 3.4 and 0.005, respectively, at 40 GHz.

TABLE I. GLASS-CORE SUBSTRATE CAPABILITIES AND ROADMAP

Item		Today (µm)	ca. 2025 (µm)
Glass Core Thickness		300	220
TGV diameter/Pitch		100/250	60/120
Maximum number of layers		3+2+2 (7)	4+2+2 (8)
Core	Line/Space	25/25	12/12
	Copper Thickness	13	10
	Dielectric Thickness	20	10
	Via/Land Diameter	45/75	30/50
Buildup	Line/Space	10/10	2/2
	Copper Thickness	6	3
	Dielectric Thickness	10	6
	Via/Land Diameter	30/60	10/14

Fig. 1 shows the substrate construction used for our initial evaluations. It consists of two 13-µm-thick copper metal layers on either side of the 300 µm-thick glass core and two 6-µm-thick copper metal build-up layers on each side of substrate for a 2+2+2 stack up. Semi-additive process (SAP) is used to define the traces and laser drilling is used to form the blind microvias. A 15-µm-thick solder resist is used for solder-masked-defined pad openings and an ENEPIG surface finish is applied.

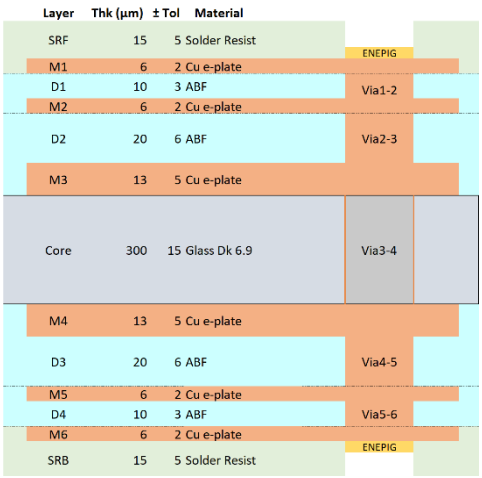


Fig. 1 Glass-core 2+2+2 substrate construction

III. RF Simulation Data

A key part of the glass-core substrate evaluation is the analysis of its suitability for millimeter-wave applications [11]. Various passive RF test structures were designed and simulated using Cadence's AXIEM® electromagnetic 3D solver including different transmission line topologies, intra-layer via transitions and couplers using. Measurement of the test structures will be used to generate models and validate EM simulations supporting future designs. Fig. 2 shows simulated performance from DC to 70 GHz for a microstrip transition between GSG launchers in the top metal layer (M1) to a 1-mm long microstrip in the next metal layer down (M2) with the ground plane provided by M3 that lies just above the glass core. Based on this optimized test structure, insertion losses of 0.13 dB and 0.24 dB at 20 GHz and 50 GHz, respectively, can be achieved with greater than 30 dB return loss up to 55 GHz bandwidth. Overall, compact microstrip transition architectures can be realized by using the selected buildup substrate.

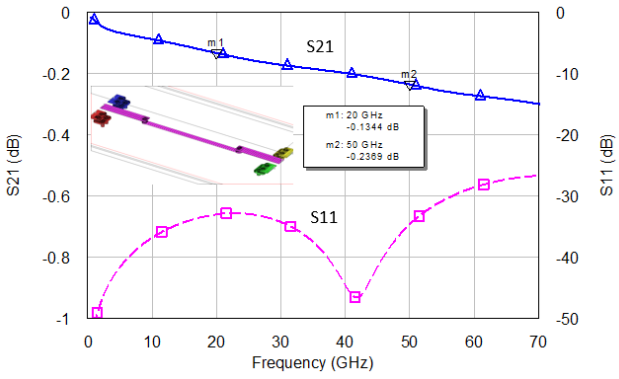


Fig. 2 Microstrip transition performance from M1 GSG launchers to M2 with microvia and 1.0-mm long M2 microstrip trace.

IV. Test and Reliability Plans

Scattering parameter measurements were performed on the RF test structures up to 60 GHz using coplanar RF probes and launchers. The thicknesses of the metal and dielectrics layers were measured from cross sections of a representative substrate and used to adjust the original design simulations to better match the measured data. This was especially important since the fabricated dimensions deviated significantly from the design targets given in Fig. 1.

Daisy chain structures within the substrates include chains of through-glass vias (TGVs) and chains of microvias in the buildup layers. Additional assemblies include daisy chains formed using silicon and GaN-on-SiC flip-chip die with either copper pillars (CuP) or solder bumps (C4) assembled with plastic overmold. The test package interfaces to the PCB are through 0.5-mm pitch BGA balls. Table II shows an overview of the reliability test plan to be completed by the end of Gen-1 phase of the SHIP-RF program expected in December of 2023. This reliability testing will provide information on both the robustness of the CuP or C4 die attach (i.e., die-to-substrate interconnect) as well as the BGA attach (i.e., substrate-to-PCB interconnect).

TABLE II. RELIABILITY TEST PLANS

Item		Notes
Components	Glass-core substrate, 2+2+2	12.25 x 9.25 or 25 x 25 mm^2
	ICP D-Coupon	68 x 14 mm^2 two half coupons
	GaN Daisy Chain Die – CuP	4.74 x 3.63 mm^2
	GaN Daisy Chain Die – CuP	5.93 x 3.896 mm^2
	Si Daisy-Chain– CuP, C4	10 x 10 mm^2
Substrate	Temperature Cycle (TC)	5000 cycles, JESD22-A104F
	Moisture Sensitivity	J-STD-020 MSL3
	Solderability	J-STD-002
	Unbiased-HAST (uHAST)	96 hr., 130C/85%RH 22A118B
	Interconnect Stress Test (IST)	IPC-TM-650 2.6.37A
	Liquid-to-liquid shock	1000 cycles, JESD22-A106B
Package	Monitored TC -55 to 125°C	1000 cycles, JESD22-A104F
	High Temperature Storage	150°C, >1000 hrs.
	Biased-HAST (bHAST)	96 hr., 130C/85%RH
	FC die & BGA ball shear	MIL-STD-883, JESD22-B117A
	Monitored Drop Test	JESD22-B111

V. RF Results

Various RF microstrip (MS), inverse microstrip, stripline (SL), coplanar waveguide (CPW), and conductor backed CPW (CBCPW) transmission lines were designed using different metal layers in the substrate. For example, microstrips using M1 as the signal trace and either M2 or M3 as the ground plane were measured. The off-target layer thicknesses, due to fabrication excursion from the target values, resulted in the measured impedances being lower than the 50 Ω design target. For example, the M1-to-M2 dielectric thickness was 7.7 µm rather than 10 µm. The M1-to-M3 thickness was 29 µm rather than 36 µm target. This prevented us from using our on-substrate designed RF calibration structures that were supposed to de-embed the CPW-to-microstrip transitions, so we used an external off-substrate impedance standard substrate (ISS) for calibrations. Also, due to missing solder resist on several of the RF test structures, M1 traces were plated with nickel in the ENEPIG surface finish resulting in increased conductor losses on those affected transmission lines.

Fig. 3 shows the s-parameters measurements of a microstrip T-line formed between M2 and M3 using ISS calibration and "backfit" simulation data using the measured layer thicknesses and dimensions extracted from measured cross sections. Reasonable agreement between measured and simulated performance was achieved.

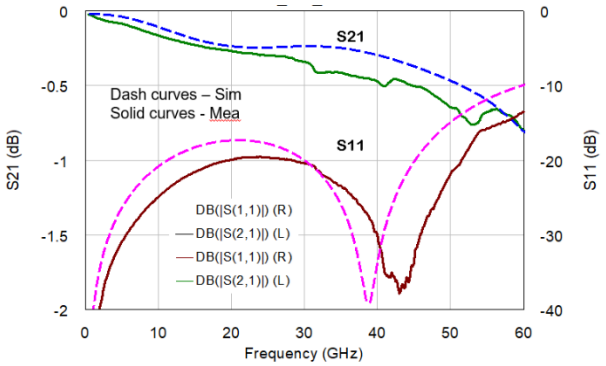


Fig. 3 Comparison of measured and backfit simulations of forward transmission and reflection coefficients of a 1-mm-long microstrip line with a M2 conductor width of 38 µm and a ground plane on M3.

Other transmission-line topologies were likewise measured and simulated to extract the insertion loss (IL) in dB/mm. Table III shows the measured IL at three selected frequency points along with the linewidth (LW) of the signal trace and the ranking (based on insertion loss). The loss of the transitions from probe pads to the start of the T-line (i.e., "launchers"), estimated from simulations, was subtracted from the IL measurements in the table. The effect of the nickel layer in the ENEPIG finish on top of M1 is especially evident in the higher loss of the M1 microstrip lines. Conductor loss of the nominally 6-µm-thick traces dominate the IL.

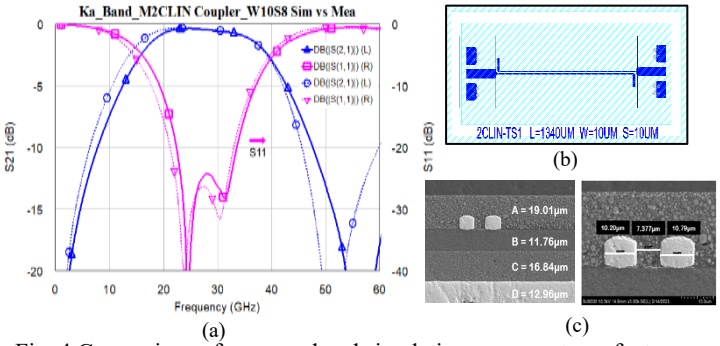
TABLE III. INSERTION OF VARIOUS T-LINES

T-Line Type	LW (µm)	@ 20 GHz IL/mm	@ 20 GHz Rank	@ 35 GHz IL/mm	@ 35 GHz Rank	@ 50 GHz IL/mm	@ 50 GHz Rank
MS M1-M2*	20	0.80	9	1.14	9	1.29	9
MS M1-M3*	100	0.20	5	0.26	4	0.33	1
MS M2-M3	34	0.11	1	0.23	2	0.40	4
Inv-MS M2	14	0.26	7	0.33	7	0.46	6
CBCPW M1-M3	38	0.18	3	0.23	3	0.52	7
CBCPW M2-M3	24	0.15	2	0.29	5	0.43	5
CPW M1	48	0.18	4	0.19	1	0.33	2
CPW M2	18	0.24	6	0.29	6	0.36	3
SL M2	10	0.28	8	0.42	8	0.68	8

* MS M1-M2, MS M1-M3 transmission lines are fully covered with Ni (i.e., ENEPIG).

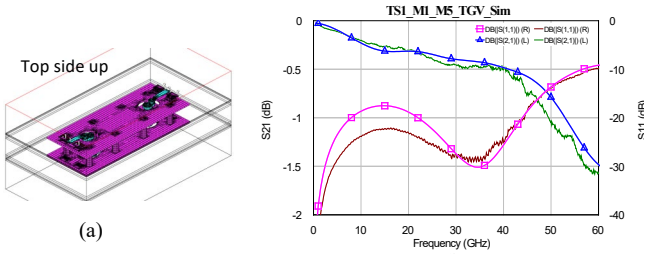
Fig. 4 shows results from a Ka-band RF coupler design consisting of two edge-coupled M1 microstrip lines — 10 µm M1 linewidth, 8 µm gap spacing, and 1.34 mm coupling length vertically separated by ~29 µm-thick dielectric from the M3 ground plane. The measured results show reasonable agreement with the backfit simulations in the band with a slight frequency shift.

Via transitions were studied using a two-port RF through structure with CBCPW-to-MS launcher that connects M1 to a series of blind microvias and TGV to connect to a 1 mm-long embedded MS line on M5 (with M4 ground plane). Fig. 5 shows the measured and simulated (backfit) s-parameter data with a good fit between measured and modeled. To estimate the insertion loss of the via transitions, simulations were used to de-embed the contributions of the launchers and M5 microstrip line. The stack of vias (Via1-2, Via2-3, TGV, and Via4-5) are estimated to contribute 0.07 dB to the insertion loss at 10 GHz increasing to 0.28 dB at 50 GHz.



(a) (b) (c)

Fig. 4 Comparison of measured and simulation s-parameters of a two-line Ka-band microstrip coupler structure (a). Design layout (b) and physical cross sections through the pair of coupled lines (c).



(a) (b)

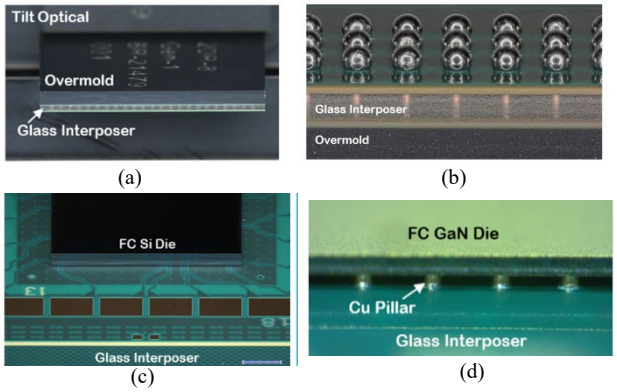
Transition Insertion Loss (dB)	@10 GHz	@30 GHz	@40 GHz	@50 GHz
M1-to-M5 via transition (incl. TGV)	0.072	0.093	0.208	0.279

(c)

Fig. 5 Two-port M1-to-M5 TGV transition test structure (a) measured and simulated (after backfit) s-parameters (b), and table of IL measurements de-embedded to include only the via transitions: Via1-2, Via2-3, TGV, and Via4-5 at four select frequencies (c).

VI. Reliability

As part of the planned Gen-1 reliability activities for these glass-core substrates, various daisy-chains were assembled in 25 x 25 mm^2 body size plastic overmolded BGA packages. Some daisy-chains were formed entirely within the substrate running between M1 and M6 to assess the robustness of the substrate construction. Other chains were formed between PCB and package to assess the BGA interconnects. Still others formed a daisy chain between a 10 x 10 mm^2 silicon die and the substrate (see images in Fig. 6). Packages were assembled onto qualification test boards (QTB) to run the tests shown in Table II.



(a) (b) (c) (d)

Fig. 6 Plastic overmolded 12.25 x 9.25 mm^2 package using a 2+2+2 glass core substrate (a). Plastic overmolded 25 x 25 mm^2 package using a 2+2+2 glass core substrate with Ø300 µm BGA balls (b). Daisy-chains with Si (c) or GaN-on-SiC (d) die with CuP interconnects.

VII. Conclusions

Glass-core substrates with low-loss build-up dielectrics are a promising substrate technology for RF multi-chip packages. Under an advanced technology (AT) effort within the DoD's larger SHIP-RF program, we are exploring such substrates for compact RF and mixed-signal microsystems by evaluating their frequency and reliability performance. Results from Gen-1 test vehicles matched the predicted performance after adjusting the simulations for fabrication deviations in the layer thicknesses from the designed target values. The insertion loss for various transmission line topologies and via transitions was characterized up to 60 GHz and found to be suitable for applications demanding high-performance RF modules. Reliability tests are ongoing and will be reported as part of a subsequent paper including new Gen-2 substrate designs that are currently going into fabrication. Some of the challenges revealed and largely overcome in this Gen-1 work included 1) defect-free unit singulation, 2) delamination of core metal from the glass, 3) precise layer-to-layer thickness control, 4) residue-free microvia drilling, and 5) Cu density balancing within and between layers.

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