Hybrid Bonding for the Next Generation of High-Performance Devices

Laura Mirkarimi

VP of Engineering, 3D Portfolio and Bonding Technology

March 10, 2022

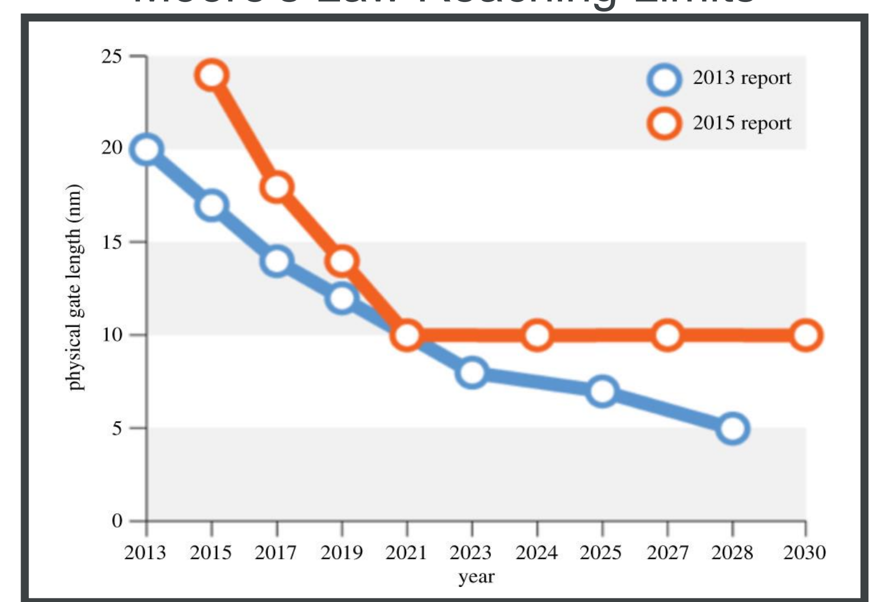
Topics for Discussion

- Market Drivers for Hybrid Bonding
- Direct Bond Interconnect (DBI ®) Description and Value Proposition
- Technology Demonstrations
- Supply Chain Readiness
- Market Adoption of Hybrid Bonding Technology

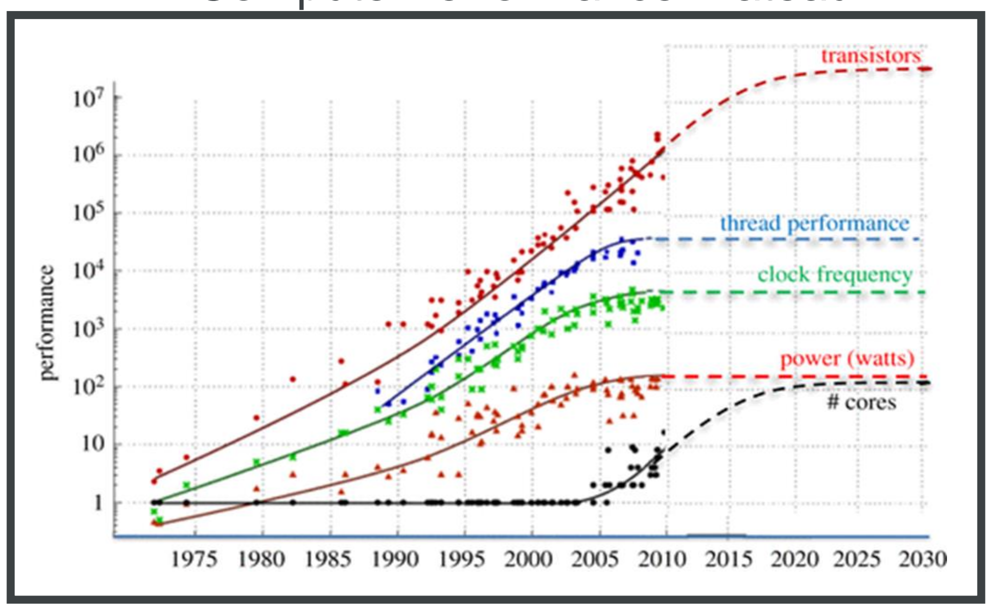
Market Drivers for Technology Adoption of Hybrid Bonding

- More than Moore Revolution
- Chiplet Architectural Concepts for Performance Enhancement and Cost Reduction
- Limitations in Solder Interconnect

Moore’s Law Limit Creates Challenges for Compute Performance



Compute Performance Plateau[1]



What Options Do We Have to Solve This Challenge?

- New Materials for Transistors
- Innovation in Computing Approaches
- **Innovation in Packaging and Chip Architecture**

1. J. Shalf, “The Future of Computing beyond Moore’s Law”, Phil.Trans; R. Soc. A,378:20190061 (Jan. 2020)

L. Mirkarimi, “Hybrid Bonding: Fueling Advanced Memory and High-Performance Compute Roadmaps, ” IMAPS Webinar ; July 2020.

Key Drivers in Heterogeneous Integration

- Disaggregation is distributing functions onto separate wafers or die
- Advantages:
  - Select optimized Si process and nodes for the particular function
  - Shorter time to market improves flexibility to bring innovative products to the market
- Chiplet Library Menu

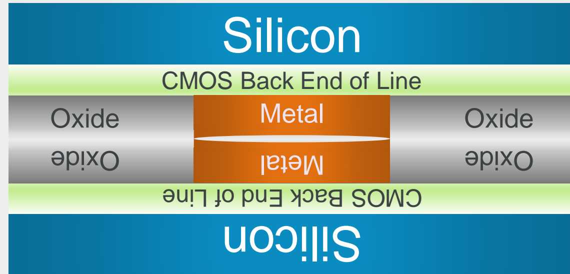
Circuit Function	Cores	Other
SoC	14nm	I/Os
FPGA	10 nm	Thermal Budget
Memory	5 nm	Comms
Accelerator		
Sensor Type		
ASIC		

- Cost savings of 2x with chiplet compared to monolithic
- Higher performance over monolithic
- Mixing and matching would allow economies of scale for many companies.

- Challenges at the package level during Re-aggregation
  - Thermal; electrical; reliability performance
  - Interconnect scalability for highly parallel interconnection requires interconnect scaling

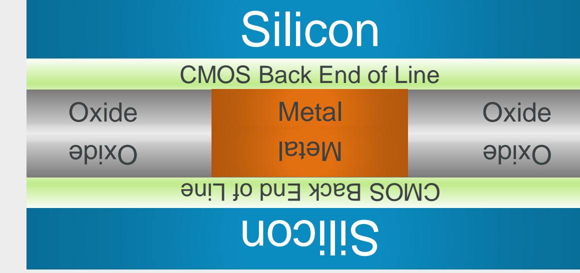
Hybrid Bonding and Direct Bond Interconnect (DBI®)

After Pick/Place



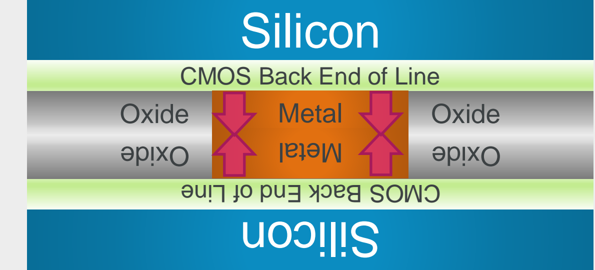
Spontaneous bond between dielectric interface at room temperature

After Heating System



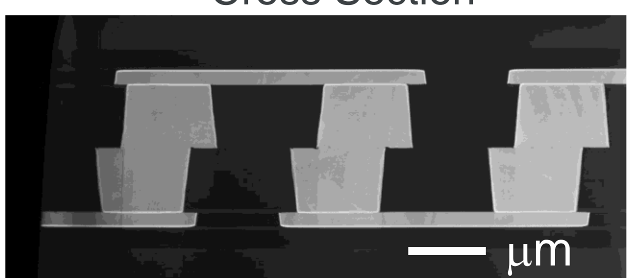
Metal interconnect forms at elevated temperature, but no external pressure

Time at Temperature



Interdiffusion of the metal pads requires time at temperature for metallurgical bond.

Cross Section

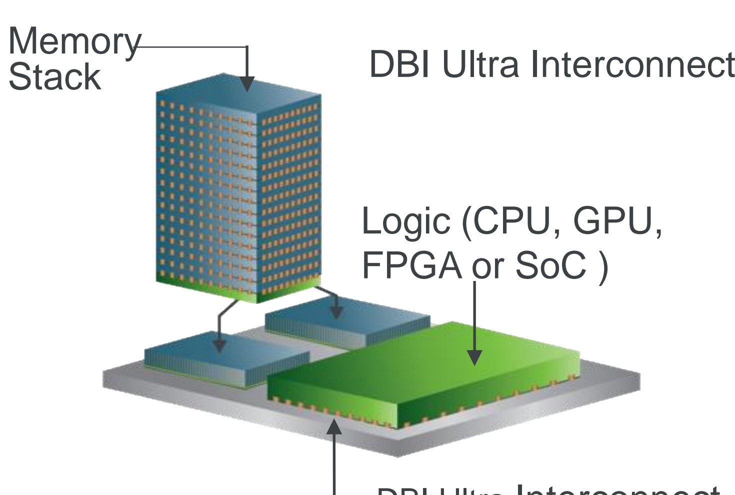


Features

Feature	Value
Bond Metal	Cu, Ni
Bond Pad Size	<1µm to 20µm
Low Temperature	~150 – 400°C
Compatible Dielectrics	Si_xO_y, $Si_xO_yN_z$, $Si_xC_yN_z$

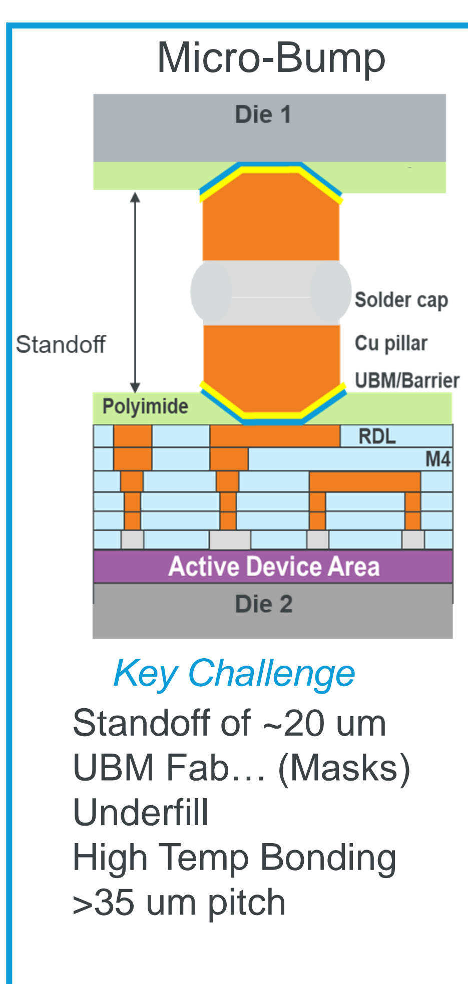
Hybrid Bonding Advantages

Hybrid Bonded Module



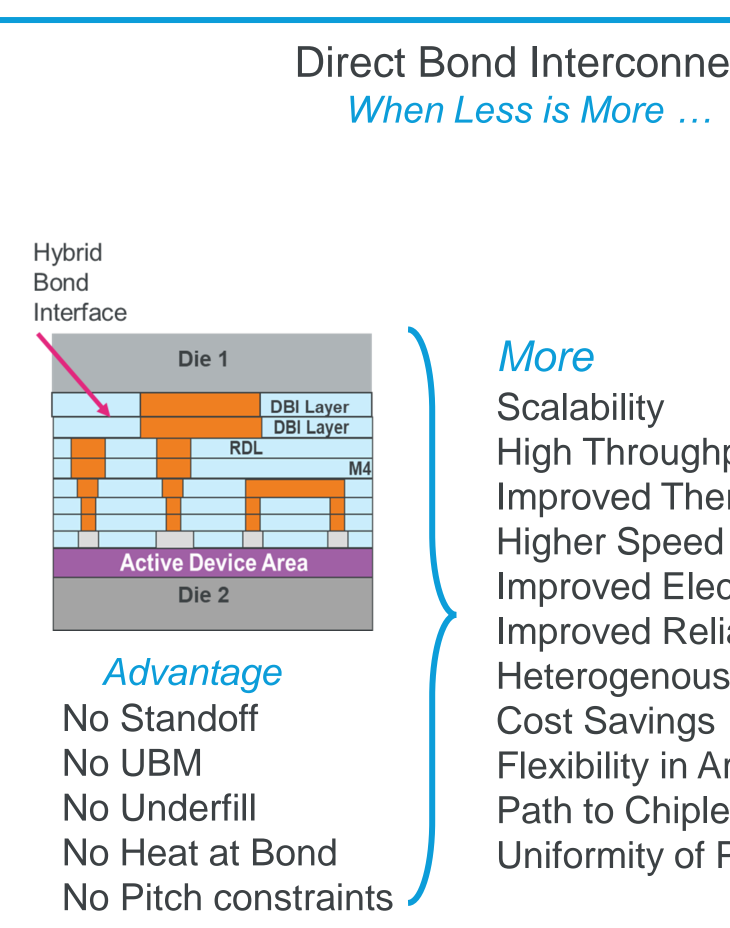
2.5 D / 3D DBI® Ultra
Hybrid Bonding Solutions

Interconnect Comparison



Key Challenge

Standoff of ~20 um
UBM Fab… (Masks)
Underfill
High Temp Bonding
>35 um pitch



Advantage

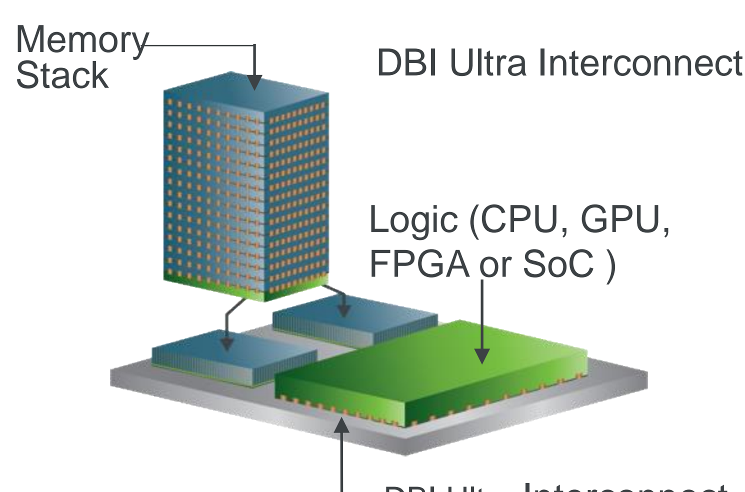
No Standoff
No UBM
No Underfill
No Heat at Bond
No Pitch constraints

More

Scalability
High Throughput Bonding
Improved Thermal Performance
Higher Speed Binning Stacks
Improved Electrical Performance
Improved Reliability and Yield
Heterogenous Integration
Cost Savings
Flexibility in Architecture
Path to Chiplet Proliferation
Uniformity of Packaging Platforms

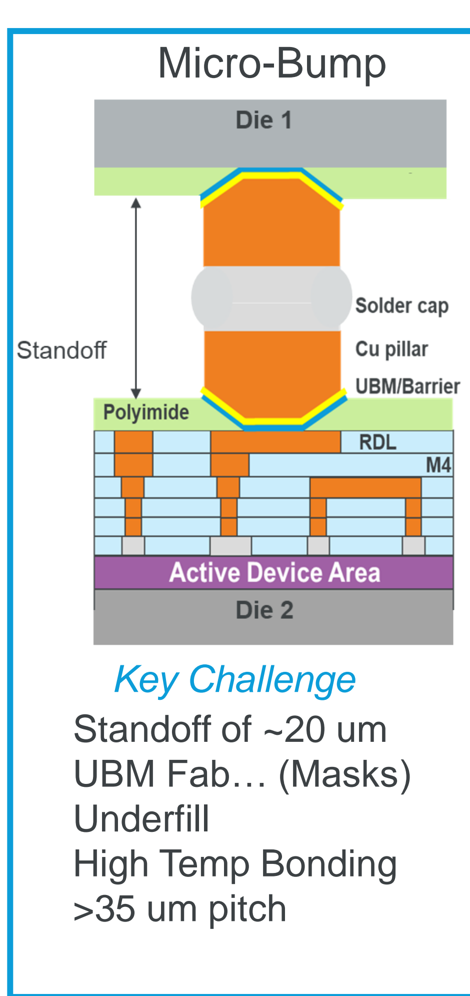
Hybrid Bonding Advantages

Hybrid Bonded Module



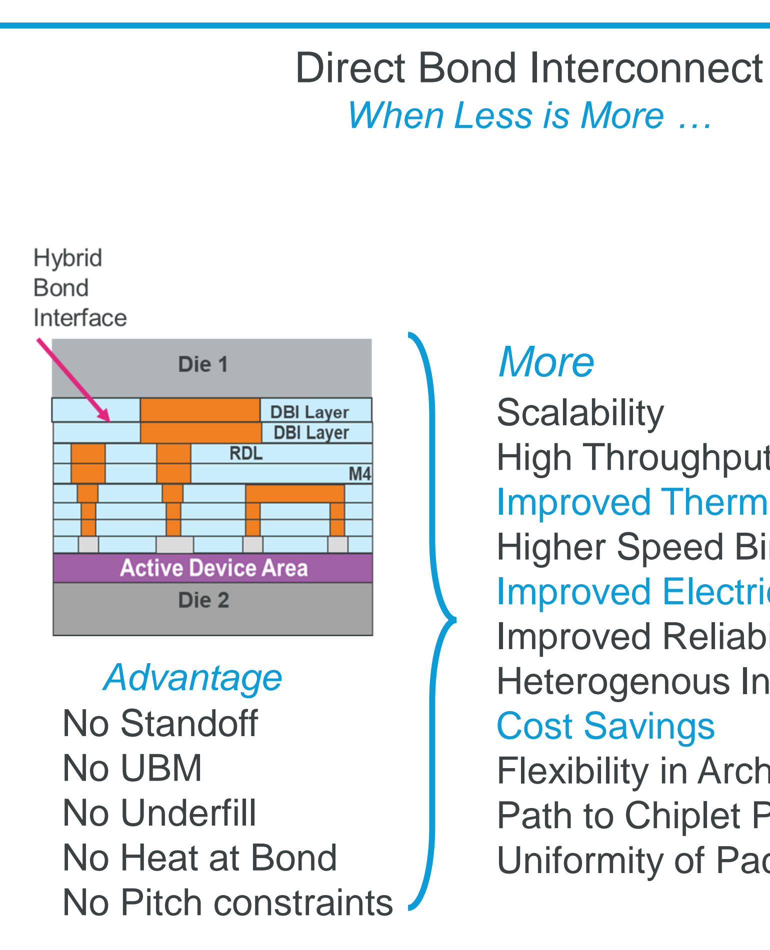
2.5 D / 3D DBI® Ultra
Hybrid Bonding Solutions

Interconnect Comparison



Key Challenge

Standoff of ~20 um
UBM Fab… (Masks)
Underfill
High Temp Bonding
>35 um pitch

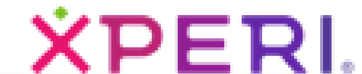


Advantage

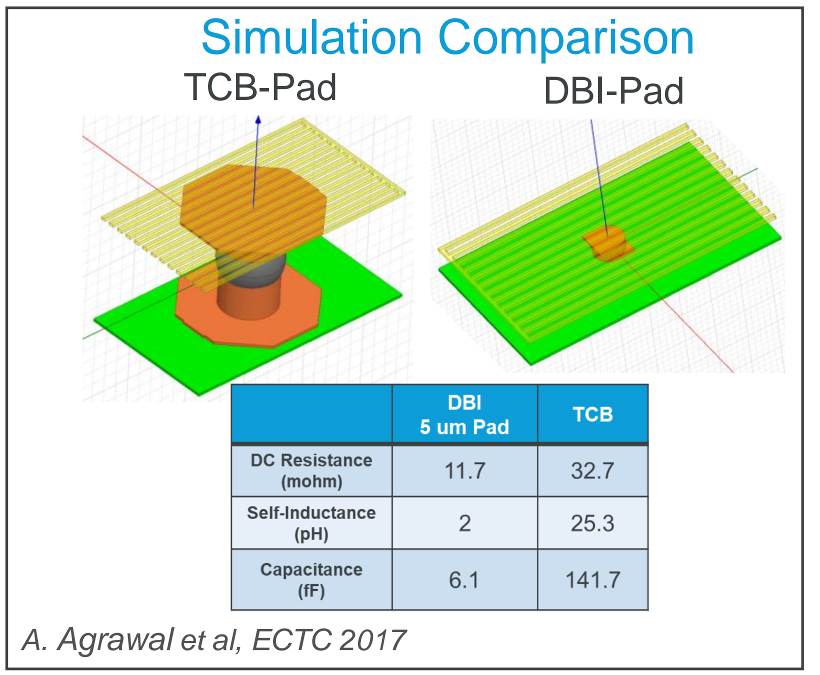
No Standoff
No UBM
No Underfill
No Heat at Bond
No Pitch constraints

More

Scalability
High Throughput Bonding
Improved Thermal Performance
Higher Speed Binning Stacks
Improved Electrical Performance
Improved Reliability and Yield
Heterogenous Integration
Cost Savings
Flexibility in Architecture
Path to Chiplet Proliferation
Uniformity of Packaging Platforms



Enhanced Electrical and Thermal Performance



	DBI 5 um Pad	TCB
DC Resistance (mohm)	11.7	32.7
Self-Inductance (pH)	2	25.3
Capacitance (fF)	6.1	141.7

A. Agrawal et al, ECTC 2017

4-Die Stack Simulation Comparison

TCB-Pad

DBI-Pad

	HBM–4Die Stack		HBM–8Die Stack	
	TCB	DBI	TCB	DBI
	Forced Convection (3m/s); 25°C			
Total Power (W)	10	10	18	18
T_J (°C)	67 ⇨	59	95 ⇨	70
ΔT btwn die(°C)	9 ⇨	1	28 ⇨	4

A. Agrawal et al, ECTC 2017

Design Analysis 2D/3D; Hybrid/TCB

PARAMETER	2D	3D	IMPROVEMENT
Clock period(ns)	4.98	4.98	+0.0%
Total Power(mW)	26.1	20.4	+21.8%
CLK power(mW)	*9.68*	*9.52*	*+1.6%*
Logic power(mW)	*16.4*	*10.8*	*+33.9%*
Area (μm^2)	193,600	174,050	+11%
Routed wire length(mm)	3030	1315	+57%

PARAMETER	2D	IMPROVEMENT OVER 2D		
		HyB	TCB_{noSD}	TCB_{SD}
$Clockperiod(nS)$	5.5	+0.68%	-13%	+0.66%
$Power(mW)$	23.5	+20%	+18%	-103%
$Area(\mu m^2)$	193,600	+10%	-429%	-86%

T. Niguisse et al, " Design Benefits of Hybrid Bonding for 3D Integration"; et al, ECTC 2021

DBI® Interconnect Offers

- 1/50th size of typical TCB pad
  96% less Capacitance (faster)
  64% less Resistance (lower DC power)
  92% less Self-Inductance
- Smaller electrical load; less power

DBI ® Interconnect Advantage in Die Stacks

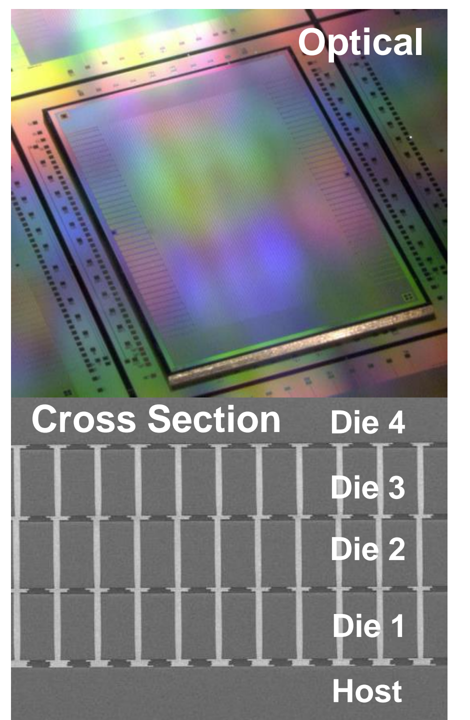
- Tj is reduced by 19- 25 degrees
- Differential Temperature
  - 1 degree for 4 die stack (9x better)
  - 4 degrees for 8 die stack (7x better)

Hybrid Bond Pads 3D Architectural Advantage

- Up to 33% Improvement in Power Reduction
- Up to 10% of an Area Improvement over

DBI® Integration Reduces Process Steps

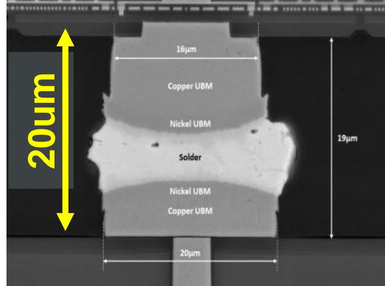
4-Die Stack Test Vehicles



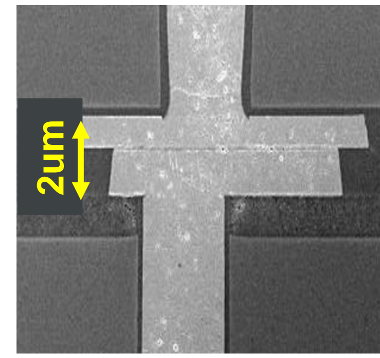
Interconnects:
Face to Face at Die to Host
Face to Back at Die to Die

Die-Wafer Level Process Savings

Solder µBump



DBI



G. Gao et al, ECTC 2020

Module Steps	Frontside Process		TSV Side Processing	
	UBM Solder	DBI	UBM Solder	DBI
1	Passivation opening	Yes	TSV reveal and Planarization	Yes
2	Lithography	Yes	UBM (Adhesion layer, seed layer)	NO
3	Adhesion layer, Cu seed layer	Yes	Lithography	NO
4	Cu electroplating	Yes	Cu electroplating	NO
5	Ni electroplating	NO	Ni electroplating	NO
6	Solder electroplating	NO	Resist strip	NO
7	Resist strip	NO	Wet etch (Cu + adhesion layer)	NO
8	Wet etch (Cu + adhesion layer)	NO		
9	Solder reflow	NO		
10	Cu CMP: NO	Yes		

DBI Module Steps = 5 - 1 CMP = 4
TCB Module Steps = 9

DBI Module Steps = 1
TCB Module Steps = 7

11 Fewer Wafer Process Module Steps for DBI over Solder µBump

DBI® Ultra Direct Bond Interconnect Process Flow Schematic

Die to Wafer Hybrid Bonding

BEOL Cu Damascene	Clean/Dice	Activate	Bond	Anneal

DIE PREPARATION

Metal
Metal Bond Pad
Silicon Wafer

Chemical Mechanical Polishing

Diced Wafer
Tape Frame

Die Activation
Plasma

WAFER 1	CMP	DICING & CLEANING	DIE SURFACE PREPARATION
WAFER 2	CMP	CLEANING	WAFER SURFACE PREPARATION

WAFER PREPARATION

Metal
Metal Bond Pad
Silicon Wafer

Chemical Mechanical Polishing

Wafer

Plasma
Wafer Activation

ROOM TEMPEATURE DIE TO WAFER BONDING

Die Pick
Flip, Align & Bond
Bond
Repeat

LOW TEMPERATURE BATCH ANNEAL

Interconnect

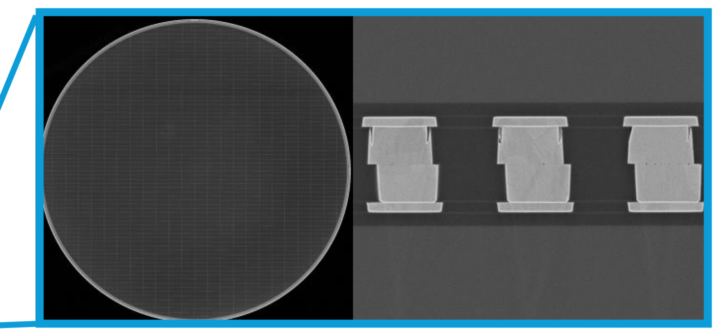
XPERI

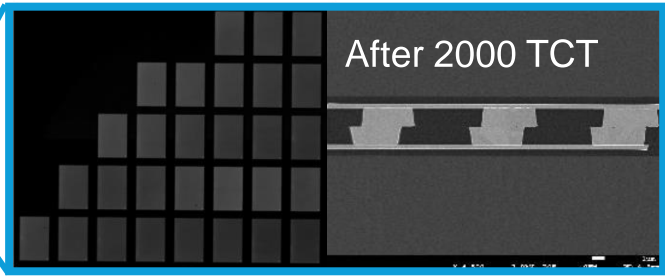
Technology Demonstrations

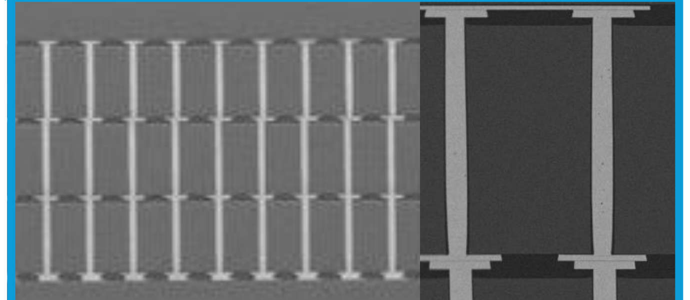
- Build test vehicles to demonstrate the technology capability
- Test structures similar to real applications
  - pad diameter
  - pad pitches
  - die dimensions (x,y, and z)

Validated Hybrid Bonding Technology Demonstrations

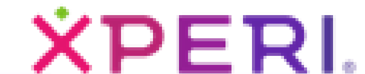
Die Size	# Interconnects in Main Chain of Test Vehicle Circuit	Pad Diameter (mm)	Pad Pitch (mm)	Assembly Technology	IO	Reliability Tests	# Die Stack
4 x 12	>8,000,000	1.2	2.4	wafer to wafer	Face to Face	Not Tested	1
1.9 x 1.9	114,920	1.9	3.8	wafer to wafer	Face to Face	Not Tested	1
8x12	1,600,000	2	4	die to wafer	Face to Face	Planned	1
8x12	31,000	10 ; 5	40	die to wafer	Face to Face	Completed	1
8x12	9480	10	38	die to wafer	Face to Face, Face to Back; TSV to DBI	Completed	5





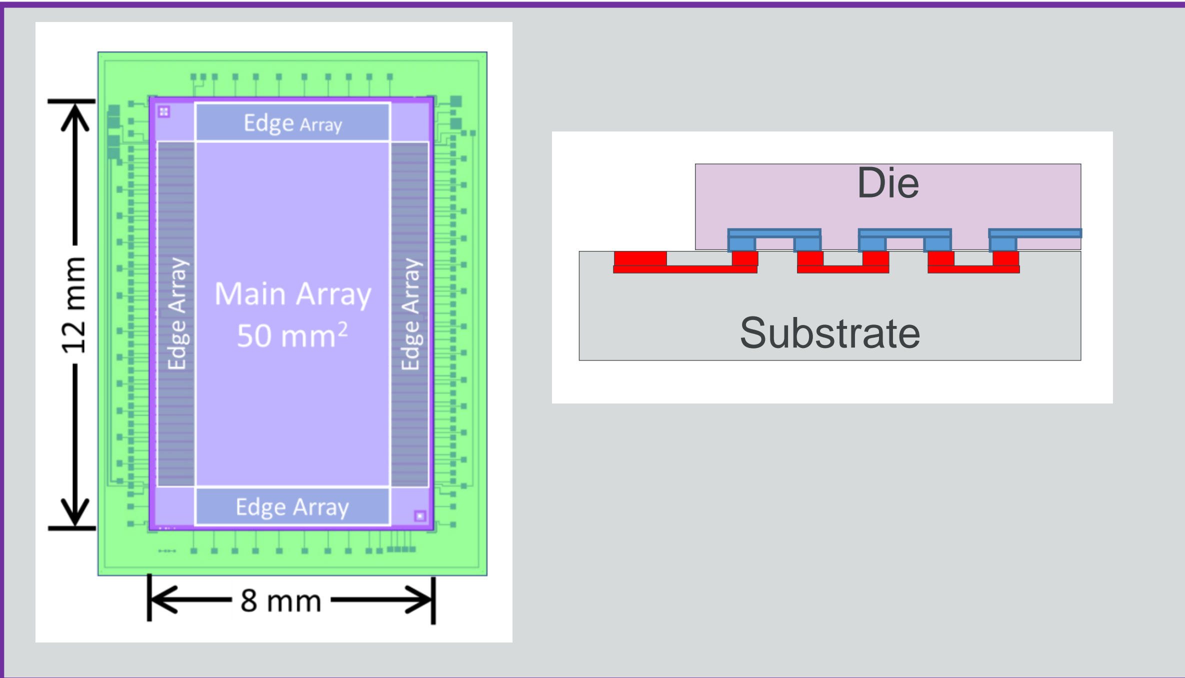


- The size range for a chiplet die (~10mmx10mm)
- DRAM die ~ 8mm x12mm
- TSV pitch ~ 38-40 um
- Logic applications require finer pitch



DBI® Ultra: DBI to DBI and TSV to DBI Memory Test Vehicle Details

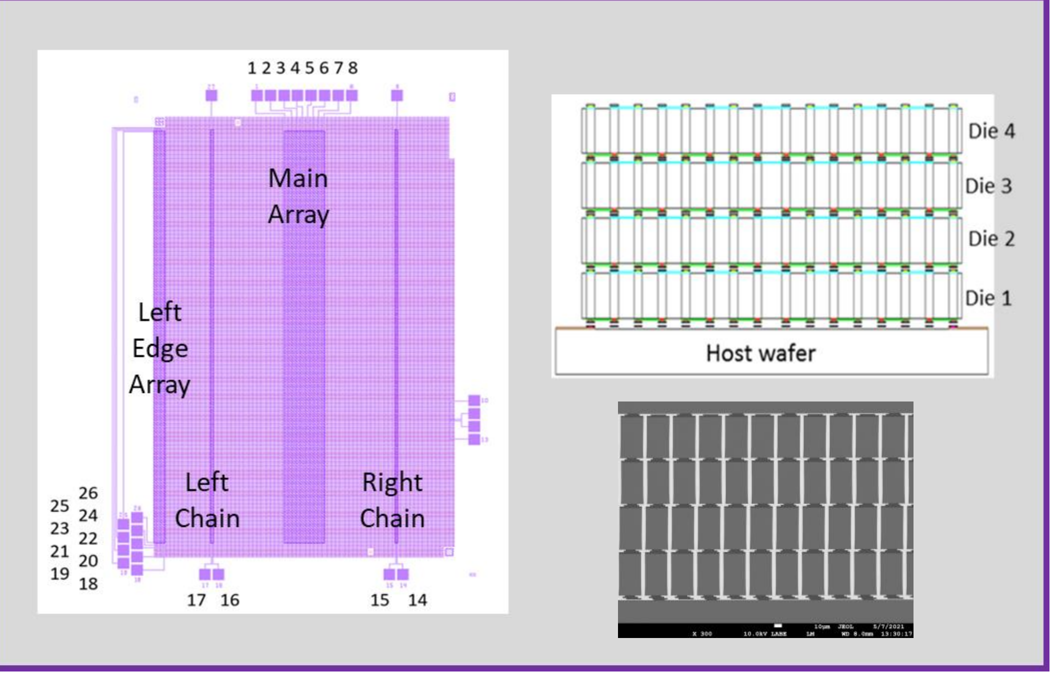
Single Die Stack



- 8 x 12 mm Test Chip
- 2 Layer Metal Pattern: RDL + DBI Bond Pads
- 10 µm pad on 40 µm pitch
- Main Center Array: 50 mm^2 with 31,356 daisy chain links
- Edge Arrays: 3400 – 5000 links, with links within 200 µm of die edge
- Both 200 mm and 300 mm substrates and component die

Tom Workman et al., IMAPS (March 2020)

5- Die Stack with TSV



- Size: 8.0 mm x 12 mm x 50 µm thickness
- TSV: 5 µm diameter on 35 µm pitch / DBI 15um on 35um pitch
- Main Array: 316 x 30 = 9,480 links
- Right & Left Chains: 316 x 2 = 632 links
- Left Edge Array: 316 x 8 = 2,528 links

Fraunhofer IZM

ASSID – All Silicon System Integration Dresden

G. Gao et al, "*ECTC 2021*

DBI® Ultra Interconnect Reliability Performance

	Single Layer DBI		5-die TSV stacked DBI	
Test	Test Condition	Results	Test Condition	Results
Temperature Cycling	-40C to 150C 2000 cycles	Pass	-40C to 125C 2000 cycles	Pass
High Temperature Storage	225C, 2000hrs 275C, 2000hrs	Pass	150C, 2000hr	Pass
Autoclave	121C, 100%RH, 15PSI, 168hrs	Pass	121C, 100%RH, 15PSI, 168hrs	Pass
Moisture Sensitivity MLS3	24hr prebake+30C/60 %RH 192hrs + 3X Reflow	Pass	24hr prebake+30C/60 %RH 192hrs + 3X Reflow	Pass

- Hybrid Bond Interconnect (DBI) is More Reliable than μbump Interconnect:
  - Enhanced Reliability (all Cu interconnect, no underfill)
  - Enhanced Resistance to Electromigration (all Cu interconnect)
  - Dielectric Hermeticity protection (<10^{-11} atm-cc/s)

DBI® Ultra: DBI to DBI Fine Pitch Logic Test Vehicle

Face to Face Fine Pitch Logic TV

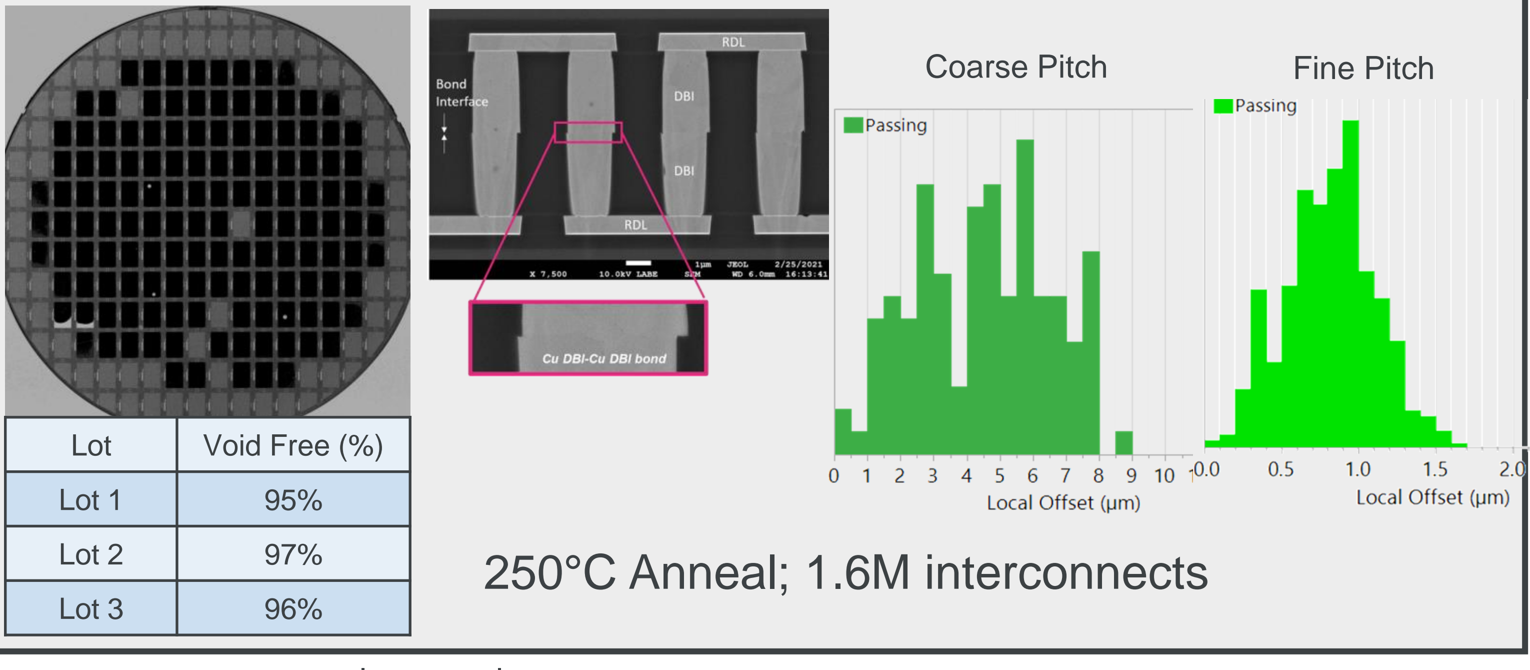
Array	Area (mm^2)	Links	Features
Center Main (DC)	50	1,600k	9 subchains
Top & Bottom (DCT) (DCB)	6	190k	
Left (DCL)	8	250k	2 subchains
Right (DCR)	8	125k +125k	2 subchains intertwined serpentines

DCT
DCL
DC
DCR
DCB
Die
4 µm
Substrate

Tower Semiconductor

- Size: 8 mm x 12 mm
- 2 µm pad on 4 µm pitch
- 5 Daisy Chain Arrays

Experimental Results



Lot	Void Free (%)
Lot 1	95%
Lot 2	97%
Lot 3	96%

T. Workman et al, 2021 IEEE 71st Electronic Components and Technology Conference | Virtual | June 1 – July 4, 2021

- Fine pitch (2 um pad);1.6M interconnects test vehicle yields at 250°C anneal
- High electrical test vehicle yield
  - Even with pad off set of (0.8*Pad Diameter)
  - Similar for both coarse and fine pitch test vehicles

Hybrid Bonding Development Areas in Packaging Industry

- Extending the Die Size Range in Die to Wafer
- Further Reduction of Thermal Budget in Final Anneal
- More Design Flexibility in the Bond Layer Metallization
- Improved Integration for Performance and Cost Reduction

Extending The Hybrid Bonding Technology Demonstration Range

Semiconductor Die Size with Application Space

Heterogenous Integration

LEDs

MEMs

RF, 5G

Lasers

Image Sensors

NAND

DRAM SRAM

3D Chips

Chiplets

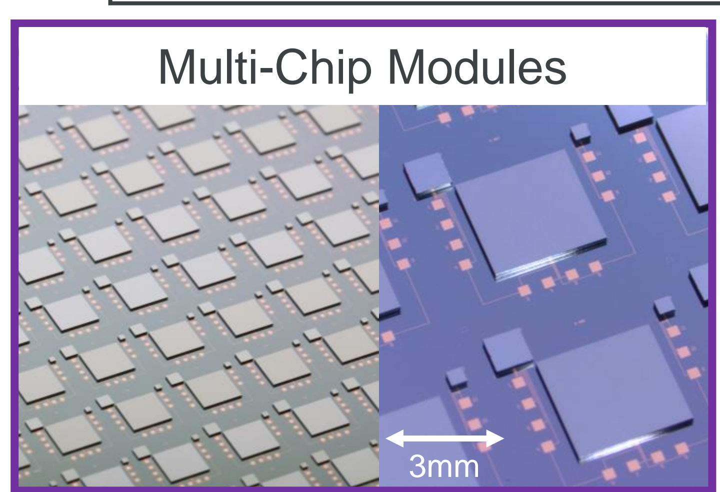
HPC, FPGA

$0.1mm^2$ — $1mm^2$ — $10mm^2$ — $100mm^2$ — $900mm^2$

▲ Feasibility, Yield Reliability

△ Feasibility

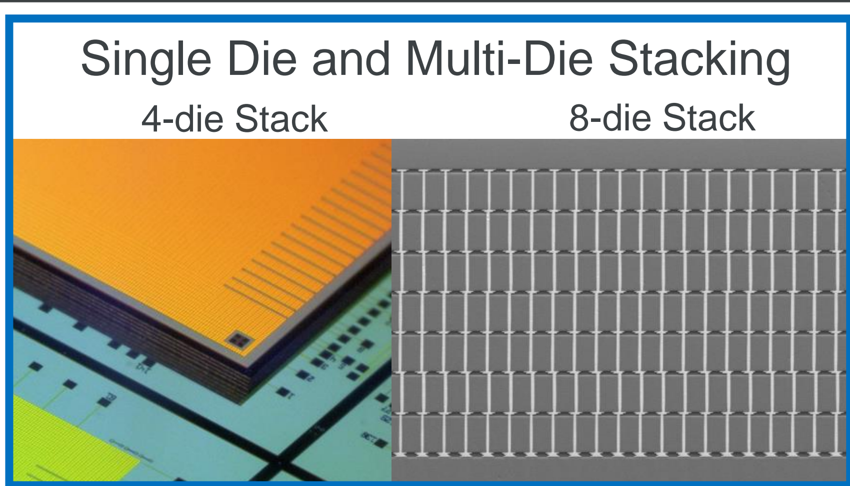
Multi-Chip Modules



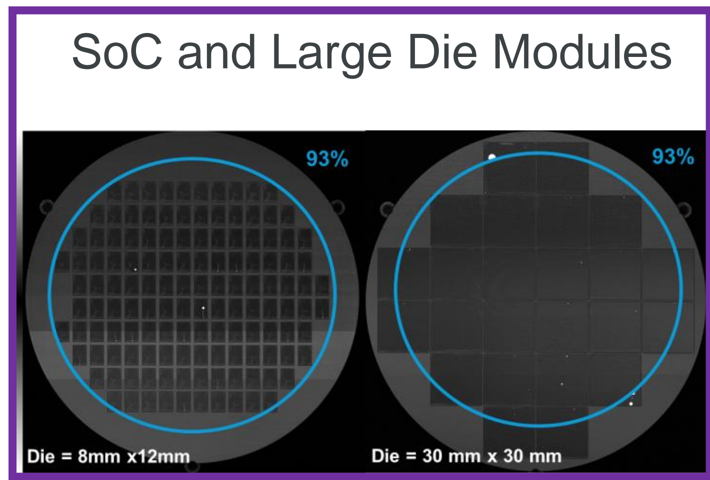
Single Die and Multi-Die Stacking

4-die Stack

8-die Stack



SoC and Large Die Modules



Hybrid Bonding Technology Development Areas

Thermal Budget Reduction

- Prior Demonstrations
  - 250 and 200C
- Industry Wants Lower Temp
  - <200C
- Industry Activity:
  - Cu microstructure
  - Nanotwin Cu [1,2]
  - Alternative options
  - are being investigated[3]

DBI Hybrid Bond Layer Innovation

- DBI Bond Layer Design
  - CMP Improvement[4]
  - Design Flexibility[5]
- Rework: Is it possible?
- BEOL Materials Innovations
  - Dielectrics[6]
    - Cu passivation
  - Metals

Integration Improvements

- Technology adoption will lead to the ability to innovate with integration [7]
- Availability of this platform technology will unleash the imagination of chip architects.
  - Architectural improvements
  - Die to Die

1. M. Liu, et. al., Sci Rep 5, p. 9734, 2015.
2. K.C Shie et al, JMR&T, p. 2332 (2021).
3. L. Mirkarimi et al, ECTC June 2022
4. L Mirkarimi, 3D & Systems Summit, Dresden 2020.
5. Theil et al; ECTC, June 2022
6. Fumihiro Inoue *et al* 2019 *ECS J. Solid State Sci. Technol.* **8** P346
7. Gao et al; ECTC, June 2022

Supply Chain Readiness

- How did we get where we are today?
- Industry Activity

3DIC Hybrid Bonding: R&D Evolution and HVM Timelines

R&D Timeline

1998 | 2000 | 2005 | 2010 | 2015 | DBI® Ultra Launch | 2020-21

1998
- W2W bonding
- (<200º C)
- Heterogeneous mm Wave III-V to AlN

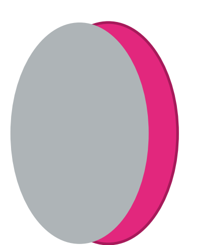
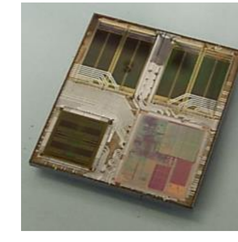
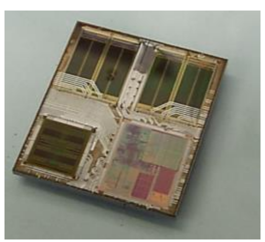
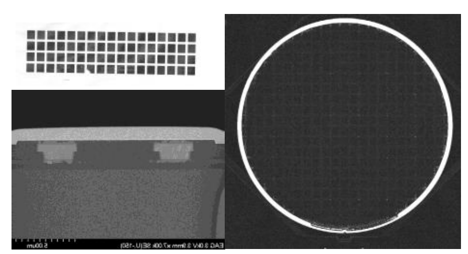
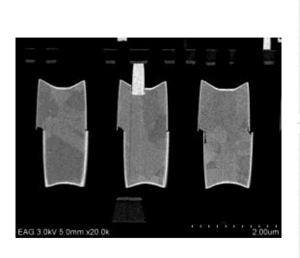
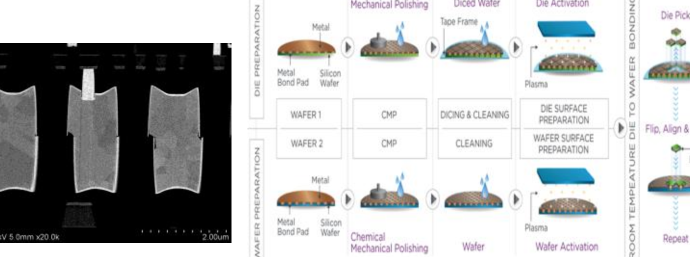
2000
- D2W SiO2-SiO2
- Interconnect-over the edge

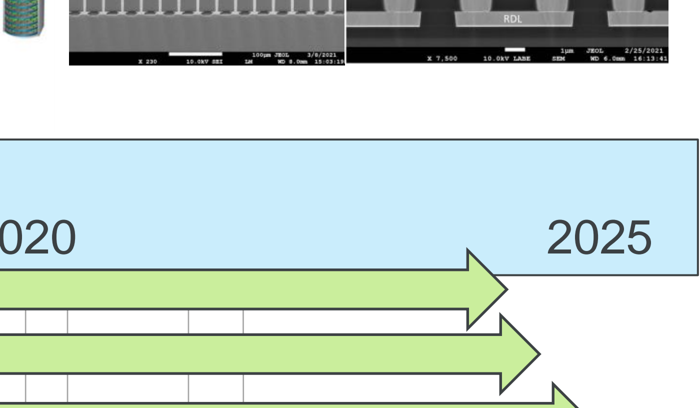
2005
- First DBI D2W
- Ni DBI
- 25um pitch
- W2W Ni DBI

2010
- W2W Cu DBI
- 2 μm pitch

2015
- Cu D2W
- HVM D2W Process

2020-21
- Solving Fundamental Challenges
  - Reliability
  - Stacking
  - Fine Pitch D2W
  - Lower Total Thermal Budgets

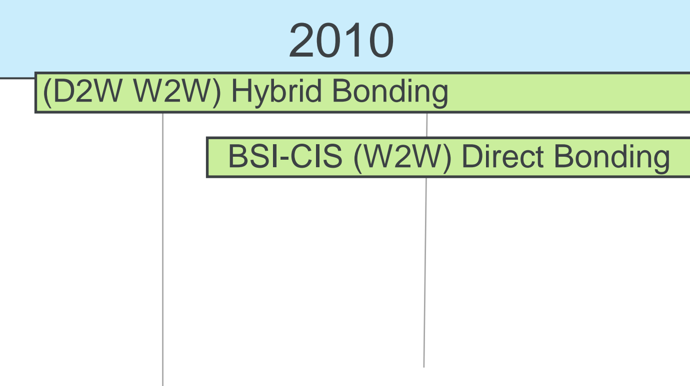









Manufacturing Timeline

2005 | 2010 | 2015 | 2020 | 2025

- (D2W W2W) Hybrid Bonding
- BSI-CIS (W2W) Direct Bonding
- Compute Intensive Modules (2.5 and 3D) (D2W)

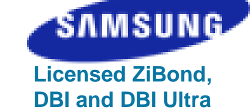


Raytheon
1st DBI Licensee

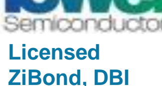
SONY
Licensed ZiBond
CIS market share in 2011 ~ 4%

SONY
Licensed DBI
CIS market share now > 50%

UMC
Licensed ZiBond, DBI and DBI Ultra


SAMSUNG
Licensed ZiBond, DBI and DBI Ultra

SK hynix
Licensed ZiBond, DBI and DBI Ultra


Tower Semiconductor
Licensed ZiBond, DBI

Canon
Licensed DBI

YANGTZE MEMORY
Licensed DBI Portfolio

Micron
Licensed ZiBond, DBI and DBI Ultra

Industry Supply Chain Readiness for Hybrid Bonding

- ✓ Wafer Fabrication Availability
- ✓ Equipment Availability and Manufacturer Roadmap Alignment
- ✓ Availability of Metrology Equipment for Process Control

Xperi Working with Key Equipment Vendors Since 2017

Hybrid Bonding Activity is Increasing in The Industry

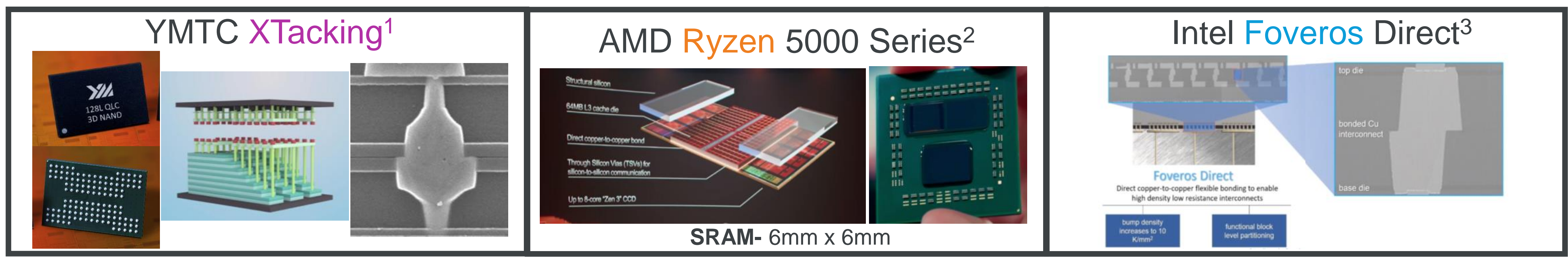
Semiconductors Company Type	Companies with Hybrid Bonding Activity and/or Roadmap
Vertically Integrated	Sony, Samsung, SK Hynix, Micron, YMTC, Intel, Nanya, Kioxia
Foundry Foundry+ Assembly	UMC, TSMC, Samsung, Global Foundries, Tower Semi
Fabless	Omnivision, AMD, Meta, Nvidia, Arm, Xilinx, Google
Government Focused	N'Hanced, Raytheon, Sandia National Labs, Lincoln Labs

Partial list.

Hybrid Bonding Delivering Performance in Next Generation Devices

Hybrid bonding technology is a toolkit enabling the next generation of packaging modules

- *Examples of Widespread Adoption*
  - 1st hybrid-bonded 3D NAND product from YMTC (2020). Wafer to Wafer process.[1]
  - AMD Ryzen 5000 series CPU with Hybrid Bonding at Computex 2021, Enhanced Performance (~12%) with hybrid bonding equivalent to an entire processing node.[2]
  - At Connecting Heterogeneous System Summit, Facebook keynote speaker (Facebook AR/VR realty lab) presented hybrid bonding as critical aspect of AR/VR image sensor for pixel level interconnect.[3]
  - Intel Foveros Direct with an interconnect pitch of 10 um or less to be in production in 2023.[4]



1. Choe, Jeongdong, "YMTC is China's First Mass Producer of 3D NAND Flash Memory", Tech Insights, 13 November 2020.
2. AMD, Lisa Su, "Computex 2021"
3. Facebook, Barbara De Salvo, Connecting Heterogeneous Systems Summit", May 2021.
4. Intel, K. Radhakrishnan; "Connecting Heterogeneous Systems Summit", May, 2021

Summary

- Demonstrated multiple test vehicles with hybrid bonded DBI interconnects have a high yield, enhanced reliability and improved performance over solder μbump.

- Hybrid bonding technology is just beginning to become available in chip to wafer formats in HVM
  - Market adopting at the major pain points
  - Proliferation anticipated across broad segments
  - As more companies access to the DBI toolkit, innovation will follow.

- Hybrid bonding is creating innovation opportunities in SEMI-industry
  - Architecture
  - Materials and Process Integration
  - Assembly Technology
  - Applications and Systems

Thank you for your attention!

Acknowledgements:

Gill Fountain, Thomas Workman, Guilian Gao, Dominik Suwito, Gabe Guevara, Cyprian Uzoh, Bongsub Lee, Jeremy Theil, KM Bang, Michael Huynh, George Hudson, Pawel Mrozek, Abul Nuruzzaman and Richard McClellan

Contact Information: laura.mirkarimi@xperi.com