Development of high performance flip chip ball grid array (FCBGA) packages for automotive application processors

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Abstract

Automobiles have witnessed rapid proliferation of infotainment, driver assistance and autonomous driving features which have led to significant increase in semiconductor content per car. However, this has also required increased integration of device functionality to meet the new automotive requirements for in-vehicle networking, autonomous driving, infotainment, and sensor integration. Advance technology/packages are needed to provide ideal solutions for automotive grade reliability, high electrical performance, and multi-function integration for automotive application processors. To address these requirements, innovative packages including Flip Chip Ball Grid Array (FCBGA) are the potential solutions. In this study FCBGA packages are developed for automotive processor application and qualified for AEC2 qualification tier. To achieve higher performance and reliability, different package substrate materials such as core dielectric and build-up dielectric were evaluated. Mechanical modelling and simulation of package reliability and influence of key material properties such as coefficient of thermal expansion (CTE), modulus of elasticity (E) and glass transition temperature (T_g) was used to provide guidance for the selection of substrate and assembly materials. Developed packages met all the product performance requirements and passed package qual conditions of high temperature storage life (150°C, 500 hours), temperature cycling (-55 °C to 125 °C, 1000 cycles), temperature humidity bias (85 °C, 85% RH, 1000 hours) and board level temperature cycling (-40 °C to 125 °C, 1000 cycles).

Key words

Advanced Packaging, Flip Chip Ball Grid Array, Automotive Grade Reliability, High Performance

I. Introduction

Personal computers demand is declining, mobile, handheld electronics market is maturing and automotive is the next market forecasted for semiconductor industry growth. A significant number of automotive-related innovations are electronics, including automotive engines, safety, and entertainment systems. Advanced Driver Assistance Systems (ADAS), assisted driving, fully autonomous driving are new areas that have created tremendous opportunities for the growth of automotive electronics market. As a result, the semiconductor content in the car is forecasted to increase in the coming years [1].

Traditionally automotive ICs were low lead count, high power wirebond and lead frame based packages that were used in engine control modules to small dashboard applications and sensors. However, due to the increasing complexities, higher performance, pin count, power, requirements of automotive applications, the packaging industry is moving towards high performance packages. Packages like flip chip ball grid array (FCBGA), wafer level fan-out package are now used for automotive infotainment, GPS, and radar applications [2]. However automotive packages must meet quite stringent requirements of performance, reliability, and cost. The package is expected to enable integration of entertainment, communication, navigation, and safety features in the car. Package reliability must also be enhanced to drastically improve the life of electronic products from two years, which is typical in the consumer or mobile market, to more than ten years for the automotive market. In addition, all the high performance, quality, reliability, conditions must be met at a low cost [3].

II. Package Development Details

In this work three different FCBGA packages were

developed; 15x15mm^2 bare die, 21x21mm^2 bare die and 21x21mm^2 lidded. The devices were assembled with 7.4x7.4 mm^2 and 5.5x5.5 mm^2 ultra low-k dies on 21x21 mm^2 and 15x15 mm^2 substrate packages respectively. All the developed packages had 6 layer (2-2-2) build-up laminate stack up. The 21 mm packages had 0.8 mm BGA pitch with 0.5 mm solder balls while the 15mm packages had 0.56 mm pitch with 0.325 mm diameter solder balls. Package cross sections are shown in fig. 1 and the key attributes are summarized in Table 1. Packages used for board level thermal cycling (BL-TC) testing had a daisy chain connection between the substrate routing layers, substrate solder ball and the printed circuit board (PCB). The solder

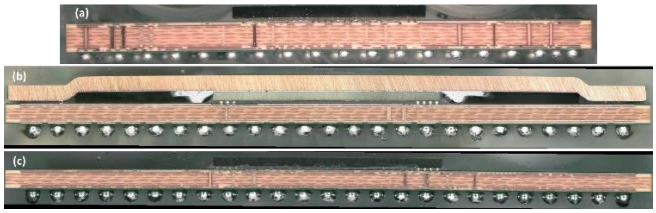


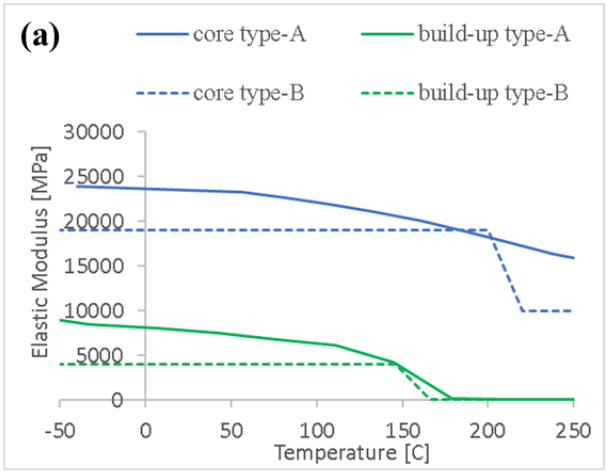
Fig. 1: FCBGA Package cross sections: (a) 15x15mm^2 bare die (b) 21x21mm^2 lidded (c) 21x21mm^2 bare die

Table 1. Key Package Attributes

Package Type	Bare Die FCBGA	Lidded FCBGA	Bare Die FCBGA
Package Size (mm^2)	21x21	21x21	15x15
Die Size (mm)	7.4 x 7.4	7.4 x 7.4	5.5 x 5.5
Ball Count	624	624	388
Ball Pitch (mm)	0.8	0.8	0.56
Ball Size (mm)	0.5	0.5	0.325
Ball Alloy	Sn/Ag3.0/Cu0.5	Sn/Ag3.0/Cu0.5	Sn/Ag4.0/Cu0.5/ Ni0.05/Bi3.0
Substrate Layers	2-2-2	2-2-2	2-2-2
Substrate Thickness (mm)	0.676	0.676	0.876

ball resistance between the package and the board was monitored in situ during BL-TC testing. The PCB for BL-TC reliability was 1.6mm thick, 8L copper and was designed and fabricated by following JEDEC specification of JESD22-B11. Thermal cycling followed JESD22A104D, condition G: -40/+125°C. For package component reliability testing, product packages were used. The 21x21mm^2 package had SnAg3Cu0.5 BGA solder balls, whereas the 15x15mm^2 package had Sn/Ag4.0/Cu0.5/Ni0.05/Bi3.0 solder ball. Usage of Bismuth doped solder alloys improves BL-TC reliability performance. Presence of Bismuth increases the strength of both the bulk solder alloy itself as well as the intermetallic interface layer between the solder joint and metal pad. This results in significant reduction in creep strain energy density or creep strain damage during BL-TC thus increasing the characteristic life [4], [5].

For the 21x21mm^2 package, two sets of substrate materials, were evaluated. First material set consists of core type-A and build up type-A and second material set consists of core type-B and build up type-B dielectric materials. Fig. 2 shows dynamic mechanical analysis (DMA) data for elastic modulus and thermomechanical analysis (TMA) data for coefficient of thermal expansion (CTE) for both the substrate materials set. Material set A has higher modulus and lower CTE in comparison to material set B. In fig. 2 the abrupt change in elastic modulus, CTE value at a specific temperature corresponds to the glass transition temperature (T_g) of the material. As shown in fig. 1, core type-A material has higher glass transition temperature than core type-B material. Build up type-A material also has slightly higher T_g than build up type-B material. Higher modulus, higher T_g, low CTE are favorable properties to reduce package warpage. In packages with cored substrate, the material properties of the core dielectric layer have the most significant impact on the package stiffness and warpage behavior. Other than the different bill of materials, the



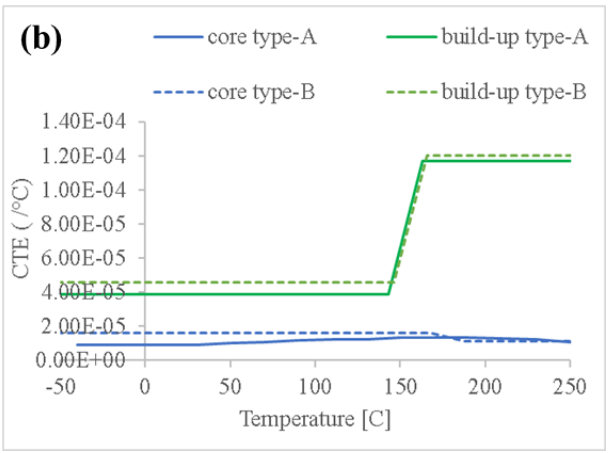


Fig. 2: (a) DMA data for Elastic Modulus for the two substrate stack material combinations, (b) TMA data for CTE for the two substrate stack material combinations performance.

substrates had identical design and layers stack up. The substrates had solder mask defined (SMD) pads and a Cu solder on pad (SOP) finish. The lidded package used a single piece copper lid attached to the substrate with an epoxy material and thermal interface material (TIM) between the die and the lid for improved thermal performance. Both 21x21mm^2 and 15x15mm^2 packages were targeted for automotive grade 2 (AEC2) product applications.

III. Package Warpage Modelling and Measurements

Commercial finite element platform has been used to simulate the electronic-package component level and board level behavior. Fig. 3 (a) shows package cross-section details and fig. 3 (b) shows substrate copper trace details captured in numerical analysis tool via ECAD-to-MCAD mapping procedure and fig. 3 (c) shows die and ball-grid-array layout. In this study, quarter symmetry model has been assumed to reduce computation burden. Table 2 provides the details on the list of constitutive models being used in this study. Component level warpage has been simulated using a typical reflow profile with the stress free reference temperature corresponding to underfill curing temperature (150 °C).

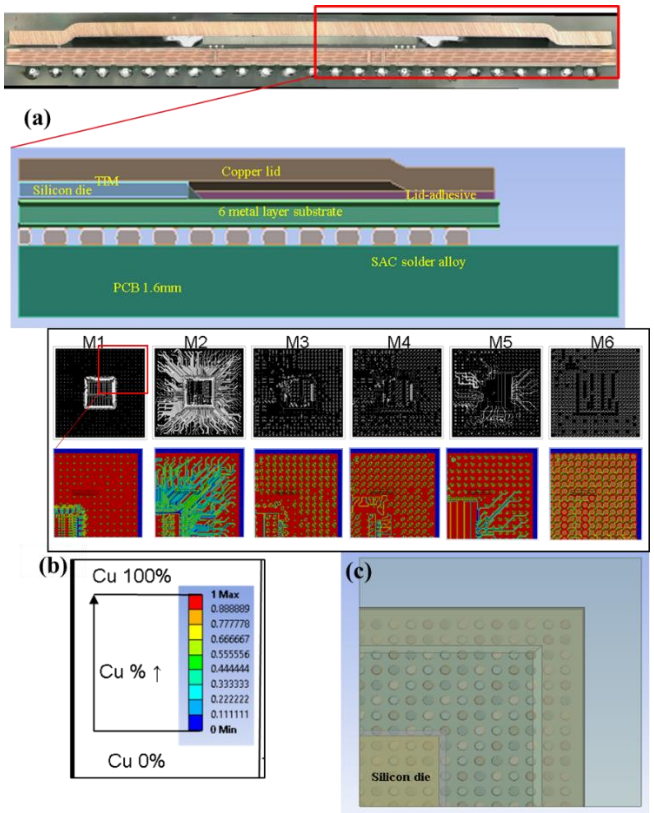


Fig. 3: (a) Model flow with cross-section showing lidded flip chip structure details (b) 6-metal layer substrate with trace layout, metal density details in FEM tool (c) top down view showing silicon die and BGAs Layout

Fig. 4 shows that the package model has reasonably accurate warpage estimation across various temperatures using substrate type-A which has been validated using shadow Moiré empirical data. Fig. 5 and 6 show warpage comparison for 21x21mm^2 bare die and lidded packages with material sets A and B. To assess warpage behavior during the lead free solder reflow process package warpage measurement was done by shadow Moire method for temperature range from 27°C => 260°C => 27°C. To avoid the solder ball coplanarity contribution, the packages for shadow Moire measurement were fabricated without the solder balls. For both bare die and lidded packages, material set A leads to less warpage than material set B over the entire temperature range. For the bare die package, the maximum warpage was reduced by ~30% when using material set A in comparison to material set B. With material set A the maximum package warpage was controlled to less than 100µm. The bare die package has warpage spec of 200µm. For the lidded package ~50% reduction in maximum package warpage can be achieved when using material set A over material set B. The maximum package warpage was controlled to less than 60 µm. The lidded package has a warpage spec of 150µm. Less package warpage is due to better mechanical properties of material set A in comparison to set B like; higher Young's modulus, higher T_g, lower CTE. Package warpage during the solder reflow process is due to the CTE mismatch between the different materials in the package. Silicon has a CTE of ~ 3 x 10^{-6} 1/°C, whereas the core and build up dielectric materials have CTE of ~10-20 x 10^{-6} 1/°C, ~40-45 x 10^{-6} 1/°C respectively. So dielectric materials with low CTE will have less mismatch, thus leading to less warpage. Dielectric with higher modulus and higher T_g values are stiffer and have less warpage deformation due to CTE mismatch induced stress. For both material sets A and B the lidded package shows less warpage than the bare die package. Lidded packages are more rigid and have less deformation, warpage than bare die packages [6]. The electrical properties like dielectric constant, loss tangent were comparable between the two sets

Table 2: List of material constitutive model in this study

Silicon	Temperature dependent linear elastic orthotropic
Bulk copper lid	Temperature dependent linear elastic isotropic
Copper thin film	Temperature dependent linear elastic isotropic
ABF	Temperature dependent linear elastic isotropic
Core	Temperature dependent linear elastic with CTE in-plane and out-of-plane
Underfill	Temperature dependent linear elastic isotropic
Solder	Creep behavior (SAC alloy)
TIM	Temperature dependent linear elastic isotropic
Lid-foot adhesive	Temperature dependent linear elastic isotropic
PCB	Temperature dependent linear elastic orthotropic (lumped property)
C4 bump and underfill region	Temperature dependent linear elastic orthotropic (lumped property)
Solder resist	Temperature dependent linear elastic isotropic

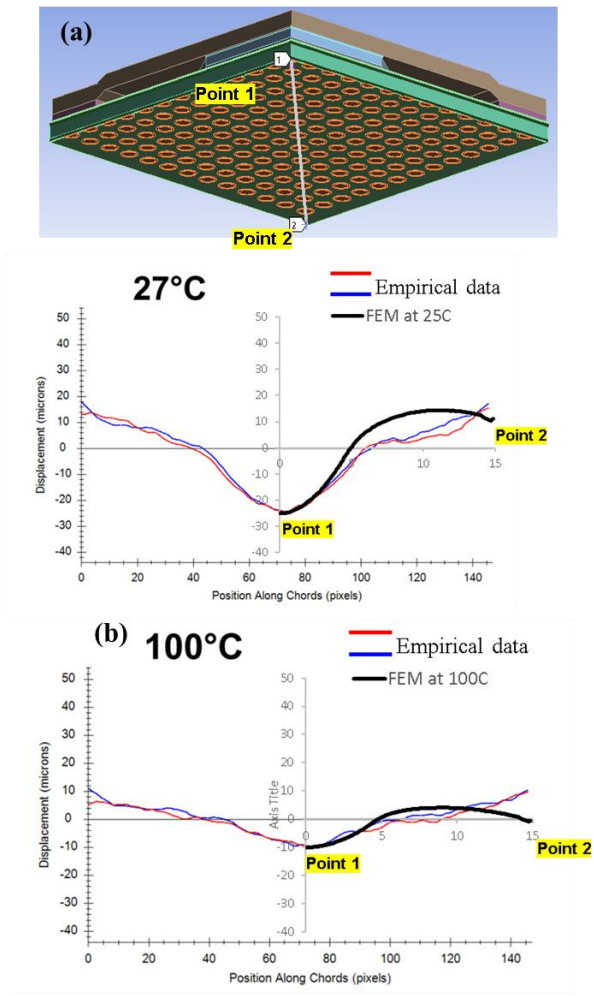


Fig. 4: (a) Warpage path definition on component level (b) component level warpage validation for 27°C, 100°C temperatures using substrate type-A

of materials. Product electrical distribution analysis showed that both material sets have similar functional test performance. Based on warpage assessment results on 21x21mm^2 package, material set A was used as substrate bill of material for the 15x15mm^2 bare die FCBGA package. Fig. 7 shows package warpage data for 15x15mm^2 package. The maximum package warpage was controlled to less than 25µm, against a maximum package warpage spec of 100µm.

IV. Package Reliability Results

Based on the warpage assessment results material set A was chosen as the substrate plan of record material and was used to develop packages that were subjected to reliability stress testing. 21x21 mm^2 package passed reliability stress tests listed in table 3. The package successfully passed AEC2 automotive grade reliability qualification. In addition to product functional testing ion mill construction analysis was

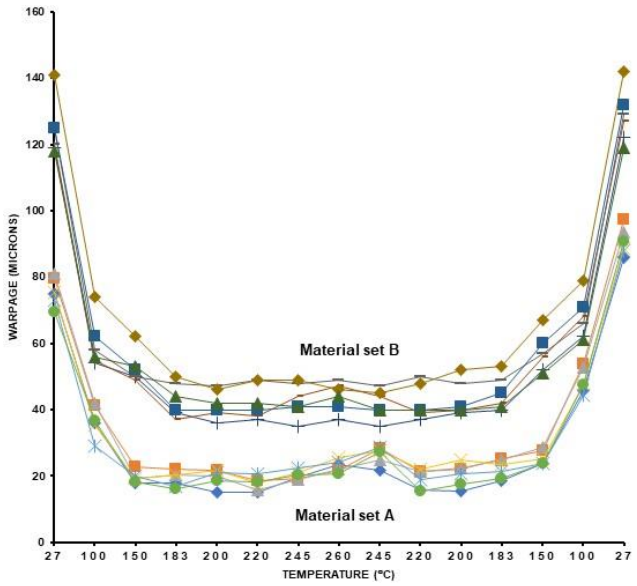


Fig. 5: Package warpage comparison for 21x21mm^2 bare die package with substrate material set A and material set B.

performed on post reliability stress units. Cross section was done on die corner bump locations, shown in fig. 8. Bumps at die corner are chosen as these are bump location with highest package stress during reliability testing [7]. As shown in fig. 9 (a), (b), (c) no material, interface degradation could be found in post TC, HTSL, THB stress units. The developed package not only passed functional testing after the reliability read points but also do not show any potential cracks or failure mode initiation, thus confirming the robustness of the package.

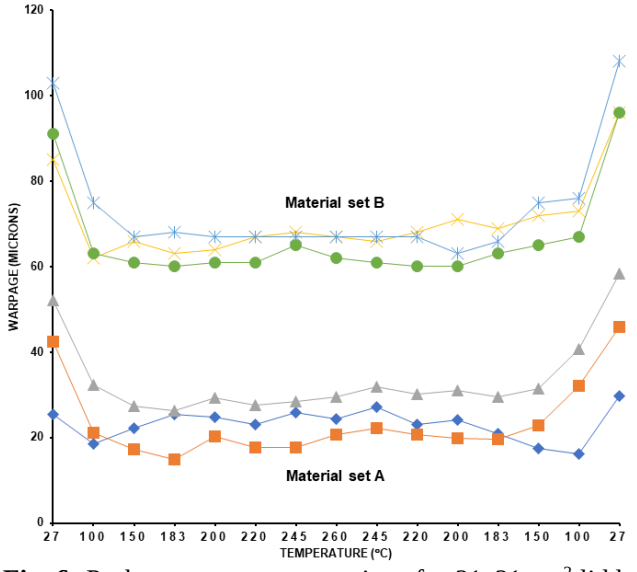


Fig. 6: Package warpage comparison for 21x21mm^2 lidded package with substrate material set A and material set B

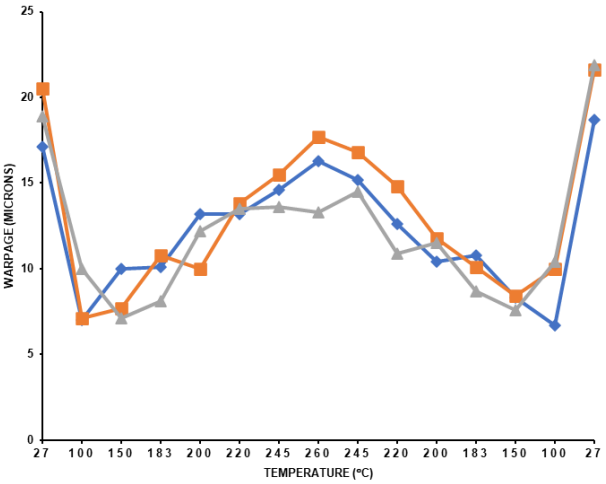


Fig. 7: Shadow Moire package warpage data for 15x15mm^2 bare die FCBGA package.

Table 3: Package and board level reliability qual results for 21x21mm^2 FCBGA package. Package passed AEC2 automotive grade qualification

Test		Condition		Sample Size	Status
Package Level	MSL3	MSL3, 260°C Reflow (3x)	-	2x14	Pass
	Temperature Cycling (TC) after Precon	-55 to 125°C	1000x	3x77	Pass
	High Temperature Storage Life (HTSL)	150°C	500h	3x77	Pass
	Temperature Humidity Bias (THB) after Precon	85°C / 85%RH	1000h	3x77	Pass
	HAST (w/o bias) after Precon	110˚C / 85%RH	264h	3x77	Pass
Board Level	Temperature cycling on board (TCoB)	-40C to 125°C, 1cy/hr	1000x	1x32	Pass

V. Board Level Temperature Cycle (BL-TC) Model and Experimental Reliability

Like component level warpage study, board level solder fatigue study also assumes quarter symmetry model to reduce computation burden. Energy dissipation (i.e., creep work density) per cycle (-40/125 °C) is used as the damage metric [8]. As shown in fig. 10, package with substrate material set A predicts critical joint location underneath the die area. Fig. 11 is the empirical BL-TC data on 21x21mm^2 lidded FCBGA package. First fail is observed at 2894c which, easily passes and exceeds the qual requirement of 1000c no fail. Fig. 12 shows the failure analysis result of first failure. The failed location is at the die corner row as predicted by the model. The failure mode is bulk solder alloy cracking at the package side. The failure mode and location are consistent with reported results in literature for similar FCBGA packages [6]. Additional failure analysis of midlife failure at 3325c showed same failure location and mode as the first failure. Failure analysis on late, end of life fail samples is currently ongoing. Experimental BL-TC reliability was also done on 15x15mm^2 bare die FCBGA, which also passed the 1000c, no fail qual requirement. First failure was observed at 1213c. Failure analysis on the first fail showed that the failure location is at solder bump under

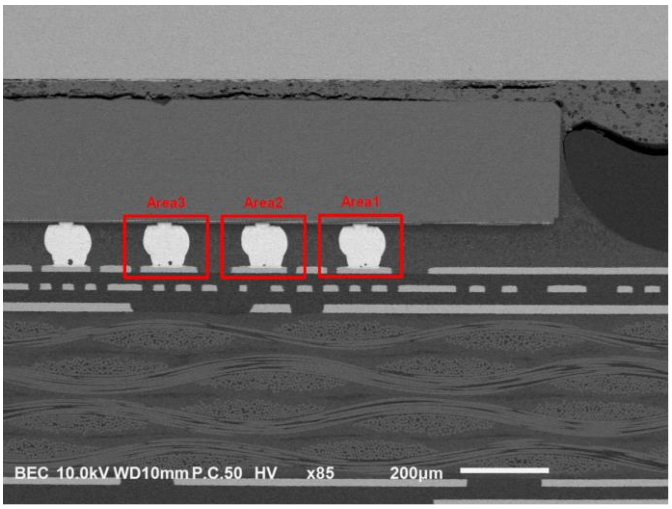


Fig. 8: Die corner row bumps location where ion mill cross section was done after reliability stress.

the die shadow and at bump at die edge. Failure mode is bulk solder failure on package side. The failure mode is same for middle and end of life fails. BL-TC characteristic life

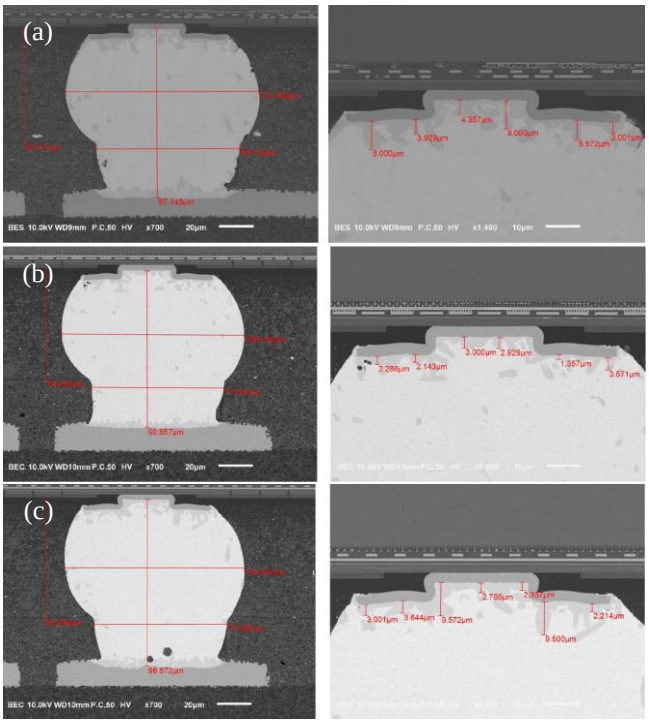


Fig. 9: Ion mill cross section of bump/substrate interface post reliability stresses (a) after TC 1000x (b) after HTSL 1000h (c) after THB 1000h. No material or interface degradation is seen confirming the robustness of the package.

(~63.2% failure) for 21x21mm^2 lidded package was 3570c. The characteristic life for 15x15mm^2 bare die package was 2070c. A smaller package size of 15x15mm^2 should improve

the BL-TC life but was not enough to offset the BL-TC life deterioration due to the smaller solder ball pitch and solder ball size in comparison to the 21x21mm^2 package. Presence of lid also contributes to improvement of the BL-TC life of 21x21mm^2 package. Since during BL-TC the packages were constrained on the PCB, the devices with higher warpage behavior resulted in larger tensile stresses to the solder balls near the center of the package and caused earlier failures. The application of a lid thus reduces package warpage and increases the BL-TC reliability life.

VI. Conclusion

Lidded and bare die FCBGA packages were developed that met and exceeded the reliability qualification requirements for AEC2 automotive grade. Construction analysis on post stress units showed no material degradation or crack initiation, further confirming the robustness of the developed package. Usage of appropriate substrate core and build up dielectric materials leads to significant improvement in package warpage and has a positive contribution to improving BL-TC reliability life. Further work is ongoing on the development and qualification of FCBGA packages for AEC1 automotive grade products.

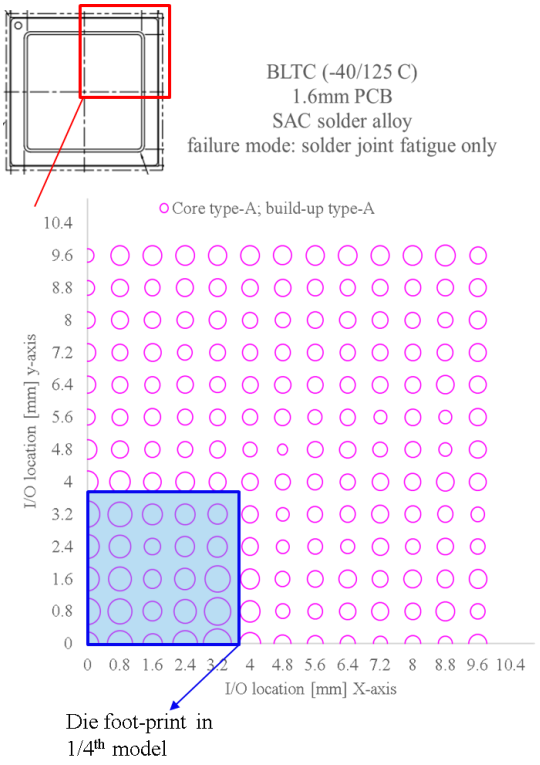


Fig. 10: Solder joint reliability model for 21x21mm^2 lidded package showing energy dissipation per cycle (-40/125°C). Bubble area scales with the solder fatigue damage level using substrate type-A. Solder bumps underneath the die corner are the highest stress locations and expected to fail first.

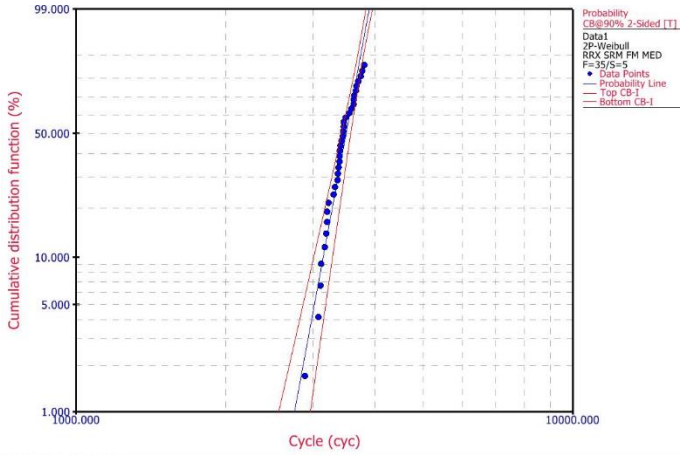


Fig. 11: Board level temperature cycling (BL-TC) Weibull plot for 21x21mm^2 lidded package. First fail = 2894c, characteristic life (~63.2% fail) = 3570c. Passed and exceeded AEC2 automotive grade qual requirement of 1000c zero fail.

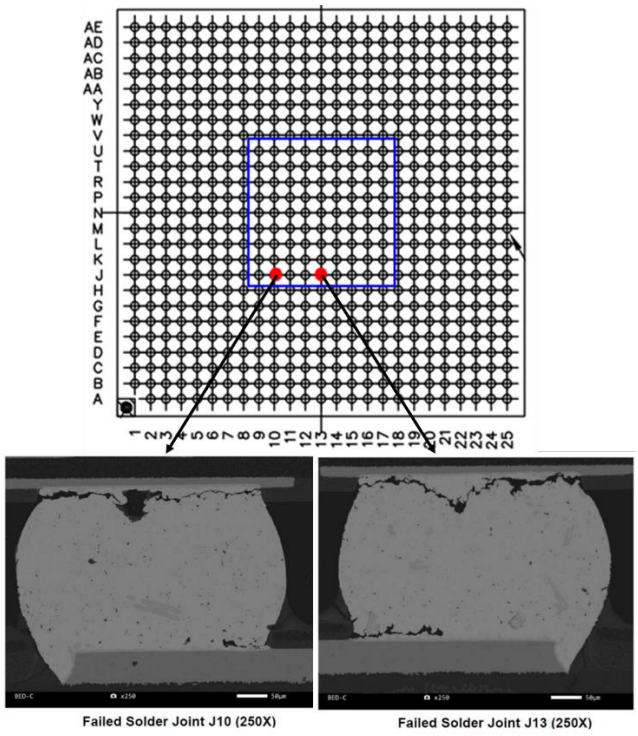


Fig. 12: BL-TC first failure location, bump cross section for 21x21mm^2 lidded package. Location is corner row bumps at the die edge. Failure mode is bulk solder cracking at package side.

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