GE SiC Semiconductor Device Operation at Extreme Temperatures

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Abstract

GE Research has been working on the design, packaging, and testing of SiC Power semiconductors devices at junction temperatures up to 500°C for the past 5 years. Intrinsically, SiC power devices are able to endure and operate reliably at harsh environments. Limiting factors to packaged devices' operation at high temperature are the contact metallization and packaging. While testing bare die power devices, probe contact resistance was found to be an issue for resistance measurements at very high temperatures. On the backside contact, traditional die attach solders have operational temperature limits. Using insulated metal substrates, sintered die attach, and wedge bond interconnect, GE Research tested its power devices up to 500°C junction temperature. GE Research also demonstrated various junction termination dielectric stackups which can block up to 1000V at 500°C junction and show improvements over traditional organic dielectric options (e.g. Epoxy, Silicone, Polyimide).

Keywords

High Temperature, Harsh Environment, Insulation, MOSFET, Power Electronics, Silicon Carbide, 500°C.

I. Introduction

Power devices that can operate at extreme temperatures are a key enabler to power conversion systems that operate in high ambient temperature environments. Applications include but are not limited to inverters and dc/dc converters for aviation, renewable energy, and oil & gas applications. Such systems can enable operation in harsh environment such as aircraft engines, gas turbines, and downhole applications where ambient temperatures can exceed the capabilities of today's commercially available Silicon (Si) and Silicon Carbide (SiC) power devices. Commercially available SiC power devices are typically limited to a 200°C maximum junction temperature. Extending the operating temperature of SiC power devices will enable operation in higher temperature environments while minimizing weight, size, and complexity associated with cooling and thermal management systems.

GE Research has designed and manufactured SiC power devices over the past 15 years. Both SiC MOSFETs and SiC PiN diodes have been fabricated and packaged for use in conventional power electronic converters as discrete parts (i.e. JEDEC plastic packages) or power modules. These parts are typically limited to 200°C junction temperature operation due to packaging limitations. These limitations stem from the use of metals for contacts and dielectrics for terminations and passivations. To achieve the full temperature capability and operation at extreme temperatures of the power semiconductor devices, novel material choices and application techniques are needed.

This paper discusses novel packaging materials for high voltage power device operation and device performance at junction temperatures up to 500°C. GE Research used state of the art devices fabricated at its pilot line cleanroom for this research. The testing reported is well above the rated junction temperature. The purpose of this testing is to demonstrate the device capabilities and shape future research topics based on the obtained results.

II. Device and Packaging Background

Wide Band Gap (WBG) semiconductors have proven that they can function at junction temperatures as high as 800°C with long term demonstrations at 500°C [1]. SiC based power devices require thick dielectric coatings to cover the device termination region where the blocking junction intersects with the device surface. At this region, high electric field strength is present, and it requires a coating thick enough to allow the electric field to drop from near die surface strength levels to values less than the maximum air

dielectric strength. The combination of high junction temperature, high electric field, dielectric thicknesses >100 microns, and mechanical stresses places severe constraints on the selection and application of materials which can support prolonged 500°C+ junction temperature operation.

One approach to achieving 500°C junction temperature operation is to increase the size of the termination region in a semiconductor device. This in turn will enable the devices to achieve desired blocking voltage in air without any dielectric addition. This will however come at the expense of active area reduction for a given sized chip leading to significant derating. A high temperature, high dielectric-withstand material and deposition process are therefore required to achieve the full junction temperature capability of the underlying SiC power semiconductor devices. High junction temperature power devices will enable high temperature and high-power density power conversion systems that are volume and weight constrained.

High junction temperature devices allow a higher case temperature rating, which reduces the performance requirements for thermal management solutions. High reliability power systems often de-rate the devices maximum junction temperature by 50% or more to meet lifetime reliability under system use conditions. To enable systems with higher temperature usage condition, power device qualification test data at increasing junction temperature is needed. This data will provide guidelines to users on the appropriate maximum junction temperature to reliably operate the devices.

III. Baseline Case Study: SiC PiN Diode

Breakdown voltage screening tests revealed that off the shelf TO254 packages are capable of sustaining 1700V at 500°C ambient. The TO254 SiC PiN diode under test used silver die attach (sintered silver capable of high use temperature) followed by aluminum wedgebonds. Prior to testing at high junction temperature, the diode was tested at room temperature (IV characteristics) to ensure proper electrical connections.

After Electro Phoretic Deposition (EPD) coating, the SiC PiN diode was initially tested up to 500°C junction temperature using a Tektronix 370B curve tracer in combination with a hot chuck. A high temperature glass insulated thermocouple was attached using high temperature cement to the TO254 package. The package was found to have a 20°C-30°C lower temperature compared to the chuck setpoint. This was compensated for at the chuck setpoint during the testing. The setup is shown in Figure 1.
The test is comprised of the following items.

- TO 254 ceramic isolated lead packages
- Ceramic insulation on hot probe chuck
- Gold lead clamped to package with a high temperature sealing clip
- Tektronix 370B 2000V capable curve tracer

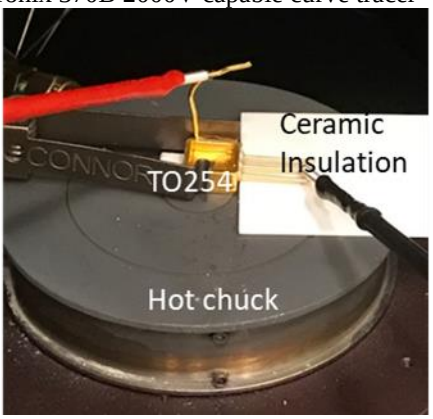

Figure 1. SiC PiN Diode test setup

The SiC PiN diodes showed excellent performance with a forward drop voltage under 5 volts from room temperature to 400°C package temperature. An increase in forward drop was observed at 500°C package temperature due to the degradation of the top metal which increased in the overall on resistance. Three samples were measured with similar performance as shown in Figure 2.

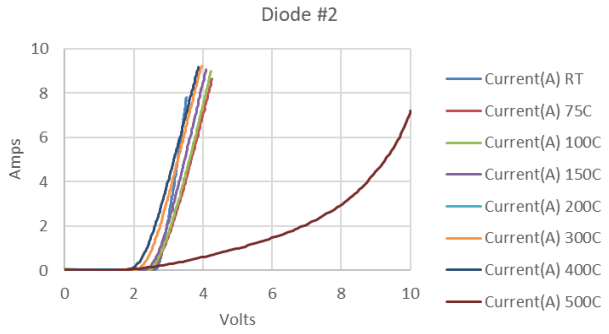

Figure 2. SiC PiN IV Characteristics at room temperature and up to 500°C (2V/div, 2A/div)

IV. SiC PiN Diode Initial Dielectric Testing

Two dielectric candidates were used to coat the SiC PiN diode (capable to 2kV blocking typically in an epoxy molded part). EPD, Silicone Gel, and a control sample (no dielectric) were tested. Figure 3 shows images of these test samples.

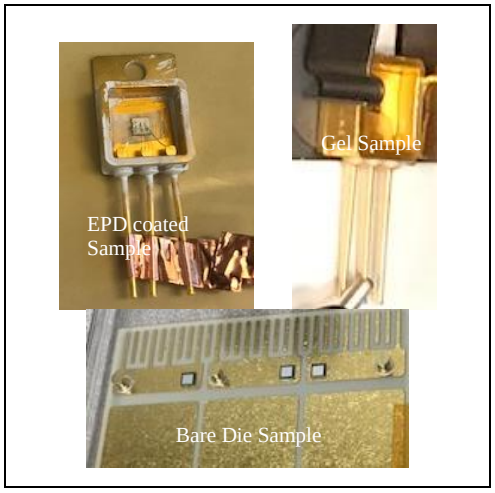

Figure 3. SiC PiN Diode test samples

The TO 254 package with silicone dielectric gel fully covering the die and cavity of the package as shown in Figure 4a was tested to 500°C. Swelling of the gel was observed during testing as shown in Figure 4b. While the part withstood high voltage there were audible arcing events. Excessive bubbling/cracking in the silicone gel was present after test as shown in Figure 4c. The latter highlighted the need for an improved dielectric selection.

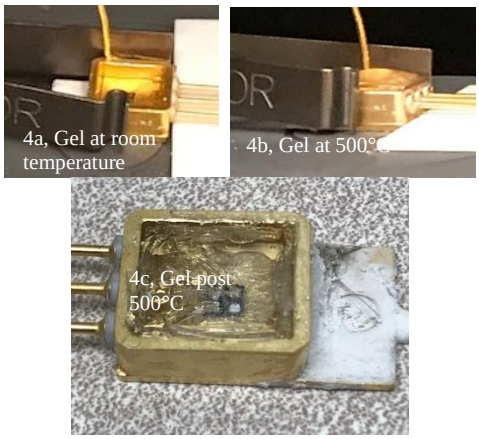

Figure 4a Silicone gel dielectric at room temperature
Figure 4b Silicone gel dielectric at 500°C
Figure 4c Silicone gel dielectric after 500°C

The arcing event was analyzed on the uncoated sample as well as on the sample with no polyimide coating. The arcing damage was found in the device termination region. During testing it was unavoidable to damage a part with a weak dielectric. When the arcover occurs, it usually causes permanent damage to the device. This was an expected result based on electrical field modeling of the device. Arcing damage in the termination is shown in Figure 5.

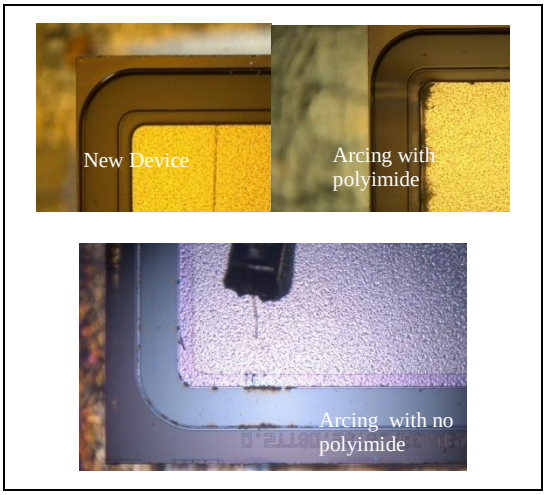

Figure 5. A new device (Top Left), Arcing damage across polyimide (top right), and Arcing damage with no polyimide (bottom)

GE Research investigated EPD which is an organic/inorganic coating. The EPD provides a coating on all surfaces post wire bonding and can be applied on large areas. Since the EPD uses electrical potential during deposition, the electrically isolated regions of the chip or substrate may not be sufficiently coated. This however was not an issue since the feature sizes of the insulated areas being studied were relatively small compared to the coated area. The EPD thickness was approximately 50 microns. The coating was masked by the wirebonds in some regions where the wire loop height was close to the chip surface. Additional optimization of the assembly and coating may be realized with EPD.

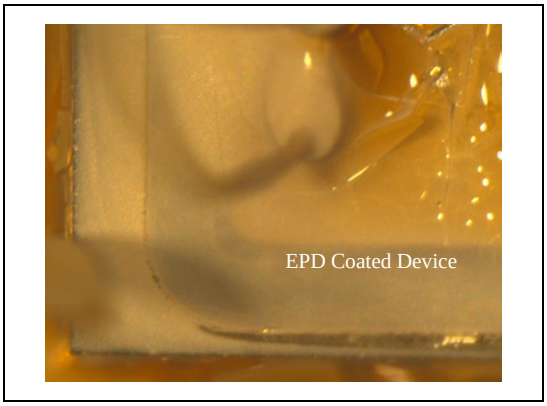

Figure 6. Close up of EPD coated device

GE Research also down selected an inorganic ceramic adhesive. There are a variety of ceramic adhesives available

for extremely high temperate use. The electrical and material properties vary widely for these materials. GE Research selected an electrically insulating material with a dielectric strength of approximately 10kV/mm. This is lower than organic encapsulation materials which typically have 15kV/mm to 30kV/mm dielectric strength. The mechanical performance of the ceramic adhesive is also key to enduring thermal cycles. GE selected a low Coefficient of Thermal Expansion (CTE) ceramic adhesive with a 7.2 in/in/ºC ×10-⁶ which is slightly higher than SiC CTE, hence minimizing mismatch. Of all the ceramic adhesive candidates tested the alumina phosphate chemistry provided the best performance. GE Research focused on the proper ceramic adhesive material application following the manufacturer's curing schedule. The microstructure or phase of the ceramic post cure was not examined.

GE Research studied the use of the ceramic adhesives in SiC power device packaging and found that when applied in large volumes it would either outgas during the dry out phase in curing or crack during curing or testing as shown in Figure7. GE Research reduced the applied volume to insulate just the device top area and then tightly control the mixing, deposition, and cure process. This resulted in bubble and crack free assemblies that endured four hours under test with high temperature excursions up to 500°C junction temperature as shown in Figure 8. Similar cracking and defects during potting with ceramic adhesives with large volumes have been reported in [2-3].

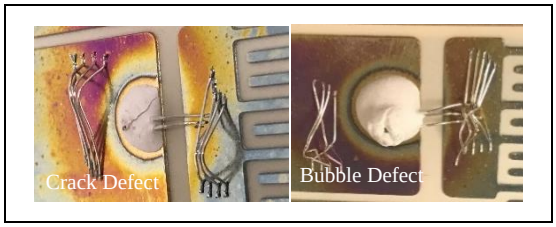

Figure 7. Large volume ceramic adhesive with cracking or bubble defect

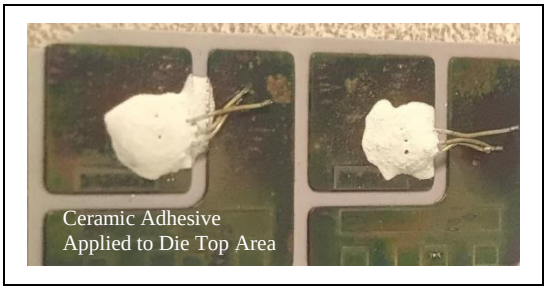

Figure 8. Well cured ceramic phosphate/alumina coating with low voiding or cracking after ~4 hours aging at 500°C

V. SiC PiN Diode High Voltage Testing

The SiC PiN Diodes were tested with various insulation materials applied to the top area of the device at 500ºC junction temperature. The devices under test are rated to 2kV blocking voltage in standard packaging materials such as plastic overmold. It was found that the silicone gel sample performed well but is severely degraded after initial testing. The EPD performed well on the first sample tested, however this performance could not be reproduced in subsequent samples. EPD was tested with and without polyimide on the device termination. The fully inorganic Alumina Phosphate coating on a device top area (including termination) with no polyimide on the termination performed well with no permanent damage during high blocking voltage (600V-1050V) testing at 500ºC junction temperature. It was noted that with EPD or Alumina Phosphate coating the blocking voltage capability was reduced by half or more. This is due to the lower dielectric strength of these insulating materials. The results are summarized in Table 1.

Test	Stripped Polyimide	Silicone GEL over Polyimide	EPD over Polyimide	EPD	Phosphate Alumina
Blocking Voltage at 500C	600-750V	1000V	925V, not repeated	Low voltage arcing	600V-1050V
Visual Inspection	Degraded surface	Highly degraded bubbled	No visible issue on surface	No visible issue on surface	No visible issue on surface
Organic/ Inorganic	Inorganic	Organic	Inorganic/ Organic	Inorganic/ Organic	Inorganic
Performance	Low	Low	Medium	Low	High

Table 1. SiC high voltage testing of blocking at 500ºC

VI. SiC MOSFET Testing

GE 1.2kV SiC MOSFETs were evaluated at high junction temperature. A metal insulating substrate with a copper nickel gold surface finish was used. Aluminum wedgebonds were used to connect the gate and source pads to the substrate. Aluminum wedgebond loops were used as test points. The SiC MOSFET test sample is shown in Figure 9.

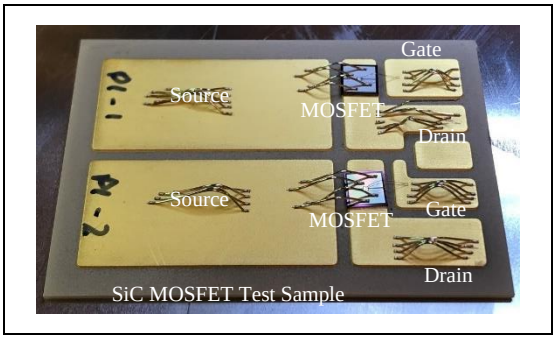

Figure 9. SiC MOSFET test sample

A high temperature hotplate (540°C capable), curve tracer, and Kelvin connections were used to test the MOSFET test

sample. The surface temperature of the sample was characterized with a thin thermocouple probe to ensure accurate temperature readings. The advantage of this setup over a traditional probe station is that drain to source current can be driven higher given the larger diameter wedgebond connection. In addition, this setup allows for the direct application of the dielectric on the device top area. The test setup is shown in Figure 10.

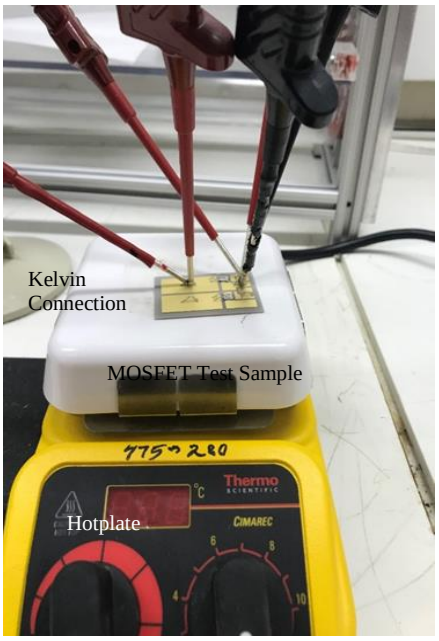

Figure 10. SiC MOSFET test setup

After testing at high junction temperature over 350ºC the sample was discolored. Figure 11 shows a typical appearance after testing to over 350ºC.

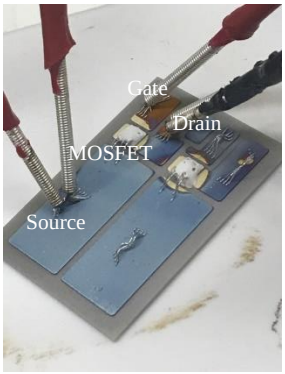

Figure 11. SiC MOSFET after thermal testing

The device current rating depends on the drain to source on-resistance (R_{dson}) and the thermal resistance junction to case (R_{thj-c}). R_{dson} was evaluated from room temperature to 370ºC. The device was measured multiple times with repeatable results. The R_{dson} was tested with a +20V gate bias. There was approximately 20 minutes of ramp time to 370ºC. The sample endured 10's of cycles but the interconnect eventually broke. This is due in part to the aluminum die metallization which is not designed for this extreme temperature range. The repeatable on resistance curves are shown in Figure 12.

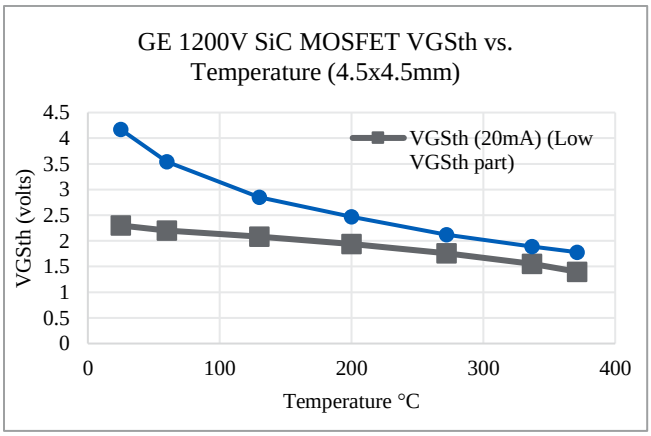

Figure 12. SiC MOSFET R_{dson} vs. Temperature

The blocking voltage and leakage current (IDSS) was measured to determine high voltage performance at 500V up to 370°C. The leakage was found to increase with increasing junction temperature. Figure 13 shows the result. The blue curve below shows results with 0 Volts gate bias voltage. When -10V gate bias was applied the IDSS was reduced to 13µA shown by the grey point. After the gate bias was returned to 0V the device Drain to Source junction was shorted. This indicated a gate stability issue causing the device to turn on with 0 volts gate bias.

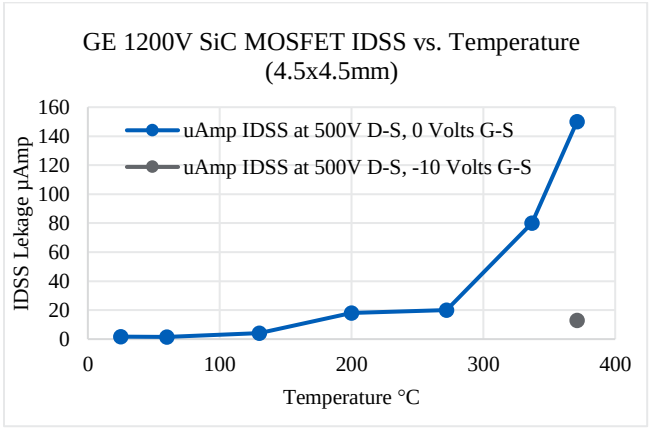

Figure 13. SiC MOSFET IDSS leakage at 500V

Given the stability issue just discovered, various SiC MOSFET samples with different gate to source threshold

voltages were tested. This was done to understand if a higher threshold voltage device could be used to improved high junction temperature operation. If the threshold voltage decreases due to a junction temperature dependance or there is a threshold stability issue the device may no longer be normally off and may spuriously turn on. GE Research found that higher starting threshold voltage parts maintained a higher voltage margin in threshold voltage compared to lower threshold voltage parts as shown in Figure 14.

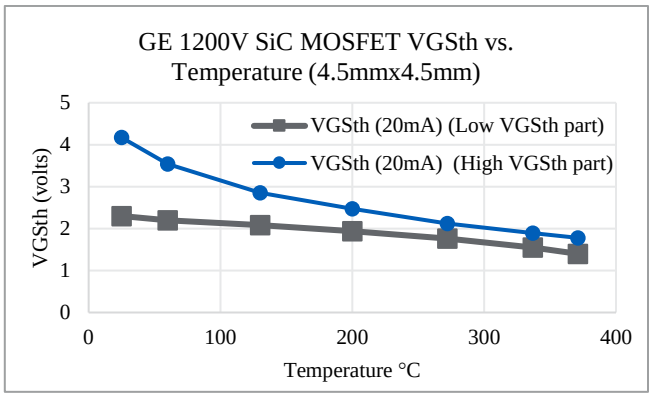

Figure 14. SiC MOSFET threshold voltage at up to 370ºc high versus low threshold voltage

GE Research further studied the IDSS performance of the high threshold voltage parts. Figure 15 shows that the first sweep yields approximately 40µA IDSS leakage at 340ºC. This value decreased to 30µA when -10V of gate bias was applied. When removing the gate bias, the leakage current increased to 80µA. Compared to the previous results shown in Figure 13, this device still was still functional when removing the gate bias. Finally, the device was tested with -10V of gate bias again with overlapping results compared to the first sweep. These sweeps are shown in Figure 15.

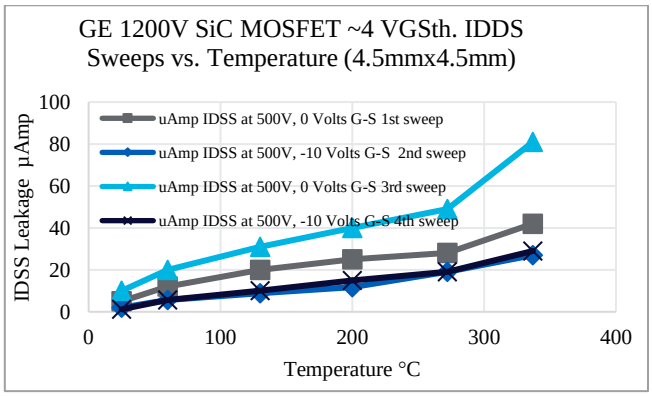

Figure 15. SiC MOSFET IDSS leakage at 500v high threshold voltage device

Estimates for current ratings versus device junction temperatures were conducted based on Equation 1 where T_{jmax} is the device junction temperature, T_c is the case temperature, R_{dson} is the on resistance, and $R_{thj\text{-}c}$ is the junction to case thermal resistance. A $R_{thj\text{-}c}$ of 0.3°C/W was assumed. Also, a junction temperature to case delta was assumed to be 100°C.

$$I_D = \sqrt{\frac{T_{jmax} - T_c}{R_{dson} \times R_{thj-c}}}$$

Equation 1. Current rating calculation

It is estimated that a 17-amp rating is achievable at 500°C as shown in the Figure 16.

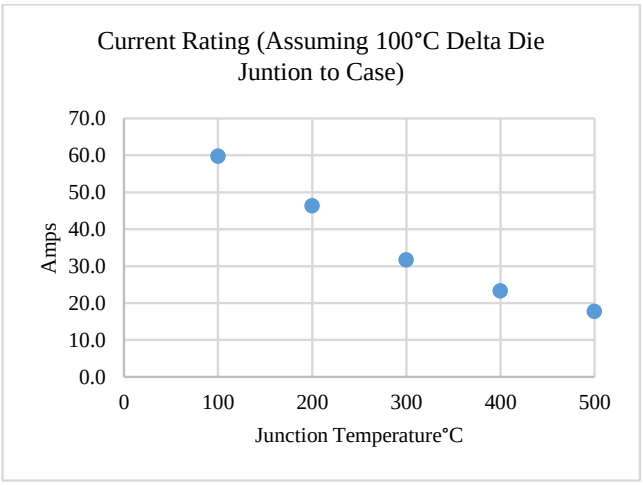

Figure 16. GE MOSFET current rating estimate at up to 500ºc

Conclusion

Testing performed to date has shown that GE's SiC power devices can operate at higher junction temperatures >200°C. A change in the dielectric blocking layer from an organic to an inorganic material is required to support the higher junction temperatures. Forward conduction performance was verified. Device stability and device selection for high temperature performance was analyzed. Long duration testing for tens or hundreds of hours was not possible due to the use of a top metal which limited the interconnect durability.

GE has extensive experience with Integrated Circuits high temperature device metallization and the next step to further this research is to extend that experience to power devices. With improvements in packaging and materials long term reliability tests such as thermal cycling, high temperature reveres bias, high temperature gate bias and negative bias instability tests can be conducted to further SiC device technology specifically for high temperature use. Based on the testing conducted, power conversion circuits utilizing SiC Diode and MOSFET power devices at extreme

temperatures are feasible. Future high temperature SiC device research will be focused on device parameters, stability, and reliability at high temperature.

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