



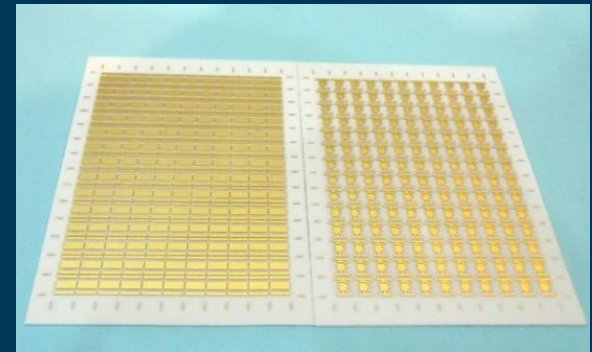
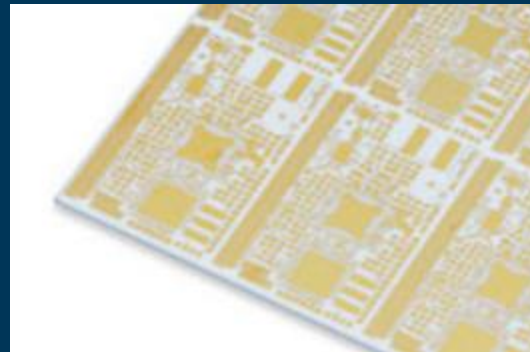
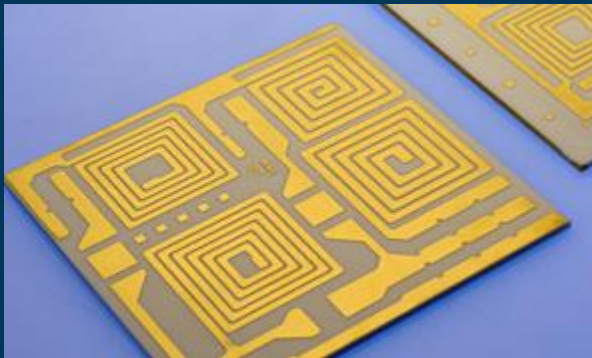
The Direct Plating Copper (DPC) Ceramic Material on Al₂O₃/AlN or LTCC Substrates

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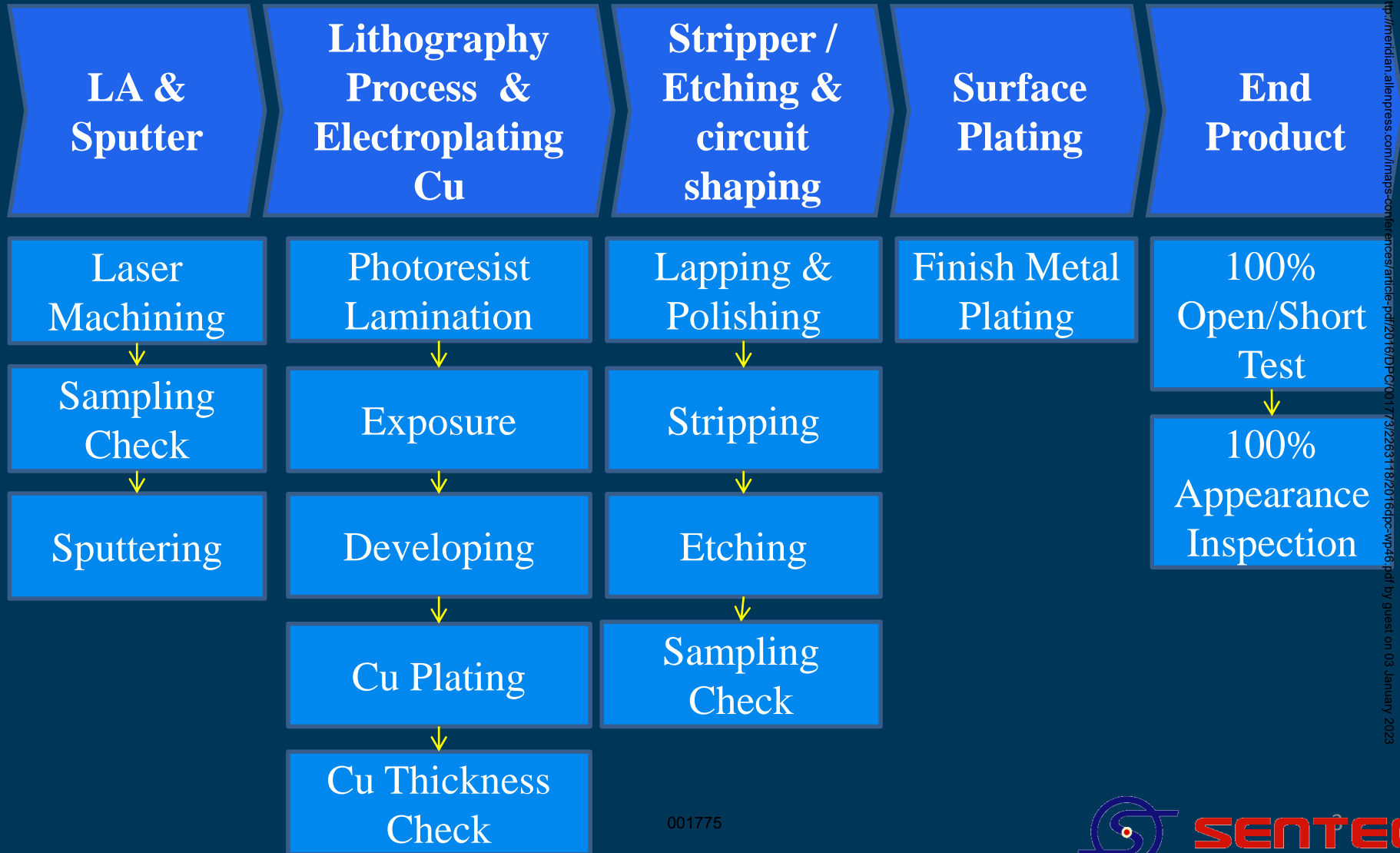


DPC on ceramic substrate

- DPC: Direct plating copper
- DPC ceramic substrate: Direct plating copper on the ceramic substrate
- DPC is widely using in high power density LED application with Alumina and AlN ceramic substrate.
- Also, we introduce DPC on LTCC or HTCC based ceramic substrates.



DPC Manufacture Process



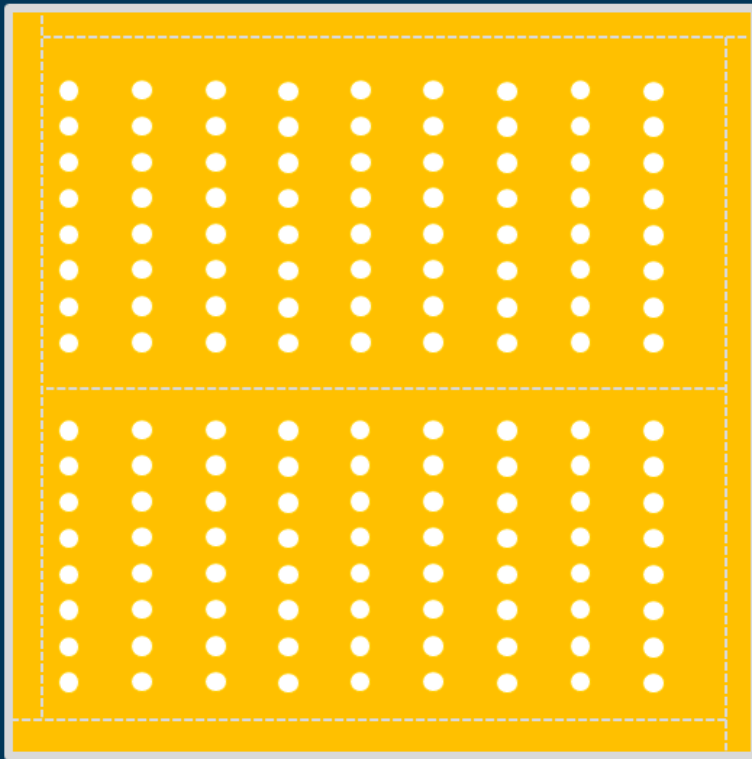
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1. Ceramic Substrate



1-1 Al₂O₃/AlN substrate

2. LA & Sputter

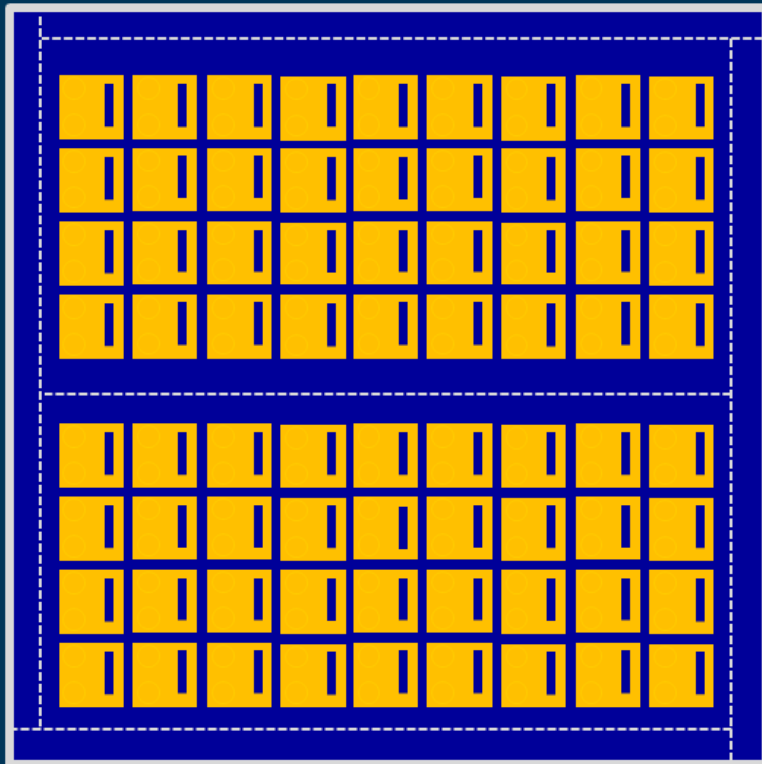


2-1 LA v-cut & via-hole



2-2 Sputter Cu

3. Lithography Process & Electroplating Cu



3-1 Exposure

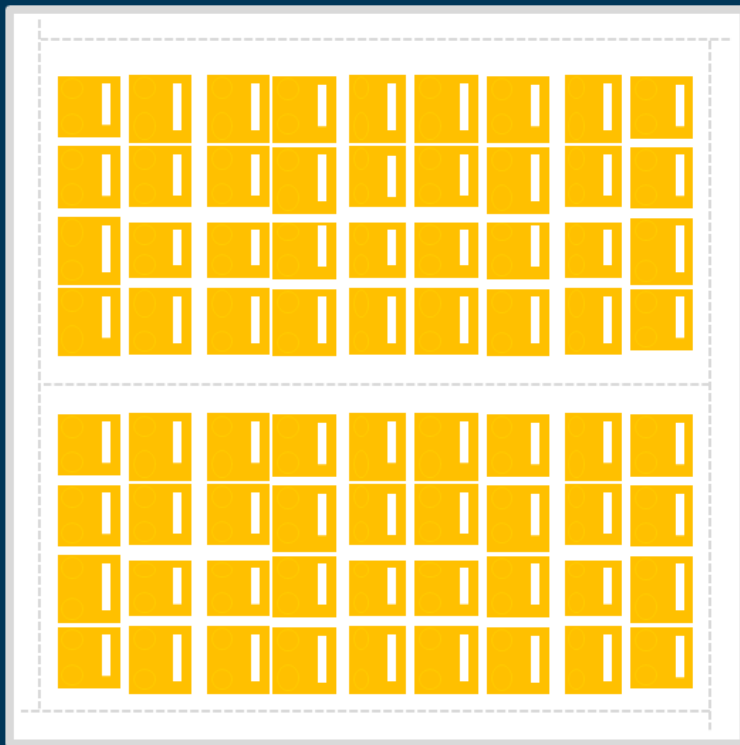


3-2 Developer



3-3 Electroplating Cu

4. Stripper / Etching & circuit shaping

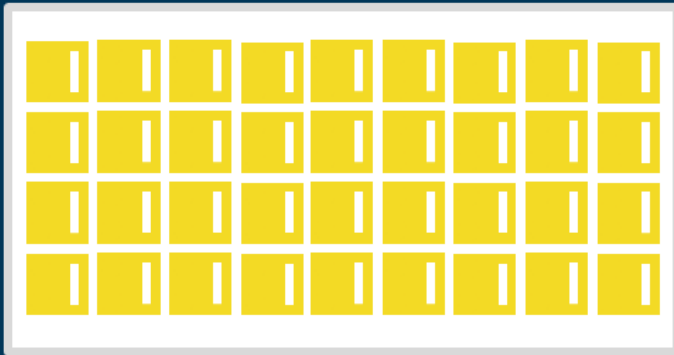


4-1 Stripping



4-2 Etching

5. Surface Plating



Plating:

- (1) Ni: 4.5um/Pd: 0.075um/Au: 0.1um
- (2) Ni: 4.5um/Au: 0.25um
- (3) Ag: 0.5um
- (4) Ni: 4.5um/Ag: 3um

Advantage of the DPC Ceramic Substrate

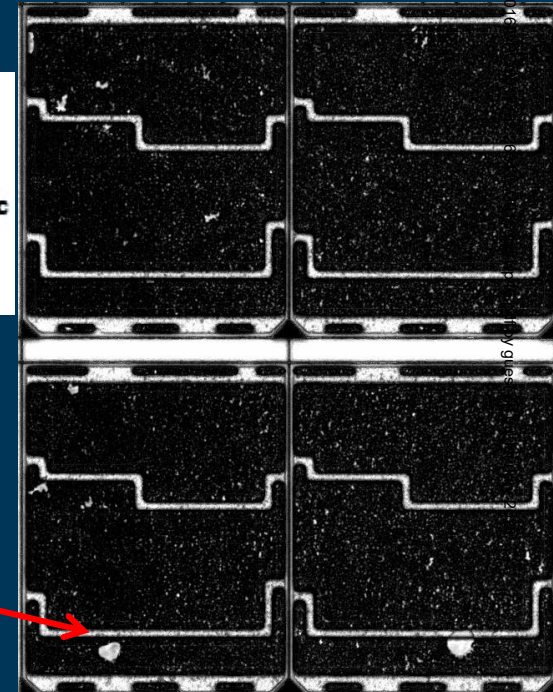
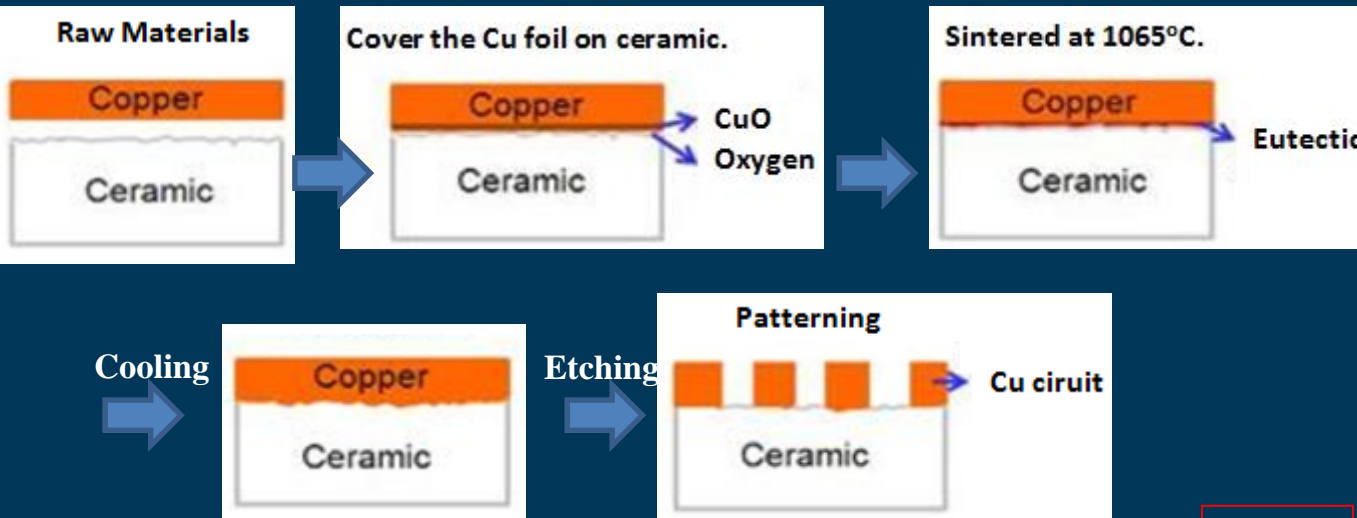
DPC ceramic substrate provide a better material stability and design flexibility comparing to the traditional DBC ceramic substrate:

- Excellent adhesion strength ($>0.5 \text{ kgf/mm}^2$ at $2 \times 2 \text{ mm}^2$ test pad) between metal and ceramic
 - The ceramic and plated Cu is integrated by sputtered Ti/Cu
- Excellent combination uniformity at metal and ceramic interface (Void rate at interface $< 1\%$)
- Low material electrical resistance of $2 \times 10^{-4} \Omega$ at $1 \text{ mm} \times 1 \text{ mm} \times 100 \mu\text{m}$ (Long/width/thickness) metal trace at 20°C .
- Two layer design available (electrical or thermal via holes between top and bottom pattern available).
- Excellent surface of the pattern surface of surface roughness, $R_a < 0.3 \mu\text{m}$.
 - To provide good solderability with lower void ratio between substrate and device
 - To provide good and high wire bondability and long term reliability.
- Excellent resolution of the pattern design
 - 100 μm line space available
 - Low dimension tolerance of 50 μm available

Benchmark between DPC & DBC

- DPC substrates exhibit advantage of low void, less than 1% (The manufacture process of the DPC ceramic is shown as page 8~13).
- DBC substrates are manufactured at 1065°C by the diffusion between ceramic and Cu /CuO layer.
 - The voids exist randomly between ceramic and Cu layer, and the high interface void ratio is about 10%.
 - Due to the heat dissipation and reliability concerns, the existence of voids in DBC is a disadvantage for high power applications.

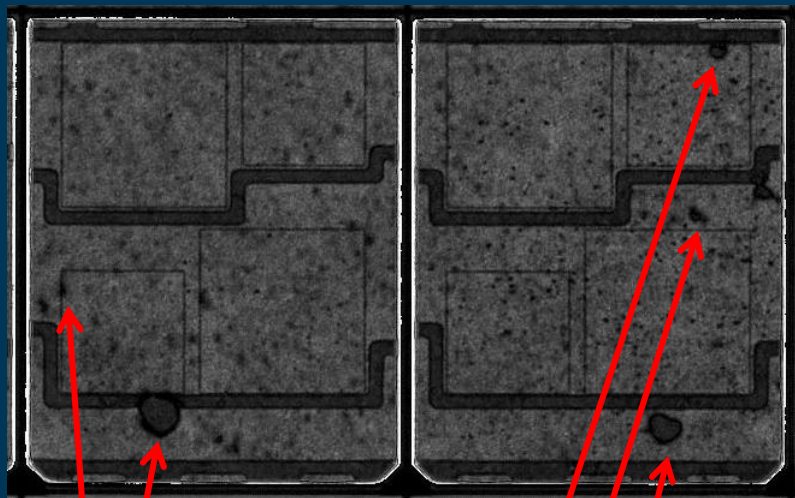
SAT analysis of DBC substrate



Void

	DBC Substrate	DPC Substrate
Max. Process Temp.	~850°C	< 200°C
Cu Thickness	≥ 200um	<10-150um
Void Rate of Interface	≈ 10%	< 1%
Typical Line Width	> 0.2mm	≈ 0.05mm
Typical Line Space	> 0.2mm	≈ 0.05mm
Dimension Tolerance	± 0.15mm	± 0.03mm
Camber	< 0.4%	< 0.25%

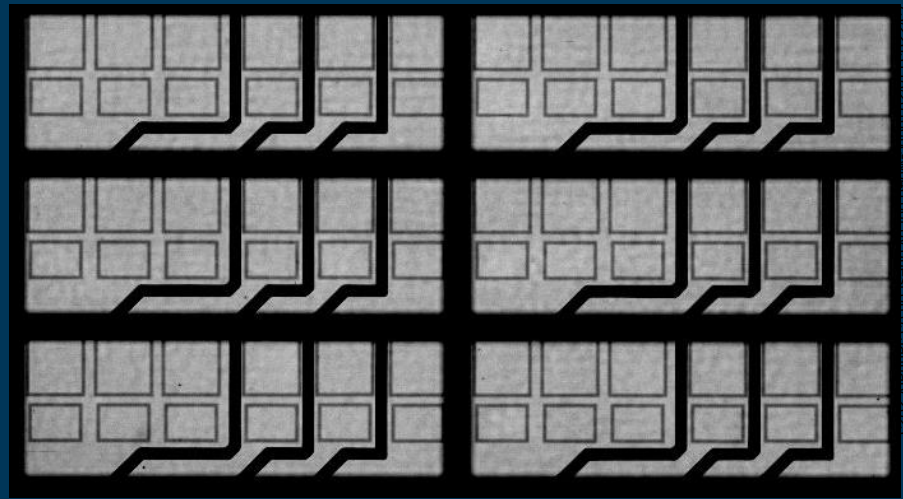
SAT analysis of DBC substrate



Void

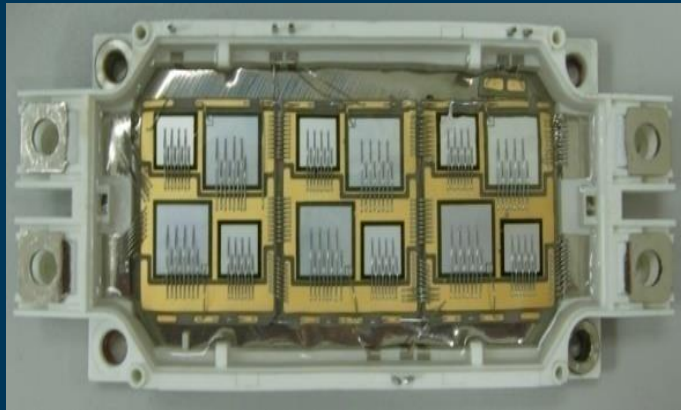
Void

SAT analysis of DPC substrate



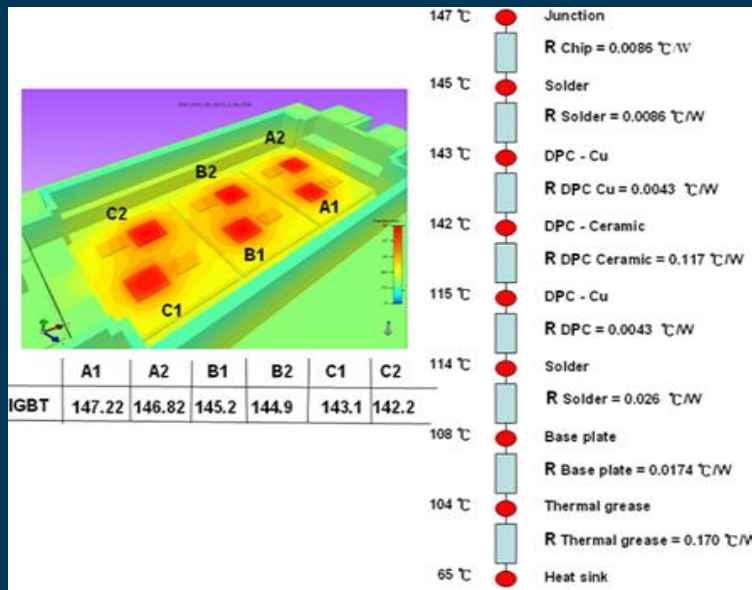
Excellent metal/ceramic interface

DPC substrate Application at the High Power module



600 V / 450 A IGBT module for EV driving

- Design of PIM, IPM and ISM
- 100 W – 50 kW products (600V/450A)
- Design for low thermal resistance and High reliability
- Manufacture using DPC substrate with high thermal conductivity
- Thermal resistance analyzation



Thermal Resistance Analyzation

- Both the DPC& DBC provide good thermal resistance behavior under driving 800 A current for 10sec and 480 A current for 150 sec.

	Test condition (Step 1)		Test condition (Step 2)	
	800 A / 10 sec		480 A / 150 sec	
	Connector	Chip	Connector	Chip
New structure 1 (DPC, Cu = 150 μm)	< 80 °C	< 50°C	< 130 °C	< 70°C
New structure 2 (DBC, Cu = 300 μm)	< 80 °C	< 50°C	< 130 °C	< 70°C

Special design v1

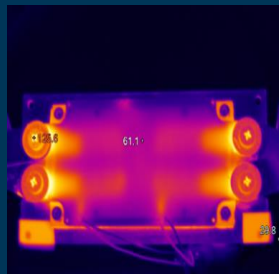
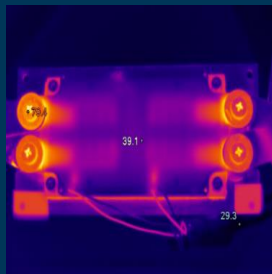
Special design v2

800 A / 10 sec

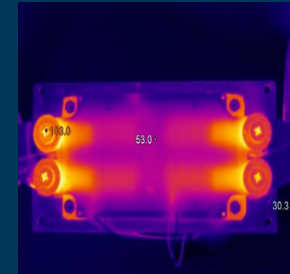
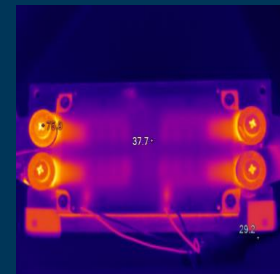
480 A / 150 sec

800 A / 10 sec

480 A / 150 sec



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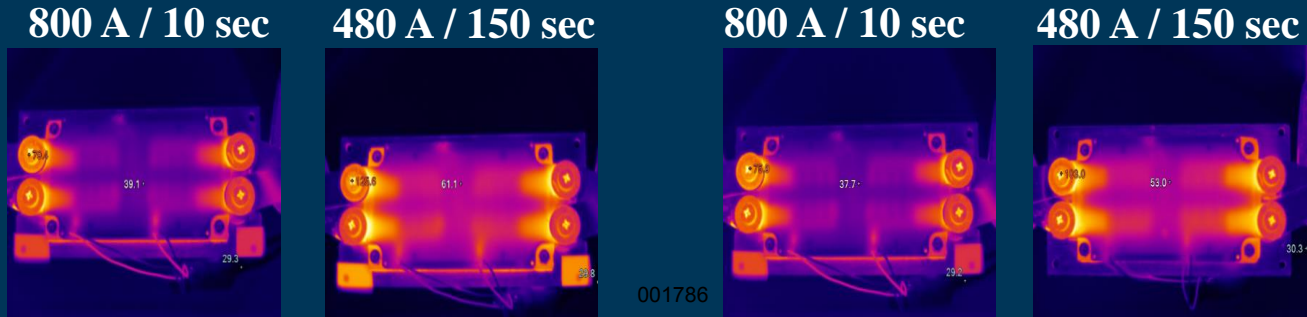
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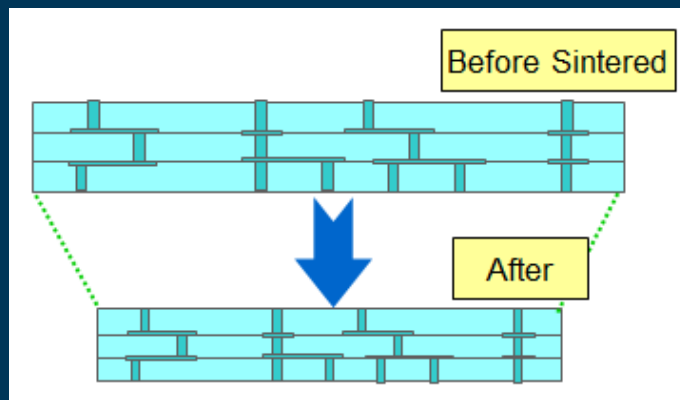
Special design v1

Special design v2

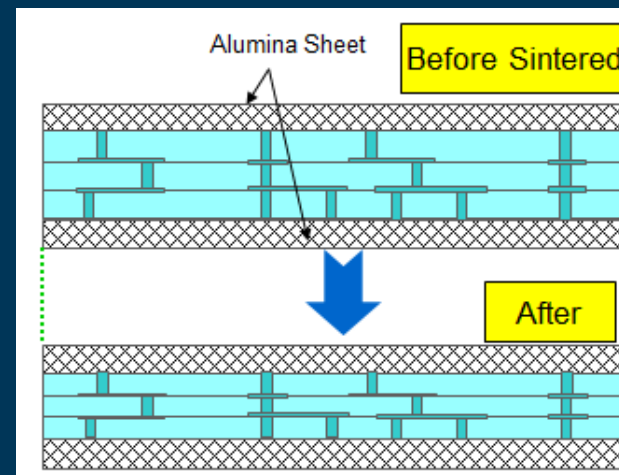


Non-Shrink LTCC ceramic substrate

- LTCC offer a wide range of possibilities to realize multilayer circuits with an almost unlimited number of layers. Together with the low dielectric losses, the LTCC technology is eminently qualified for many applications.
- To realize the DPC plating on the LTCC substrate, the non-shrink LTCC technique is introduced.



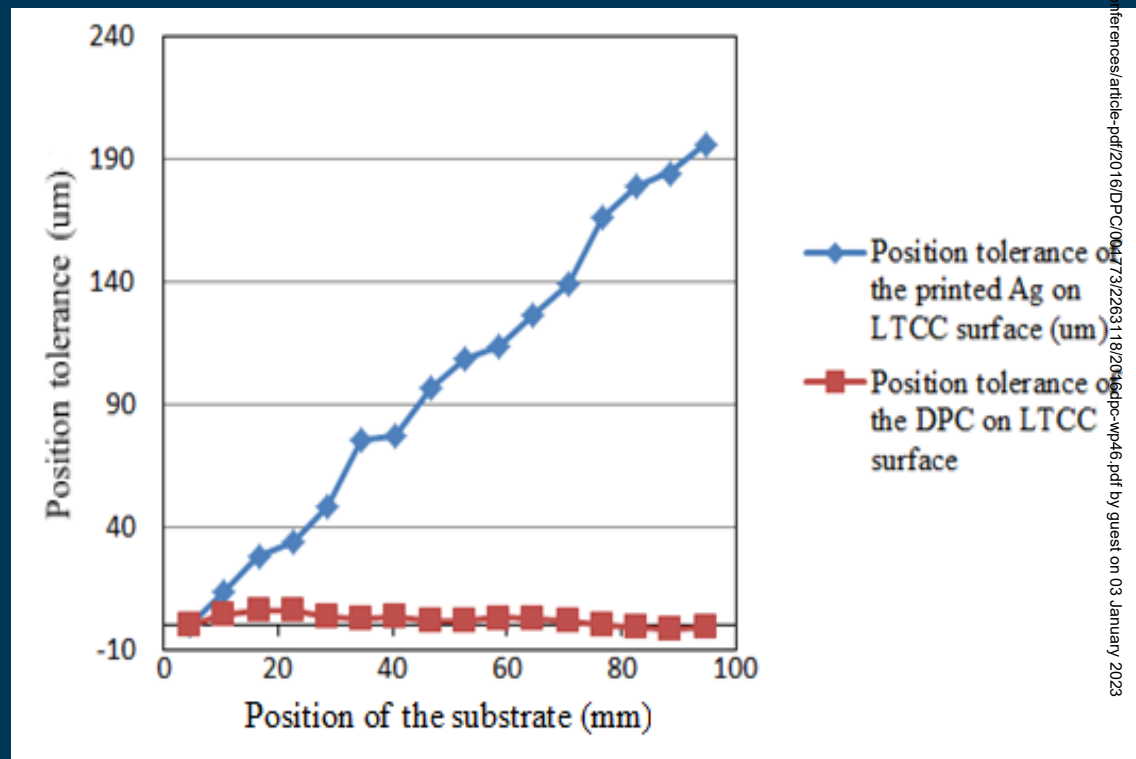
Normal LTCC



001787 Non-Shrinkage LTCC

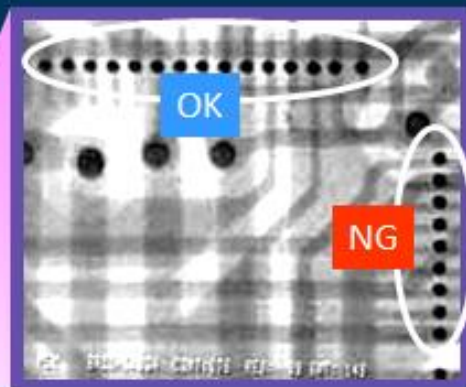
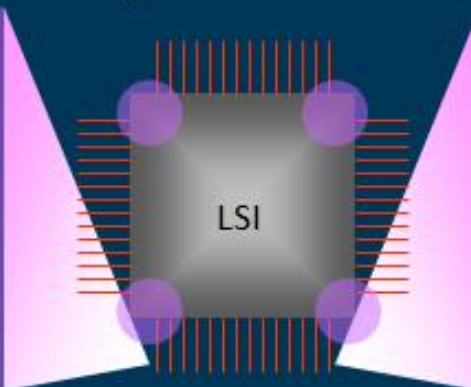
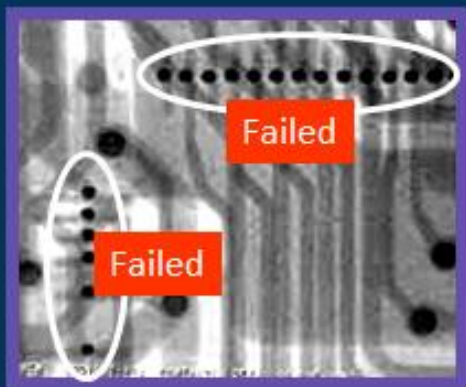
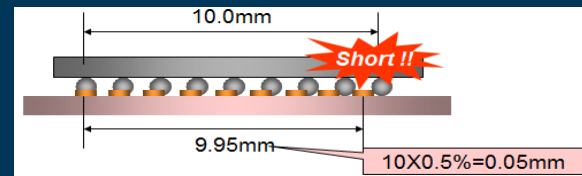
DPC on the LTCC ceramic substrate

- In the non-shrink LTCC technique, by the strong control of the process parameters, the tolerances of freely sintered LTCC substrate can be reduced to around 0.2%.
- In the case, the total size tolerance can be controlled under 200 μm at 100 by 100 mm^2 . This dimension tolerance can be further improved by the following DPC metalized layer.

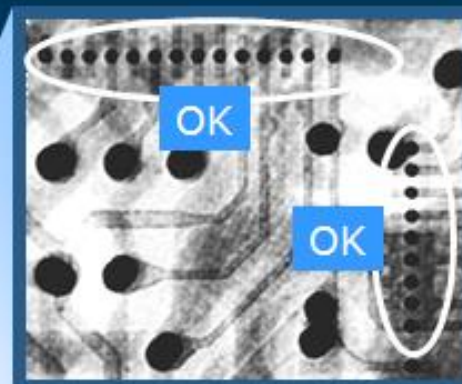
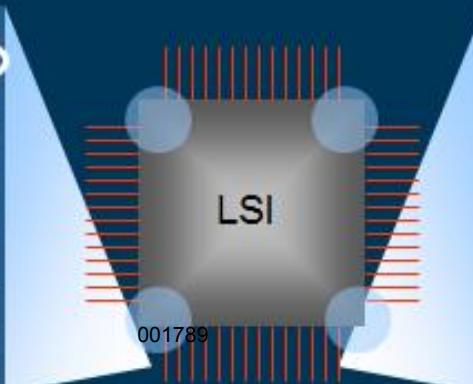
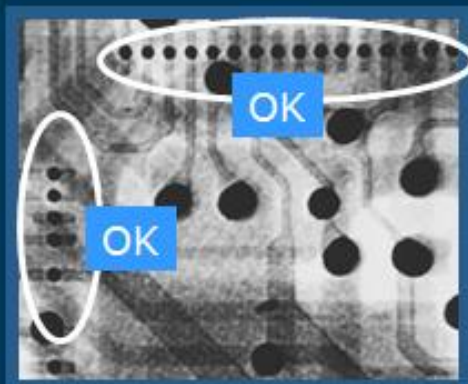
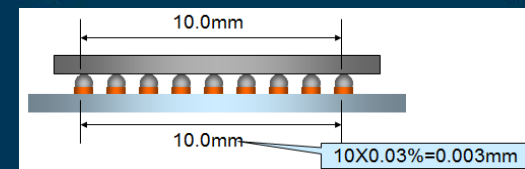


X-ray Photograph of DPC on LTCC

Standard LTCC in flip chip interconnection



DPC on non-shrink LTCC in flip chip interconnection



Conclusions

- DPC ceramic substrate provide a better metal/ceramic interface uniformity and material reliability due to much less voids in the metal/ceramic interface.
- According to the 600 V / 450 A IGBT module for EV driving test, the DPC substrate is stable with well thermal dispassion at the high power module.
- The DPC substrate provide gold pattern resolution of 100 um line space with tight tolerance of 20 um min. available
- With a suitable design DPC is an ideal ceramic substrate material for high power module.
- By the non-shrink LTCC technique introduced, a high accuracy surface metallization multi-layer ceramic substrates design can be realized.