

A 200 °C Motor Control ASIC

Steve J. A. Majerus^{1,2}, Daniel T. Goff^{1,2}, and Walter Merrill¹

1. BluBerry, LLC, Columbia Station, Ohio

2. Case Western Reserve University, Cleveland, OH

Abstract

A custom application-specific integrated circuit (ASIC) has been designed for positional control of brushless DC or servo motors in high-temperature (>200 °C) environments. Applications would include valve and position control for aerospace and industrial systems. Patented high-temperature circuit design techniques facilitate high-temperature operation from a conventional, low-cost, 0.5-micron bulk CMOS foundry process. The ASIC is highly integrated to enable software- and processor-free local control of motor position, and uses external power MOSFETs for motor commutation. Motor position can be controlled in open- or closed-loop modes with an integrated rotational variable displacement transformer (RVDT) direct digital synthesis (DDS) waveform generator, rail-to-rail op-amp driver and demodulation circuit. The ASIC can accept both analog (0–10 V) or digital (SPI bus) position setpoint commands from an external controller. Motor position is indicated by both analog and digital output signals. The full-scale displacement of the controlled motor is programmable from 5 to 8 bits of resolution, permitting 32–256 positions of control. Safety features such as a 500-ms power-on delay, overtemperature and motor overcurrent detection, and control signal undervoltage lockout were included to minimize the need for external control.

ASIC bench-test results confirmed circuit functionality at ambient temperatures up to 225 °C using room-temperature power MOSFETs and motor load. ASIC performance at the 8-bit level was demonstrated, although the clock oscillator frequency shifted by about 15% over the full temperature range. Control of the motor at 200 °C was also demonstrated, although moderate loss of motor holding torque was observed due to internal heat generation in the motor. The ASIC was combined with commercially-available off-the-shelf high-temperature components on a printed wiring board (PWB) to form a compact (4 x 3.5 inch) motor control demonstration system capable of prolonged operation at temperatures beyond 200 °C. Environmental and long-term testing of the PWB is planned to demonstrate system reliability.

Key words: instrumentation amplifier, sigma-delta converter, motor driver, buck converter, PWM controller

I. INTRODUCTION

Several industries—automotive, aerospace, and downhole drilling—have historically relied on high-temperature electronics, but the application of the electronics was usually limited by the maximum operating temperature or reliability needs. Continued efforts to push the performance envelope while reducing overall system size, weight, and cost have demonstrated the need for complex integrated circuits capable of operating at elevated temperatures of 200 °C and beyond. Increasingly reliable operation of semiconductors at these temperatures has been demonstrated, and it is now feasible to construct more complex systems with high-temperature semiconductors.

New applications such as all-electric aircraft, distributed engine controls, and instrumented downhole equipment often seek to reduce wiring requirements,

increase redundancy and overall system robustness by placing sensing and actuation electronics as close to the mechanical “hot zones” as possible. Bridging the electrical/mechanical gap is not trivial however, as high-temperature motors and actuators are frequently weaker than their industrial-temperature equivalents, and might require special feedback and control laws to provide accurate control.

Brushless DC (BLDC) and servo motors, for example, can operate at high temperatures, but use lower permeability core materials. The resulting motors are more stable over temperature but have reduced motor torque. Furthermore, commonly-used feedback elements such as Hall-effect sensors, cannot be used at high temperatures, limiting commutation accuracy. Finally, while motor control is typically implemented in software, the lack of long-life, high-temperature microcontrollers as well as the regulatory issues surrounding software in certain applications limit the

motor control implementation options.

We have designed an application-specific integrated circuit (ASIC) to permit local, closed-loop control of a BLDC or servo motor in a high-temperature ($>200\text{ }^{\circ}\text{C}$) environment. Continuous commutation of a high-temperature motor can lead to a large level of self-heating, so the ASIC was designed for positional control of motors which typically have 30 – 250 turns over their full range. A high level of integration reduces the overall system component count and allows for direct interfacing to motor feedback elements and drive circuitry.

II. HIGH-TEMPERATURE INTEGRATED CIRCUIT DESIGN

Researchers at CWRU and BluBerry, LLC have worked with NASA and AFRL to extend the useful operating temperatures of bulk CMOS circuits to beyond 200°C . By using circuit techniques to address physical shortcomings, monolithic circuits comprising oscillators, amplifiers, and sigma-delta ADCs were fabricated in a $1.5\text{-}\mu\text{m}$ process and demonstrated to function beyond $275\text{ }^{\circ}\text{C}$ [1], [2]. The same principles were applied to a $0.5\text{-}\mu\text{m}$ process to create a set of application-specific integrated circuits (ASICs) for sensing and actuation. The ASICs were combined with other components to form a “smart node” for distributed engine control, and operation of the hardware from -55 to $200\text{ }^{\circ}\text{C}$ was demonstrated. Further test results at $200\text{ }^{\circ}\text{C}$ were reported in [3]. Continuous operation of the circuits at $200\text{ }^{\circ}\text{C}$ was demonstrated for 4700 hours; a

commercial part failure halted testing but no loss of performance in the custom ICs was observed [4].

The technical challenges involved in developing high-temperature, bulk CMOS circuits include:

- Degradations in electron/hole mobility
- Decrease in MOSFET voltage threshold
- Increase of bulk junction leakage current
- Greater vulnerability to latch-up
- Increase in silicon intrinsic carrier density

High-reliability IC layout techniques were used to improve device reliability at elevated temperatures. Conservative design rules which emphasize redundant vias and short, wide traces were used to reduce the rate of failure due to electromigration [5]. Depletion guard structures, plentiful substrate contacts, and integrated catch diodes helped to prevent latch-up conditions at elevated temperatures [6]. Finally, proprietary biasing schemes and drift-tolerant circuit architectures were adopted to provide robust high-temperature performance.

III. MOTOR CONTROL ASIC OVERVIEW

The motor control ASIC described in this paper was designed for fabrication in a conventional, low-cost $0.5\text{-}\mu\text{m}$ bulk CMOS process. The system specifications were selected to be flexible to a number of configurations typically used for positional motor control. Because the selected process is designed for low-power 5-V use, motor driving MOSFETs and gate drive/level shift circuits were not included on-chip as

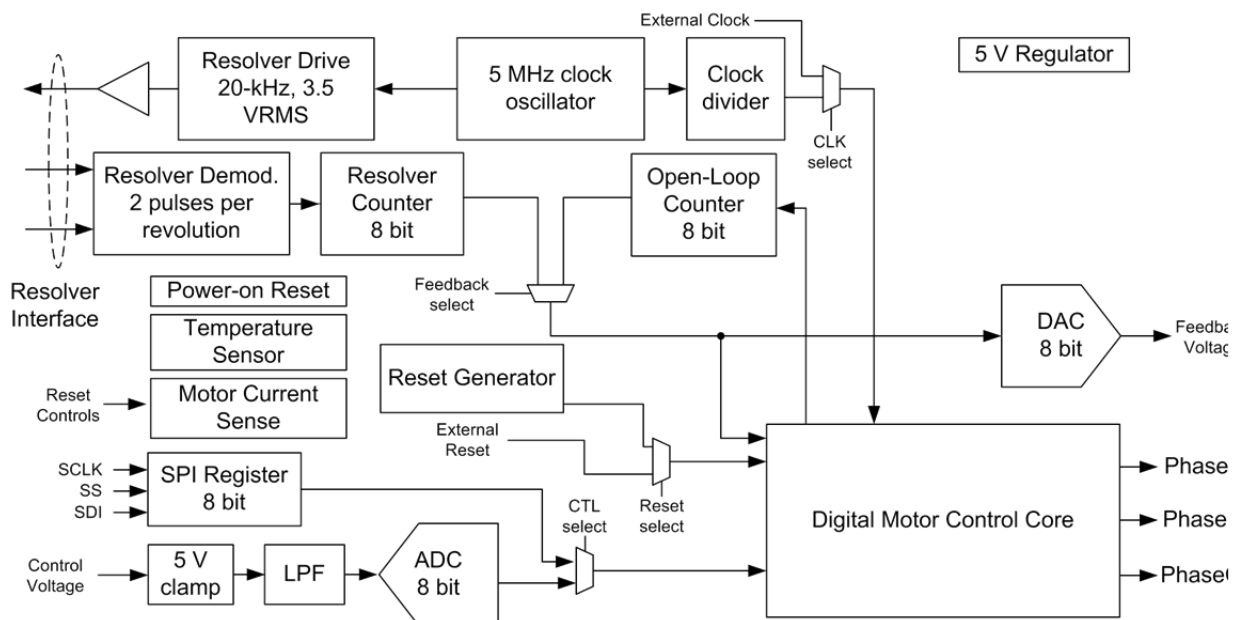


Figure 1: BMC1 ASIC simplified block diagram.

they are available commercially [7]. Drain-extended MOS structures were used to create a power regulator capable of producing a fixed 5-V supply rail from a 6 – 15 V input signal. A block diagram of the BluBerry Motor Control (BMC1) ASIC is shown in Figure 1.

The ASIC was designed to work with both traditional hierarchical controllers or with a high-temperature microcontroller if such a part is acceptable in a given application. The full-scale motor position can be programmed from 32 – 256 positions. For traditional control modes, the ASIC accepts a 0-5 V control signal which is digitized by an 8-bit analog-to-digital converter (ADC) to program the motor position setpoint. As the motor commutates, a digital-to-analog converter (DAC) reports each motor position as a voltage step, such that a feedback voltage signal can be sent to the controller to form an all-analog control loop.

In the digital control mode, an integrated serial-peripheral interface (SPI) bus is included for bidirectional serial communication to a nearby host controller. Position setpoints are sent to the ASIC over SPI, and the current motor position is reported back over the same bus. The feedback DAC continues to report the analog motor position in both control modes.

While the ASIC can control motor position in an open-loop fashion, this mode is only intended when a servo motor is used. Due to varying torque ripple and potentially varying load characteristics, BLDC motors are best controlled in a closed-loop fashion when positional accuracy or rotational speed is important. Currently, the most stable high-temperature motor position feedback mechanism is the rotational variable displacement transformer, or RVDT. An RVDT functions similarly to its linear counterpart the LVDT, except that the coupling between primary and secondary coils varies cyclically rather than linearly. For closed-loop positional control using an RVDT, the ASIC includes a dedicated 20-kHz sinusoidal driver circuit for the RVDT primary winding, plus circuitry to demodulate the secondary signals. The demodulated secondary signals are processed into binary waveforms and counted so that motor position can be tracked.

The general motor position control law is illustrated by the state diagram shown in Figure 2.

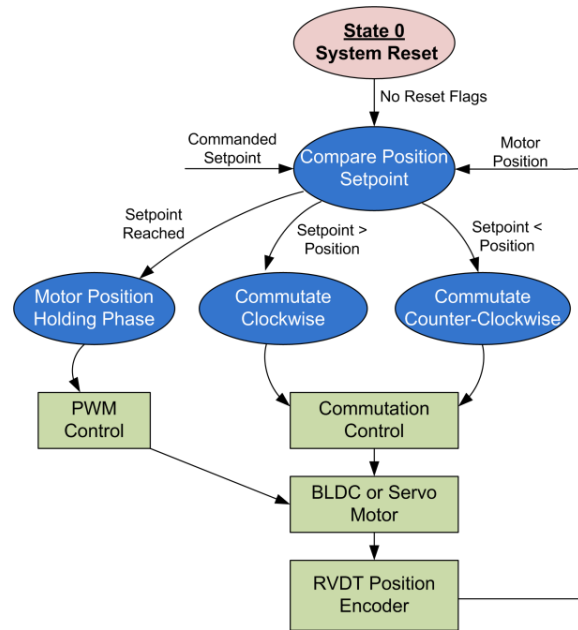


Figure 2: BMC1 motor position control loop.

To simplify commutation requirements, the motor always proceeds at a fixed rotational rate regardless of the distance between the current position and the commanded setpoint. This is acceptable in positional control applications, where motor position is usually changed in small increments such that motor acceleration effects can be neglected. Once the commanded setpoint is reached, the motor switches into to a holding mode, in which the commutation pattern changes to a PWM-controlled drive signal to reduce the average motor current and to prevent self-heating.

IV. MOTOR CONTROL ASIC DESIGN

The control law for the BMC1 is implemented with static digital logic, but several critical functions of the IC required custom analog and mixed-signal circuitry. Many of the circuit building blocks have been previously reported in [2], [8], and [9], but new designs for the 8-bit ADC, DAC, and RVDT driver/demodulator were created for the BMC1. The ADC and DAC used fairly conventional successive-approximation and current-steering topologies with R-2R DAC elements used to provide tight temperature coefficient matching.

One unique circuit on the BMC1 is the RVDT driver, depicted in Figure 3. The RVDT primary winding must be driven by a large-scale (5 V_{pp}), low-distortion sinusoid to provide good signal-to-noise ratio at the secondary windings. The sinusoid signal is created by a direct-digital-synthesis (DDS) circuit which stores pre-computed coefficients of a sine wave and is

clocked by a fast on-chip oscillator. The DDS produces a 20-kHz delta-modulated sine wave which must be filtered to remove high-frequency distortion.

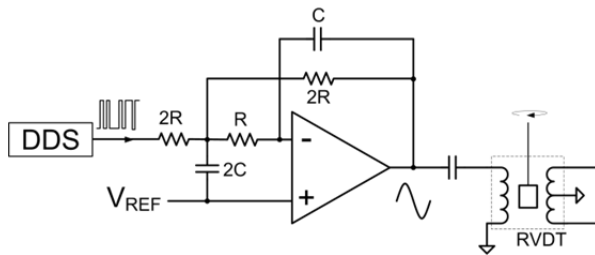


Figure 3: 20-kHz RVDT primary driver schematic.

The DDS output is filtered by a 3-stage op-amp, arranged as a multiple-feedback lowpass filter. This configuration is useful as it provides constant bandwidth due to matched resistor temperature coefficients, and the feedback maintains a constant common-mode input voltage. The opamp is compensated to drive large inductive loads, and has a rail-to-rail output such that it can be directly connected to the RVDT primary through a DC-blocking capacitor.

As the motor rotates, the RVDT coupling to its secondary windings varies, such that each secondary can be treated as the AM-modulated waveform,

$$y(t) = [1 + \cos(2\pi f_m t)] \cdot A \sin(\pi f_c t),$$

where f_c is the 20-kHz primary winding signal of amplitude A and f_m is the rotational frequency of the motor. The AM-modulated signal can be de-modulated in a variety of ways, but the BMC1 uses non-synchronous envelope demodulation so that it is not sensitive to carrier frequency phase shifts between the RVDT secondary windings.

During motor commutation, the differential RVDT

output signal envelopes are described by

$$A(t) = \cos(2\pi f_m t), B(t) = \cos(2\pi f_m t \pm \pi/2),$$

such that the A and B signal envelopes are always $\pm 90^\circ$ apart depending on the direction of motor rotation. In precision RVDT applications, the A/B relative amplitudes can be computed to obtain an accurate representation of the motor shaft position from 0 to 360° .

For motor positional control, however, the motor shaft can only be rotated to align with the fixed stator poles, so R must only be resolved to an integer multiple of 360 . A 4-pole motor with six stator windings, for example, can only hold at discrete multiples of 30° where the rotor poles align with the stators. Therefore, to simplify the RVDT demodulation, and to permit a digital solution, the circuit depicted in Figure 4 was created. The circuit first uses switched-capacitor peak detector (SCPD) circuits to recover the coarse envelope of the motor rotational signal. Mixed-signal techniques were used to set the time constant of the peak detectors so that the time constant was frequency-locked to the DDS clock oscillator to enhance temperature stability and chip-to-chip matching.

The output of the SCPDs is essentially the envelope of the RVDT secondary signals, with a small amount of f_c ripple as determined by the detector time constant τ_s . The comparators which convert the envelope to binary waveforms include hysteresis equal to twice the f_c ripple to limit glitches in the binary converted RVDT secondary signals. The comparators share a reference signal which is self-generated by replica SCPD circuits.

Because the signal levels at the RVDT primaries can be affected by changing primary winding drive amplitude or drift in the SCPD V_D , the comparator

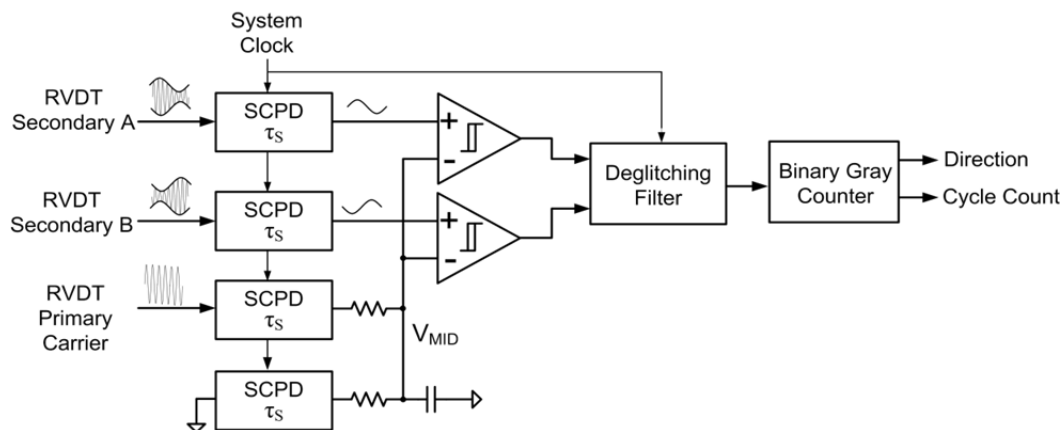


Figure 4: The RVDT signal analog-to-binary demodulator.

reference V_{MID} is automatically generated to track any drift over temperature or time. The V_{MID} level is generated by a replica circuit consisting of two additional SCPDs. One SCPD produces the peak envelope of the RVDT primary carrier, while the other produces a DC level V_{MID} representing the voltage drop V_D of each SCPD. The two levels are summed to produce a voltage which tracks the mean voltage at the output of both secondary SCPDs.

The RVDT secondary binary signals are further processed by a digital deglitching filter. Motor direction and rotational count is determined by a Gray counter, which increments a position counter within the control law state machine.

V. MOTOR CONTROL ASIC TEST RESULTS AND PERFORMANCE SUMMARY

The BMC1 was fabricated in a low-cost, 0.5- μm bulk CMOS technology, and a die photo is shown in Figure 5.

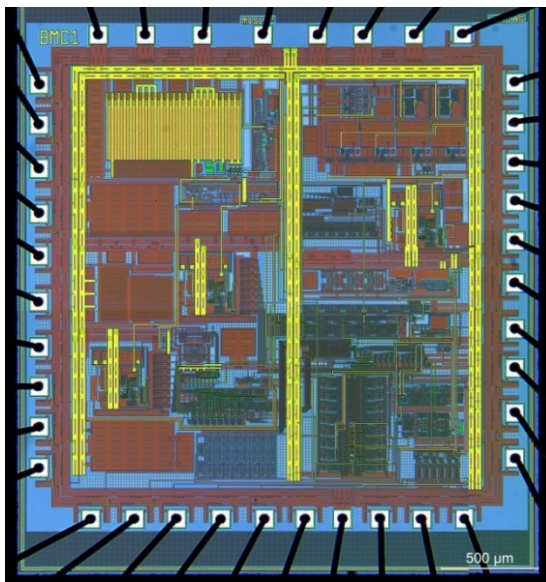


Figure 5: BMC1 die photo. Die size is 2.5 x 2.6 mm.

The die was packaged in a 40-pin ceramic DIP for ease of testing; later versions of the die were packaged in a 22-pin narrow DIP to save area. Testing of the ASIC over temperature was performed with a clamp heater, as shown in Figure 6. The heater maintained temperature control of the ASIC, while other PWB components operated at room temperature.

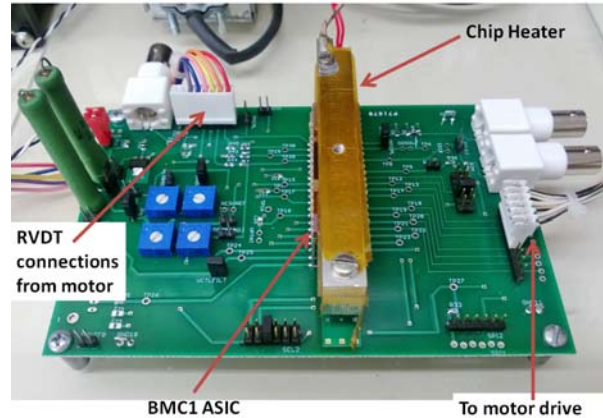


Figure 6: BMC1 high-temperature test setup.

An off-board motor driver constructed of commercially-available power MOSFETs was used to drive a high-temperature-capable BLDC motor. The motor drew on average 1 A while commutating and included a 2-cycle per revolution RVDT.

Generally, the ASIC performed as expected, although minor digital race hazards were discovered in the 8-bit control mode when operating above 170° C. Because the rail-to-rail low-pass filter opamp was used extensively within the ASIC, its temperature stability was confirmed with a network analyzer, as shown in Figure 7. The average filter bandwidth was 37 kHz with about $\pm 2\%$ variation over temperature. The filter gain of 3 dB was incredibly stable and remained within $\pm 0.1\%$ across the temperature range.

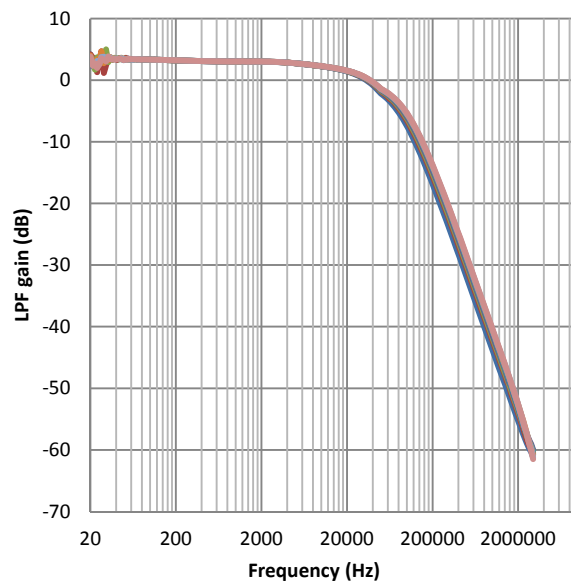


Figure 7: Measured BMC1 lowpass filter opamp frequency response from 25 – 210° C.

The DDS output was connected to the lowpass opamp, which drove the RVDT primary with a 5-V_{PP} signal. The opamp filtered the binary DDS output to produce a low-distortion, 20-kHz sinusoidal current of 3 mA_{RMS} in the RVDT primary, as shown in Figure 7.

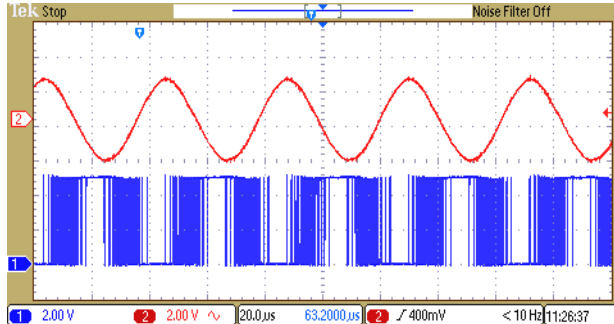


Figure 8: The DDS binary output (bottom trace) is filtered to produce a low-distortion sine wave (top trace).

The closed-loop operation of the ASIC at 200 °C is shown in Figure 9. An analog control square wave was used to command motor position (blue bottom trace). The top trace shows one of three motor commutation signals; the motor enters a PWM holding when the commanded position is reached and commutates at a fixed rate otherwise. The lower red trace shows the feedback voltage from the ASIC, representing motor position. The motor commutates until the commanded position is reached, and the system enters the PWM holding phase, as expected.

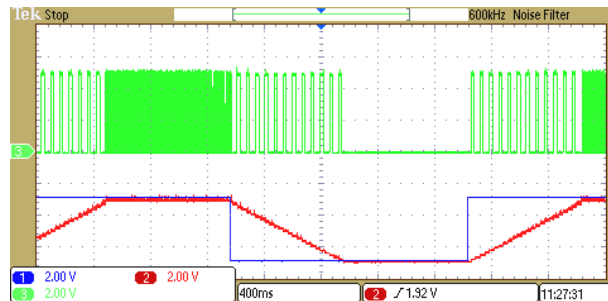


Figure 9: Closed-loop motor control step response demonstrating fixed-speed commutation and PWM motor holding phases.

VI. CONCLUSION

A motor-control ASIC capable of closed-loop control of BLDC and servo motors at temperatures beyond 200 °C has been developed. The ASIC architecture was chosen to be flexible to multiple motor control modes and range, while still integrating as many circuits as possible to increase reliability while limiting overall system size. Stable operation of key circuit

blocks was confirmed, and 200 °C closed-loop operation of a high-temperature motor was demonstrated.

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