Parametric study of electronics components joining using reactive films for high temperature applications

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Abstract

In this paper, in order to assemble electronic components onto substrates, a local rapid soldering process using an exothermic reactive foil sandwiched between solder preforms was evaluated. Among others, the main interest of this technique is that it can allow the use of high temperature melting solders, without the need to heat the whole assembly above this melting temperature. The reactive foil is commercially available and is formed from alternatively stacked nanolayers of Ni and Al until it reaches the total film thickness. Once the film is activated by using an external power source, a reaction takes place and releases such an amount of energy that is transferred to the solder preforms. If this amount of energy is high enough, solder preforms melt and insure the adhesion between the materials of the assembly. The process was evaluated using a standard SAC305 and a high temperature $Au_{80}Sn_{20}$ preforms. The influences of the applied pressure, the reactive film thickness as well as the solder and the attached materials nature and thicknesses were investigated. The initial joint quality was evaluated using scanning acoustic microscopy, scanning electron microscopy, and shear strength measurements. It was shown that the applied pressure during the process has a strong effect on the joint initial quality. The voids ratio between metallized diode dice and an Active Metal Braze (AMB) substrate decreases from 64% to 26% for pressure values between 0.5kPa and 100kPa respectively. Otherwise, under a constant low pressure of 13kPa, reducing the substrate metal thickness on a low thermal conductivity insulator allows the improvement of the initial joint quality and a voids ratio of about 15% was reached when using 35µm of copper on FR4 substrate. The use of aluminum instead of copper as a metal for the ceramic metallized substrate (with the same gold finishing layer) led to a reduction in the void ratio in the joint. The microstructure of the AuSn joint achieved using the reactive films shows very fine phase distribution compared to the one obtained using conventional solder reflow process in the oven. The mechanical properties of the joint were evaluated using shear tests performed on 350µm thick silicon diodes assembled on AMB substrates under a pressure of 100kPa. The reactive films were 60µm thick and were sandwiched between two 25µm thick SAC preforms. The void ratio was about 37% for the tested samples and shear strength values above 9.5MPa were achieved which remains largely higher than MIL-STD-883H requirements. Finally, the process impact on the electrical properties of the assembled diodes was compared with a commonly used solder reflow assembly and results show a negligible variation.

Key words

Reactive film, nanolayers, soldering, void ratio, shear strength, high temperature electronics

I. Introduction

The market introduction of high temperature wide band-gap Silicon Carbide (SiC) or Gallium Nitride (GaN) power semiconductor devices with junction temperature exceeding 200°C significantly accelerates the trend towards high power density and severe ambient temperature electronics applications [1],[2]. Such evolution allows to reduce the mass and volume of the power electronics systems that may have a great impact in aeronautics applications, especially with the development of More Electric Aircraft (MEA) as well as hybrid and full electric aircraft. As a consequence, the aircraft operating cost could decrease [3].

New packaging materials suited to more severe thermal constraints is mandatory to achieve high performance and augmented reliability of systems employing such new high operating temperatures power semiconductor devices. Among others, die attaching materials and processes must be developed to meet these requirements.

Conventionally, the electronic components (power semiconductor devices, capacitors, inductors…) of the power module are attached to the substrate by the use of solder paste or solder preform combined in a reflow process in an oven. Reliable joint can be achieved by using the solders below 80% (temperature in Kelvin units) of their melting temperature (Tm) while the reflow temperature should be about 30K higher than Tm [4],[5],[6]. During the soldering process, the temperature variation and the high reflow temperature can induce the degradation of sensitive materials as well as the substrates bowing [7]. Those issues are commonly encountered in high temperature electronics packaging and can be bypassed by developing processes with rapid and local heating techniques. The aim of this paper is to evaluate a technique based on the use of reactive film sandwiched between two solder preforms to attach electronic devices on their substrates. Once the reactive film is activated, the energy of the reaction taking place at atomic level of the nanolayers forming the film can lead to the increase of the solder temperature above its fusion temperature. Hence, the melted solder will allow to attach the elements that are in contact with it. A parametric study enabled us to evaluate and understand the impact of various parameters (pressure, element thicknesses and nature) on the voids ratio in the joint. In addition, the microstructure of the joint and its mechanical shear strength were evaluated. Finally, since the process induces a high increase of the temperature during very short time (several milliseconds (ms)), the impact of the latter on the electrical characteristics of the diode was tested.

II. Experiments

Infineon IDC51D120T6M (7.00mm×7.30mm×110µm) and ABB 5SLY12E1200 (6.3mm×6.3mm×350µm) both silicon (Si) diodes both with silver (Ag) finish back metallization were attached to three types of substrates. In most cases, Active Metal Brazed (AMB) Cu/Si$_3$N$_4$/Cu (300µm/300µm/300µm) substrates were used. The joint on Direct Bonded Aluminum (DBA) Al/AlN/Al (300µm/635µm/300µm) substrates was also tested in order to evaluate the effect of the substrate metallization material (copper (Cu) and aluminum (Al)) on the joint quality. The last substrate type (printed circuit board PCB) was involved in this study to evaluate the impact of metal thicknesses on the final joint. The process was performed on FR4 material with copper metallization of 35µm and 70µm. All the substrates have a Ni/Au finish layer which allows to neglect the effects of the latter on solder wettability. Reactive Films (RF) composed of alternatively stacked nanolayers of Ni and Al are commercialized under the trademark *NanoFoil®* by Indium Corporation. Two foils thicknesses of 40 and 60µm were used in this study. The RF was sandwiched between two solder preforms that are in contact with the components to assemble. SAC305 (25µm and 50µm thick) and Au$_{80}$Sn$_{20}$ (50µm thick) solder preforms were evaluated. Once the assembly was stacked, a small pressure was applied on the top of the dice by using stainless steel weights. Stainless steel weights were thermally decoupled from the die by using a 250µm porous Teflon film on the top of the die (Fig. 1a). The reactive film was activated using an electrical power source (applied power of 6W). After activation, the film initially composed from consecutive nanolayers on Ni/Al reacts and the exothermic reaction allows the solder preform melting. The final assembled sample and a cross section view of the joint are illustrated in Fig. 1b and 1c respectively.

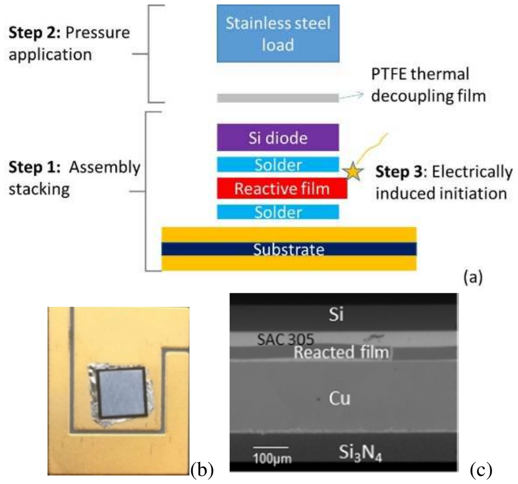

Fig. 1: Schematic illustration of the process steps (for clarity reasons dimensions are not to scale) (a), top view of the assembled sample (b) and cross section view of the joint (c).

The test conditions with various used parameters are presented in Table I. The voids ratio was evaluated for various test conditions by using scanning acoustic microscopy coupled to image treatment software (Image J®). Each value of void ration represents the mean value of three measurements of three samples assembled using the same conditions. The variation between the highest and lowest value for each condition was less than 7%. Backscattered secondary electron microscopy imaging was used to evaluate the joint microstructure and the interfaces for samples realized using the test conditions C2 and C13. Shear tests and I-V measurements were achieved on thick ABB 5SLY12E1200 diodes assembled to the substrate using the test condition C16.

III. Results and discussions

A. Parametric study

The pressure effect on the voids ratio between 110µm thick Infineon IDC51D120T6M diodes assembled on AMB and DBA substrates was evaluated in the pressure range between 0.5kPa and 100kPa by using a 40µm and 60µm reactive foil thickness sandwiched between 25µm SAC305 preforms. As presented in Fig. 2, for all the tested conditions, the increase of the pressure leads to a strong improvement on the joint quality and the voids ratio decreases significantly when the applied pressure changes from 0.5 to 100kPa. This can be explained by the improvement of the solder flow under higher pressure leading to a better surface wettability and voids elimination [8]. Another pressure dependent parameter that can explain this improvement is the contact conductance which increases by increasing the pressure [9]. In fact, higher thermal conductance values induce a better thermal transfer and fewer losses in the air during the joining process that can play a role in the improvement of the joint quality.

Table 1: Various test conditions used for the parametric study.

Test condition	Substrate nature	RF thickness (µm)	Metallization thickness (µm)	Solder nature	Solder thickness (µm) x number	Die thickness (µm)	Pressure (kPa)
C1	Cu/Si$_3$N$_4$/Cu	40	300	SAC305	25 x2	110	13
C2	Cu/Si$_3$N$_4$/Cu	40	300	SAC305	25 x2	110	100
C3	Cu/Si$_3$N$_4$/Cu	40	300	SAC305	25 x2	110	50
C4	Cu/Si$_3$N$_4$/Cu	60	300	SAC305	25 x2	110	13
C5	Cu/Si$_3$N$_4$/Cu	60	300	SAC305	25 x2	110	5
C6	Cu/Si$_3$N$_4$/Cu	60	300	SAC305	25 x2	110	50
C7	Cu/Si$_3$N$_4$/Cu	60	300	SAC305	25 x2	110	100
C8	Cu/Si$_3$N$_4$/Cu	60	300	SAC305	50 x2	110	13
C9	Al/AlN/Al	60	300	SAC305	50 x2	110	13
C10	Al/AlN/Al	60	300	SAC305	50 x2	110	100
C11	FR4/Cu	40	35	SAC305	25 x2	110	13
C12	FR4/Cu	40	70	SAC305	25 x2	110	13
C13	FR4/Cu	60	35	Au$_{80}$Sn$_{20}$	50x2	110	13
C14	FR4/Cu	60	35	SAC305	50x2	110	13
C15	Cu/Si$_3$N$_4$/Cu	60	300	SAC305	25 x2	350	13
C16	Cu/Si$_3$N$_4$/Cu	60	300	SAC305	25 x2	350	100

In the pressure range between 13 to 100kPa, the relationship between the pressure and the voids ratio seems to be linear and the slope can depend from the test conditions. The slope is higher if the void ratio corresponding to the test condition at low pressures is high. Accordingly, the improvement of the joint quality induced by the pressure is more pronounced if the initial value of voids ratio under low pressure is high.

For the next presented results of this parametric study, a pressure of 13kPa was applied since it remains simple to manually apply by using weights on components and does not impact potential pressure sensitive components of the assembled parts. In addition, the voids ratio at this pressure is relatively high and hence, the impact of the other parameters can be simply detected.

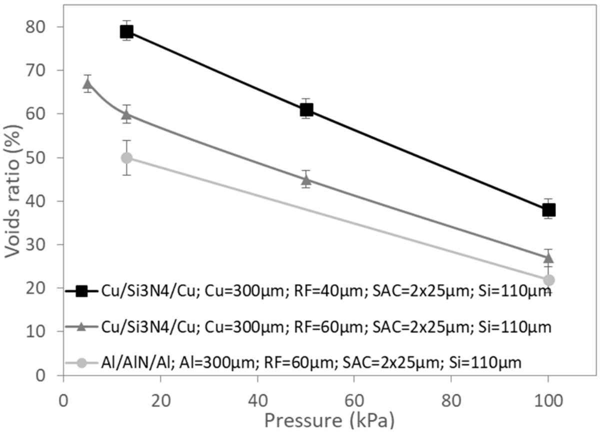

Fig. 2: Voids ratio variation as function of pressure for three test conditions. Each point represents the mean value of three measurements and the standard variation is represented by the bars on the symbols.

The impact of the RF, solder, and substrates metallization and diodes thicknesses on the voids ratio in the joint is illustrated in Fig. 3. In fact, the thickness of each of these elements will have an effect on the melting duration of the solder which in turn will impact the joint quality [10],[11]. A short melting duration during the assembly process will reduce the ability of the solder to flow as well as its surface wettability and will lead to large non wetted surface.

The void ratio decreases from 80% to about 60% for RF thickness of 40 and 60µm respectively. The additional energy induced by increasing the thickness of the reactive foil increases the duration of melting and hence it improves the solder flowing and a better surface wettability is obtained.

In order to evaluate the impact of the solder preform thickness on the void ratio, 25 and 50µm thick SAC preforms were used. At 13kPa applied pressure, and by using a 60µm reactive film to join 100µm silicon die on the Cu/Si$_3$N$_4$/Cu substrate, the value of the voids ratio was 60% and 75% for 25µm and 50µm preforms respectively. This dependence can be explained by the fact that when using a constant energy source (produced by the RF), the increase of the solder thickness will consume additional energy in order to reach the melting temperature as well as for phase changing (enthalpy of fusion). Accordingly, the maximal temperature reached in the thicker solder as well as the melting duration were expected to be lower. As already mentioned, longer melting duration will improve the solder flow and its substrate wettability.

The effect of the copper substrate metallization thickness on the joint quality was evaluated using two different insulating materials (FR4 for thin Cu (<100µm) and Si$_3$N$_4$ for thick Cu

(300µm)). It has been shown that the thickness variation of Cu metallization is significant when using a low thermal conductivity substrate underneath the copper metal layer (like FR4) and can be neglected when using high thermal conductive ceramics [10]. In the same reference, results have also shown that the insulator nature has no impact on the melting duration for Cu thicknesses ≥ 150µm. Hence, the comparison of the metallization thickness effect using both Si_3N_4 and FR4 substrate for thick and thin metallization respectively can be allowed. Using a reactive film of 40µm thickness between two SAC solder preforms of 25µm each under a pressure on 13kPa, the voids ratio in the joint between Si diodes and the substrates was found to be 15%, 25% and 80% for 35µm, 70µm and 300µm copper thicknesses respectively.

The Si diode thickness also affects the void ratio in the joint and a voids ratio of 60% and 73% for 110 and 350µm thick diodes respectively. The increase of the Cu and/or Si thicknesses will consume additional energy and hence the melting temperature and duration of the solder will decrease. This leads to higher voids ratio in the joint. However, we notice that the impact of diode thickness variation in less pronounced than Cu metallization one. This can be explained by physical properties of Si which has lower thermal conductivity as well as its lower specific capacity by density product ($Cp \times \rho$) compared to Cu. Hence, the solder melting duration is less impacted when the diode thickness is changed.

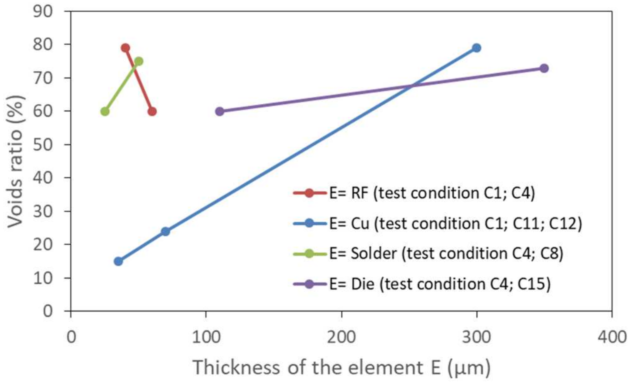

Fig. 3: Impact of the thickness of various element of the assembly (E) on the voids ratio. For all mentioned conditions, the pressure was maintained constant (13kPa).

Finally, the impact of solder and substrate metal nature has been evaluated and the results are illustrated in Fig. 4. A 13kPa applied pressure was used to attach 100µm Si die to the PCB substrate with 35µm Cu thickness by using 50µm $Au_{80}Sn_{20}$ or SAC305 solder preforms and 60µm thick RF. The voids ratio is slightly higher for AuSn solder. While the heat of fusion of the used $Au_{80}Sn_{20}$ (34.2J/g) is lower than SAC305 (67J/g), which can be advantageous from thermodynamic point of view, its fusion temperature as well as the product of its density and its specific capacity are higher and lead to a slightly lower duration of melting compared to SAC and hence a negligible variation in voids ratio is detected. Meanwhile, varying the substrate metallization nature can have a more significant impact on the solder preform melting duration and the joint quality. This was evaluated by comparing DBA and AMB substrates. When Al metallization is used, the lower voids ratio can be explained by its lower thermal conductivity as well as its lower $Cp \times \rho$ product compared to copper, which strongly impact the heat transfer mechanisms in the package.

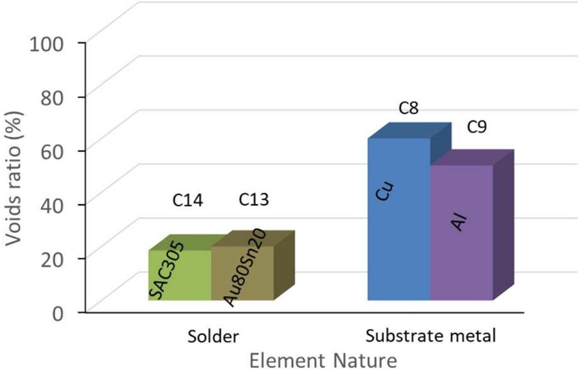

Fig. 4: Impact of the solder and the substrate metal nature on the voids ratio. For all mentioned conditions, the pressure was maintained constant (13kPa).

B. *Microstructure evaluation*

The joint microstructure realized using the C2 test condition parameters is illustrated in Fig. 5. Red arrows in Fig 5a point some voids at a specific location while Fig 5b shows in another location in the joint, some cracks in the reacted film filled with the solder. The latter observation can prove that the energy released during the reaction of the films is high enough to induce the melting of the solder for a sufficient duration that allows the solder to flow in the gaps. The focus on the interfaces between the solder and the substrate and the one between the solder and the Si diode are presented in Fig 5 c and d respectively. It can be shown that intermetallic compounds are mainly formed between the solder and the Ag finish layer of the diodes and between the solder and the reacted film (blue arrows).

Otherwise, the microstructure of $Au_{80}Sn_{20}$ joint using C13 condition is compared to the one realized using a conventional solder reflow process in an oven in air. In the conventional process (Fig. 6a), two coarse phases can be distinguished with a gold rich phase that appears in clear grey (ξ phase, Au_5Sn) and a dark tin rich phase (δ phase, AuSn), while very homogenous solder joint is observed using the reactive film (compared at the same scale) (Fig. 6b). This can be explained by the slower cooling rate in conventional soldering. At a higher magnification, a very fine lamellar eutectic structure can be observed when RF is used (Fig. 6c) suggesting the two ξ and δ equilibrium phases for this composition. These phases grow simultaneously and form parallel plates in grain-like colonies with a spacing between these plates of about 100nm. It has been shown that the fine microstructure of the solder can induce a positive impact on the joint mechanical properties [12].

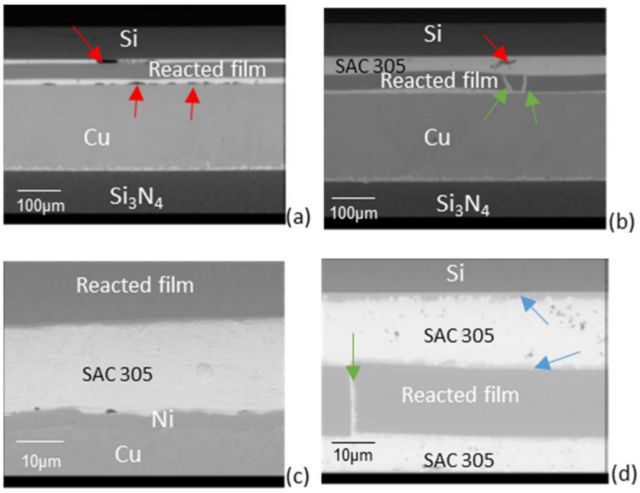

Fig. 5: Global view of the cross section of the assembly at two different locations in the joint (a) and (b). Higher magnification at the interface solder/substrate (c) and solder/Si diode (d). Red arrows point some of the voids in the joint, green arrows point the fracture of the reacted film filled with solder and blue arrows indicate the intermetallic location at the interface between the solder and the Si diode and between the solder and the reacted film.

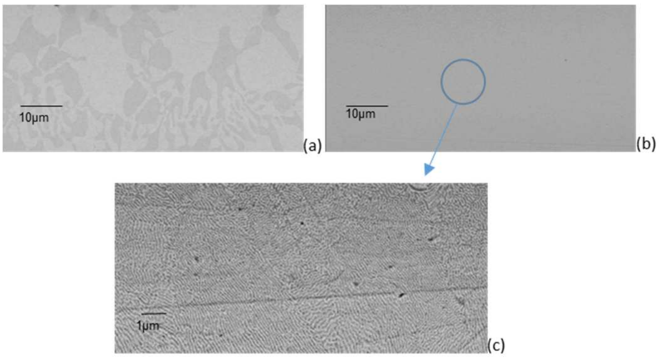

Fig. 6: $Au_{80}Sn_{20}$ solder microstructure with conventional soldering reflow process (a) and using reactive films soldering process (b). High magnification on the latter joint showing nanometer size plates (c).

C. Evaluation of shear strength and process impact on device initial electrical properties

The shear test equipment consists in a load-applying instrument with an accuracy of ±5 % of full scale. A linear motion force is used and the direction of the applied force is parallel with the plane of the substrate. The shear tool was set to 100µm height over the substrate and the shear test velocity was fixed to 100µm/s. For the shear tests three samples using the 350µm thick ABB diodes attached to AMB substrate by using the test condition C16 were evaluated. All the diodes were partially fractured without being able to completely snatch them (see Fig. 7). The applied forces until the first fracture of the diode were 38, 44 and 66kgf which correspond to strength values of 9.5, 11.1 and 16MPa respectively. The real shear strength value will be greater than the aforementioned ones. However, these values remain largely higher than the requirement of the MIL-STD-883H where the shear force should be higher than 5kgf for components larger than 4mm^2 [13].

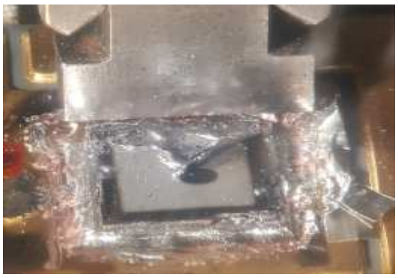

Fig. 7: Die fracture after the shear force application (66kgf).

In a previous paper [10], the authors have shown that the surface of the semiconductor can reach a temperature of about 400°C for a duration less than 1ms. In order to evaluate the process impact on the electrical properties of the attached semiconductor, I-V curves of ABB diodes attached to AMB substrate by using the condition C16 and the conventional soldering process were compared. As illustrated in Fig. 8, the process using the reactive foil does not significantly modify the electrical characteristics of the diodes at initial time (t_0). The authors are aware that additional in depth evaluations should be performed in order to be sure that the process does not create any weaknesses in the semiconductor devices that can appear under repetitive functional power cycles or during the aging.

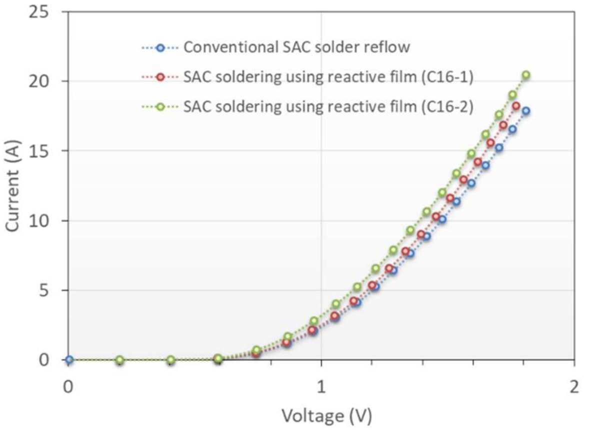

Fig. 8: I-V characteristics of ABB diodes using conventional soldering reflow and reactive film soldering using C15 conditions (2 tests).

III. Conclusion

Joining electronics components using reactive films and solder preforms is a promising and economically viable technology for high temperature electronics applications and for assembling electronics packages on massive structures.

The impacts of pressure, assembled material thicknesses and nature on the voids ratio in the joint were evaluated. All the aforementioned results can be explained by the fact that the flow ability of solders is improved by increasing the applied pressure and the solder melting duration, leading to a better joint quality. The solder melting duration can be longer if the thickness of the reactive film is increased, the die, the substrate metallization and the solder preforms thicknesses are decreased and if the thermal conductivity and the product of the density by the specific capacity of the assembled elements are reduced. Compared to conventional soldering process, a finest microstructure of the solder can be obtained when using reactive films. The shear strength of the attached devices are largely higher than the MIL-STD-883H requirements. The process impact on the electrical properties of the assembled diodes was compared with a commonly used solder reflow assembly and results show a negligible variation.

Meanwhile, additional investigations should be done in the future in order to address the three following tasks:

- To reduce the void ratio by additional pressure increasing, preheating of the substrate, increasing the foil thickness as well as the initiation of the foil in vacuum.
- To evaluate the impact of the intermetallic compounds detected between the solder and the diode and between the solder and the reacted films on the joint reliability.
- To validate that the process does not create any weaknesses in the device that can appear under repetitive functional power cycles or during thermal aging.

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