Characteristics of Organic-Based Thermal Interface Materials Suitable for High Temperature Operation

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Abstract

Historically, for semiconductors subject to standard operating temperatures--which tend not to exceed 125°C--the T_g (glass transition temperatures) of the organic packaging materials protecting the chips is usually around 175°C. Given that, when it comes to electronics operating at high temperatures—typically an environment where the ambient temperature exceeds 200°C—the use of organic materials is generally prohibited due to rapid degradation. At those elevated temperatures, the packaging materials selected are generally composed of metals and ceramics but these materials come with their own shortfalls as well as higher material and manufacturing costs. Therefore, it would be desirable if there were 'ruggedized' versions of the organic compounds so commonly used in semiconductor packaging but available for more extreme temperatures, both to reduce cost and package footprint.

Meanwhile, the demands from recent developments in high performance computing (HPC) and high-speed data networks means a greater need for increased power and thermal dissipation coupled with very large package body sizes to accommodate the high I/O count. The latest in server microprocessor (MPU) products can easily generate up to 300W during operation, and the heat generated must be quickly transported away from chip to prevent the threat of thermal shutdown. The thermal dissipation issue is controlled by the use of heat spreaders and heat sinks, both of which are intended to make contact with the back-side of a flipped MPU via a thermal interface material (TIM), as part of a large die, large body-size flip-chip ball grid array (FCBGA) package.

The thermal interface materials discussed here are examples of organic engineered materials that are capable of withstanding higher operating temperatures than typically seen by semiconductors encased in organic-based packaging. This paper will look at the key material and mechanical attributes for a good thermal interface material, examines the pros-and-cons of various thermal interface material formulations, and discusses the factors for reliable thermal dissipation performance.

Key words
Materials, organic, packaging, ruggedized, semiconductor, thermal interface

I. Introduction

The difficulty in using organic materials for high temperature—exceeding 150°C to well over 200°C—is obvious, given the glass transition temperature (T_g) of qualified organic materials in the production of semiconductor packages tends to be no higher than 175°C [1], [2].

But even without the addition of elevated temperatures, the high-power demands of high-performance computing (HPC) and modern data networks means the microprocessors (MPUs) in these advanced systems can generate enough heat to risk thermal shutdown.

To control the thermal dissipation needs of these MPUs, heat spreaders and heat sinks are employed as part of the packaging system, both of which are intended to make physical contact with the back-side of a flipped chip through a thermal interface material (TIM).

Therefore, a set of advanced TIM candidates were evaluated on a large body-size flip chip ball grid array (FCBGA) under several criteria: ease of use in assembly FCBGA, withstanding a battery of reliability test, and thermal characterization and performance post-reliability testing. The optimal TIM candidate should be able to pass these criteria and more.

II. Experimental Process

A. Materials Selection

As shown in Table I, three organic-based thermal interface materials (TIMs) were selected for thermal characterization and optimization. TIM candidate #1 is a current production material used for heat dissipation for large die, large body-size flip-chip ball grid array (FCBGA) packages. TIM candidate #2 differs from the current production material by being in an organic film format but uses the same type of alumina (Al_2O_3) filler. TIM candidate #3 used graphite as a thermal conductor--which theoretically offers an order of magnitude superior performance compared to alumina—but was only available in an organic film instead of a paste. Thus, the selection of TIM candidate #2 served as an intermediate comparison between candidates #1 and #3, by having the same thermal conductivity filler (alumina) as #1 but in the same material form (an organic film) as #3.

Table I: TIM Candidates

TIM candidate	#1	#2	#3
Thermal Filler Type	alumina	alumina	graphite
Material type	Paste	Film	Film
Viscosity (Pa)	250	n/a	n/a
Modulus (MPa) @25°C	0.4	192	n/a
Hardness (Asker C)	12	65	40~50
Min thickness	0.036mm	0.025mm	0.15mm
Thermal conductivity	3.8 W/mk	5.5 W/mK	40~90 W/mK
Post-mounting cure	90min@125C	n/a	n/a

B. Evaluation Methodology

The large die, large body-size FCBGA package test vehicle used for evaluation was a 50x50mm external heat sink FCBGA (EHS-FCBGA), as shown in Fig. 1. Fig. 1(a) also shows this package structure using a 4/2/4 build-up (four thin build-up layers on each side of a rigid core) organic substrate. The experimental methodology was to first evaluate process characterization of each candidate in order to optimize conditions for process assembly. Fig. 2(a) shows the typical process flow for applying TIMs, and further intermediate steps regarding TIM placement are illustrated in Fig. 2(b).

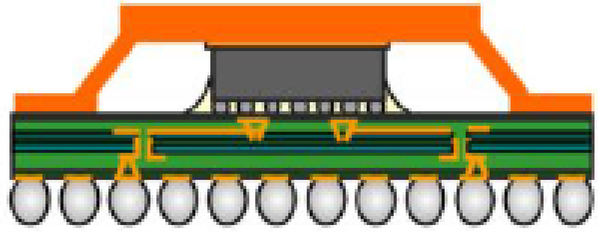

Fig. 1(a): EHS-FCBGA illustration.

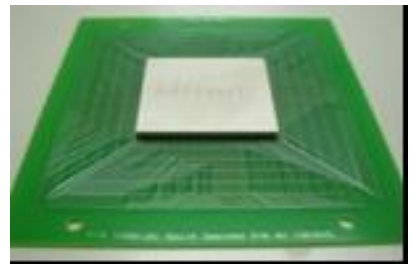

Fig. 1(b): Photo of an EHS-FCBGA.

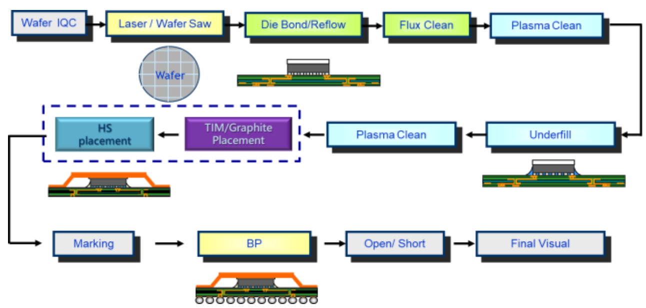

Fig. 2(a): Process flow for using TIMs.

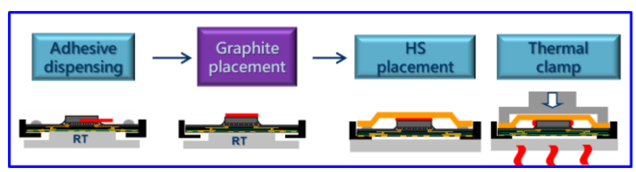

Fig. 2(b): Further detailed steps on TIM placement.

Once process optimization was achieved, thermal test chips were then assembled into the package test vehicles for thermal measurements. In addition to the thermal characterization, there were plans to subject the TIMs to package reliability testing—MRT (moisture reliability testing) coupled with TCT (temperature cycling test), HTS (high temperature storage), and HAST (highly accelerated stress testing). Post-reliability tests, the test vehicles would be examined for TIM coverage degradation and consequently any impact on thermal performance.

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C. Process Characterization

The results from process characterization are shown in Table II. For TIM candidate #2, the results pointed to issues with adequate TIM coverage during package assembly. Upon further examination, it was theorized that two likely causes may be too thin a recommended bond line thickness and the elevated material hardness (note the comparison in Table I) which may have together have caused difficulties in maintaining adequate coverage on backside of the chip. Therefore, further evaluations going forward in this particular set of experiments focused only on TIM candidate #1 (current production material) and candidate #3 (graphite film).

Table II: Process Characterization Results

	Process Setting			Initial TIM Coverage			OS Yield
TIM	Sample Size	Clamp Setting	Clamp Temp./°C	Min.	Max.	Avg.	
#1	15	1.9Kg	125	99.9%	99.9%	99.9%	100%
#2	15	1.9Kg	125	57.0%	95.4%	78.8%	100%
#3	15	5.4Kg	150	98.2%	99.9%	99.6%	100%

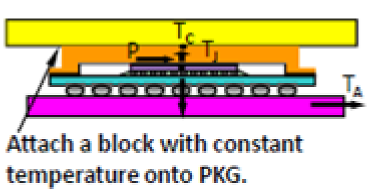
D. Thermal Evaluation

As explained earlier, thermal test chips were assembled into the EHS-FCBGA test vehicles using TIM candidates #1 and #3 for thermal measurements along with the battery of reliability tests—MRT, TCT, HTS, and HAST--to examine the TIM coverage before and afterwards to determine the level of thermal degradation.

The thermal measurement focused on thermal resistance from junction to case—or Θ_{JC}-- to get the thermal performance of two targeted TIM materials.

Fig. 3(a) are photographs of the thermal test equipment, while Fig. 3(b) illustrates the technique to obtain Θ_{JC} readings. Fig. 4 shows the thermal test chip used in these evaluations. The input power used for the thermal measurements was 250W.

Fig. 3(a): Thermal test equipment.



$$\theta_{JC} = \frac{T_J - T_C}{P} ;$$

Fig. 3(b): Illustration of how Θ_{JC} measurements were taken.

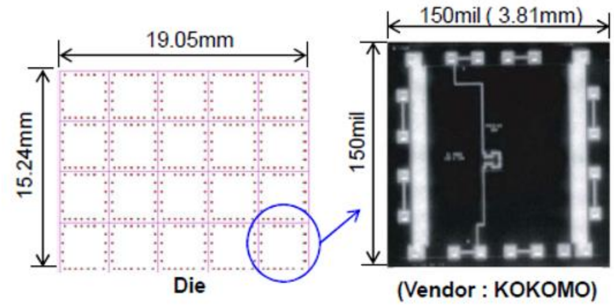


Fig. 4: Thermal test chip.

E. Reliability Testing

Table III shows the criteria used for each reliability test, which are based on industry standards, also listed in the table.

Table III: Reliability Tests

Reliability Test	Temperature Range, °	Relative Humidity, %	Time Period, Hours	Number of Cycles	Pressure, psia	Industry Standard
Moisture Sensitivity, Level 4 (MRT)	30	60	72	n/a	n/a	IPC/J-STD-020
Temperature Cycling, condition B (TCT)	55 to 125	n/a	n/a	up to 1000	n/a	JESD22-A104
High Temperature Storage (HTS)	150	n/a	1000	n/a	n/a	JESD22-A103
Highly Accelerated Temperature and Humidity Stress Test (HAST)	130	85	96	n/a	33.3	JESD22-A110

Fig. 5 illustrates the procedure for obtaining the Θ_{JC} results, as per JEDEC 51 standard, before and during reliability testing. Also note the "Thermal Calibration" step in the figure. This step was necessary to obtain the calibration curve based on changes in voltage over temperature for the correct junction temperature (T_J) reading for the EHS-FCBGA test vehicle.

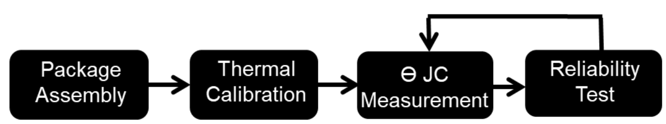


Fig. 5: Thermal measurement process flow.

F. Thermal Measurements and Reliability Test Results

Table IV present the results of thermal measurements and reliability testing. TIM candidate #3 (the graphite-based film material) offered more than 50% improvement in Θ_{JC} readings compared to TIM candidate #1 (the current production material), and the film maintained good chip backside coverage throughout the reliability tests. On the other hand, TIM candidate #1 showed a decrease in backside coverage after HTS testing, resulting in a Θ_{JC} thermal degradation of about 15% when compared to initial measurements.

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Table IV: Experimental Results

Input Items		T0			MSL4+TCB 700			MSL4+TCB 1000			HTS 1000hrs			uHAST 96hrs		
TIM Type	S/S	Theta JC	TIM Cov	BLT	Theta JC	TIM Cov	BLT	Theta JC	TIM Cov	BLT	Theta JC	TIM Cov	BLT	Theta JC	TIM Cov	BLT
#1	15	Min:	Min:	AVG: 98.9um	Min:	Min:	--	Min:	Min:	AVG: 82.9um	Min:	Min:	AVG: 80.2um	Min:	Min:	AVG: 97.6um
		0.13	99.90%		--	85.40%		0.14	70.50%		0.15	51.20%		0.13	99.70%	
		Max:	Max:		Max:	Max:		Max:	Max:		Max:	Max:		Max:	Max:	
		0.15	99.90%		--	95.40%		0.15	89.60%		0.17	56.80%		0.15	99.70%	
		Ave:	Ave:		Ave:	Ave:		Ave:	Ave:		Ave:	Ave:		Ave:	Ave:	
		--	99.90%		--	90.50%		--	78.70%		--	54.00%		--	99.70%	
#3	15	Min:	Min:	AVG: 176.3um	Min:	Min:	--	Min:	Min:	AVG: 186.1um	Min:	Min:	AVG: 182um	Min:	Min:	AVG: 183.1um
		0.058	98.30%		0.058	97.30%		0.058	96.50%		0.058	94.80%		0.058	98.00%	
		Max:	Max:		Max:	Max:		Max:	Max:		Max:	Max:		Max:	Max:	
		0.066	99.90%		0.066	98.30%		0.066	97.90%		0.066	95.10%		0.066	98.90%	
		Ave:	Ave:		Ave:	Ave:		Ave:	Ave:		Ave:	Ave:		Ave:	Ave:	
		--	99.60%		--	97.70%		-	97.30%			95%		--	98.50%	

III. Conclusion

As mentioned in the previous section, the current production material--TIM candidate #1--showed a decrease of chip backside coverage, especially after HTS testing. This issue is not uncommon [3], and further action may be required to optimize the adhesive pattern to maintain the TIM coverage through the span of reliability test time periods.

In all, the graphite-based film material offers more than 50% Θ_{JC} thermal improvement comparing to current alumina paste qualified for production and sustained good coverage through the reliability tests. However, more criteria need to be evaluated before TIM candidate #3 could be incorporated into a high-volume manufacturing process: material and usage costs, and package and chip size limitations due to increased hardness levels are but two issues to consider. Such considerations may be part of the next set of future evaluations.

Acknowledgment

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References

[1] B. Murrell, "Advanced high temperature semiconductor packaging material based on PBO foam technologies," *McNair Scholars Journal:* Vol. 10: Iss. 1, Article 10, 2006.

[2] O. Aviño-Salavado, W. Sabbah, C. buttay, H. Morel, and P. Bevilacqua, "Evaluation of printed-circuit boards materials for high temperature operation," in *Proc. High Temperature Electronics Network (HiTEN 2017)*, Cambridge, UK, 2017.

[3] F. (C.-P.) Tung, M. (C. Y.) Lu, A. (C. Y.) Lan, and S. (C. A.) Pan, "Assembly challenges for 75x75mm large body FCBGA with emerging high thermal interface material (TIM)," in *Proc. 67th IEEE Electronic Components and Technology Conference*, Lake Buena Vista, CA, 2017, pp. 130–135.

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