High Temperature Memory Design, Implementation, and Characterization in 1µm SiC CMOS Technology

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Abstract
Electronic systems capable of withstanding high temperature environments are in high demand in various applications such as logging-while-drilling (LWD) systems and embedded electronics which are in the core of gas turbine engine controls. Designing memory that can process massive amounts of data in harsh environments while consuming low power opens doors for next generation, smart, high temperature electronic systems. In this work, a CMOS based six transistor (6T) static random-access memory (SRAM) cell is designed and implemented in a state-of-the-art SiC 1µm triple well CMOS process. The designed SiC SRAM cell performance has been characterized for different values of cell ratios (CR) [0.5, 0.6, 1, 1.5, 2, 2.5] and pull-up ratios (PR) [1, 2, 3, 4, 5, 6] to determine the cell size with optimal performance parameters. Static noise margin (SNM) values for the different combinations of CR and PR are calculated using the model developed by Seevinck, et. al. [13]. The highest SNM values observed at 25°C and 300°C are 4.71 V and 4.65 V, respectively. Read static noise margin (RSNM) values of 1.94 V and 1.90 V are achieved at 25°C and 300°C, respectively. Analysis of measured data shows that the optimum cell size is with a CR of 2.5 and a PR of 6. However, these results are significantly impacted by highly resistive ohmic contacts.

Keywords
High Temperature, Memory, Noise Margin, Silicon Carbide CMOS, SRAM

I. Introduction
Decades of research and development of wide bandgap (WBG) semiconductors has paved the way to implementation of these materials in high temperature, high frequency, high voltage, and radiation hardened applications. Silicon carbide (SiC) and gallium nitride (GaN) are the two most commonly used and produced WBG semiconductor materials. SiC has emerged as the most mature of the WBG semiconductors with the release of commercial 6H-SiC bulk substrates in 1991 and 4H-SiC substrates in 1994 [1].

Research into SiC ICs began with power electronics being the central focus. Specifically, the key motivation was to achieve heterogeneous integration of SiC power die and SiC gate driver circuitry in a single power module. However, there has been a growing demand for high temperature capable circuitry in a multitude of other applications.

SiC is particularly suited for these applications due to its intrinsic carrier concentration being approximately 19 orders of magnitude lower than silicon [2]. This leads to SiC transistors having lower leakage current than bulk silicon devices and is paramount in achieving high temperature operation. The maximum operating temperatures of bulk silicon and silicon-on-insulator (SOI) are limited to approximately 150°C and 300°C, respectively [3], [4]. With SiC ICs, this boundary is extended to over 500°C for both analog and digital circuitry [5]-[7].

Leveraging the high temperature capabilities of SiC ICs is crucial to automotive, aerospace, deep well drilling, and wireless telemetry systems [8]. Although building blocks for extreme environment data acquisition have been demonstrated in [9], a memory module is necessary to enable data storage and therefore a more robust electronic system. This work will demonstrate the design and measurement results for a six transistor (6T) static random-access memory

(SRAM) cell using a triple-well, 1 µm single poly, single metal (1P1M) SiC CMOS development process fabricated at Fraunhofer IISB.

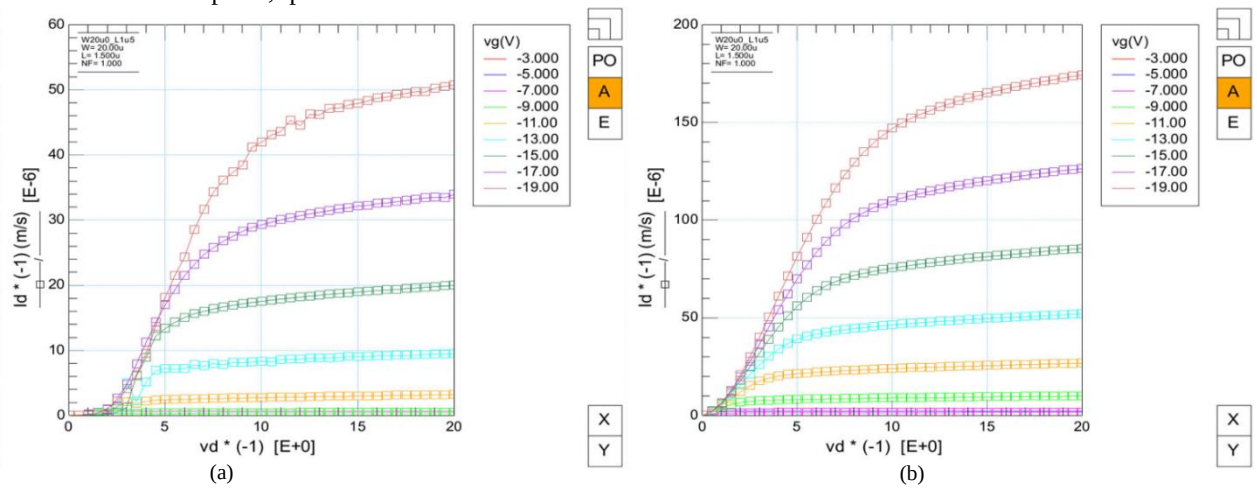
II. SiC Integrated Circuits (IC) Fabrication and Challenges

SiC crystallizes in over 250 different crystal lattice structures (polytypes), each of them having different and unique electrical characteristics. Polytypes are divided into three basic crystal structures; cubic (C), hexagonal (H), and rhombohedral (R). Due to commercially available wafers being 4H-SiC and fabrication issues being prevalent with other polytypes, research at the IC level has primarily been focused on the 4H-SiC polytype. The strength of the bonds between silicon and carbon atoms results in less space between atoms and a larger bandgap than silicon alone. Due to being a wide bandgap material, SiC has a higher critical electric field which improves breakdown voltage. Simultaneously, it has higher thermal conductivity and less susceptibility to radiation.

However, the drawbacks of having stronger bonds are higher ionization levels for dopants, partial ionization at room temperature, and very low diffusion rates. Therefore, ion implantation is the only option available for adding local dopants to the wafer and controlling well concentrations. Annealing is required as a subsequent step to ion implantation. Recursive ion implantation followed by annealing leads to permanent damage in parts of the SiC crystal structure that impacts the performance of a device [10]-[12].

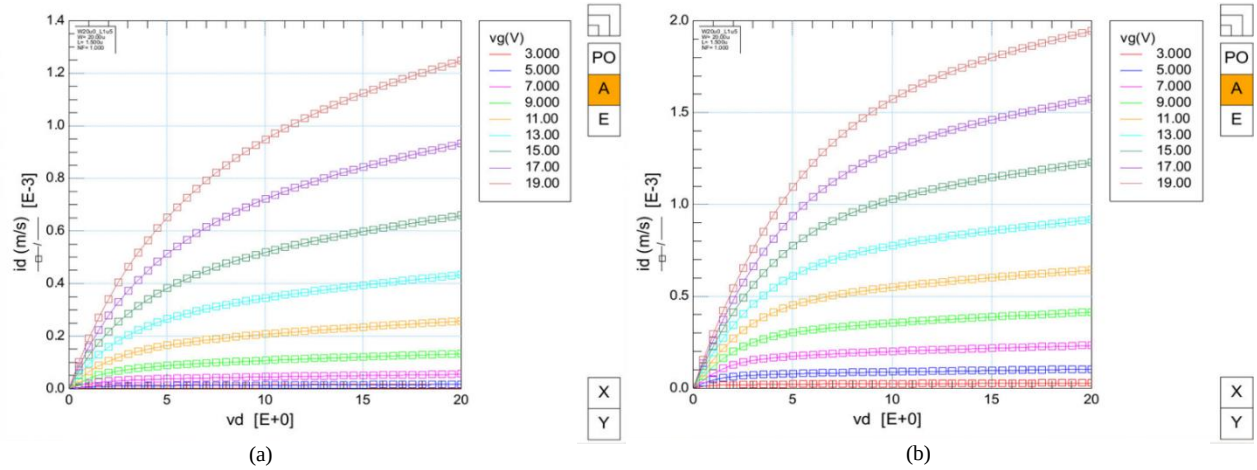
Processing of low resistance ohmic contacts is one more challenge in SiC. Achieving high active p+-doping concentrations on 4H-SiC through ion implantation remains a challenge due to compensation with ion-implantation generated defects. This effect hampers the fabrication of ohmic contacts by tunneling of carriers through the metal contacts comparable to the approach taken in silicon. The memory cells are highly sensitive to the contact resistance of the P+ ohmic contacts when short channels are used. Similarly, the sheet resistance of the P+ regions is high due to compensation effects and incomplete ionization even at 300°C. Examples of the output curves for MOSFETs fabricated on this run are shown in Figs. 1 and 2.

It is evident that contact resistance of the PMOS transistors



(a) (b)

Fig. 1. The output characteristics for a 20µm width and 1.5µm channel length PMOS (a) 25°C (b) 300°C.



(a) (b)

Fig. 2. The output characteristics for a 20µm width and 1.5µm channel length NMOS (a) 25°C (b) 300°C.

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reduces with increasing temperature as depicted in Fig. 1(b). However, ideal ohmic behavior still cannot be achieved at 300°C. The result is a noticeable degradation in the performance of PMOS devices. This is largely a result of the unintentional over-etching of the P+ diffusion region during device fabrication which results in a significant increase in drift region resistance that may also have a detrimental effect on the contact formation process.

III. SRAM Cell Design Summary

Stability and cell area are the two important aspects for SRAM cell design. Cell stability is usually defined using static noise margin (SNM), which is the maximum DC noise voltage that can be tolerated by the cell without having any effects on the stored bit. The bit cell, shown in Fig. 3, is most vulnerable to static noise voltage when it is in the read mode. This is due to pre-charged bit lines being connected to the storage nodes that can increase the potential of the storage nodes with a logic '0' value and cause a stored bit to flip to a logic '1'. In order to perform a nondestructive read operation, the ratio of current driving strength for the access transistor as compared to the pull-down transistor must be carefully selected. This is critical in order to avoid unintentionally increasing the voltage of the storage node when it ideally has a logic '0'. The ratio between the access transistor and pull-down transistor is termed cell ratio (CR), which is expressed below.

$$Cell\ Ratio = \frac{W_{PD}/L_{PD}}{W_{AD}/L_{AD}}$$

W_{PD}, L_{PD}, W_{AD}, L_{AD} are the widths and lengths of the pull-down and access transistors, respectively.

Similar to CR, there is another sizing parameter referred to as the pull-up ratio (PR). This term refers to the ratio of the pull-up transistor to the access transistor. The restoring strength (current driving capability) of the pull-up transistor must be higher than the strength of access transistors for a cell to perform a write operation. An expression for the PR is provided below. W_{PU} and L_{PU} are the width and length of the pull up transistors, respectively.

$$Pull\ Up\ Ratio = \frac{W_{PU}/L_{PU}}{W_{AD}/L_{AD}}$$

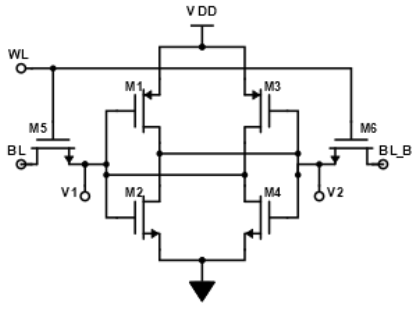


Fig. 3. 6T SRAM cell schematic.

Due to the nature of the fabrication process and the early development phase of SiC integrated technology, multiple variants of SiC SRAM cells have been implemented in this fabrication run. Different values of CR (0.5, 1, 1.5, 2, 2.5) and PR (1, 2, 3, 4, 5, 6) are selected in order to determine the optimal cell size from the various performance parameters measured over temperature for each cell. SNM values for the different combinations of CR and PR are calculated using the model developed by Seevinck, et. al. [13]. Each cell variant is designed using minimum length NMOS and PMOS transistors (L = 1µm). Fixed width NMOS (W=4µm) is used in the cross-coupled inverters, where the width of the PMOS increases to increase the pull-up ratio from 2:1 to 12:1.

Layouts for the cells are optimized for this process but are affected by the limitation of the availability of only a single metal layer for routing. Thus, poly has been used as a second routing layer. Poly is a more resistive routing layer (R_{sh} = 13 Ohm/sq.) and an effort was made to minimize its use in the various layouts. The layout of an SRAM cell having a CR = 0.5 and PR = 3.0 is shown in Fig. 4. In order to make bitline routing less resistive, only the metal layer is used. The downside to this layout decision is that the power rails of a cell are routed on poly wherever bitline is crossing. The chip micrograph of the fabricated SRAM cell is shown in Fig. 5.

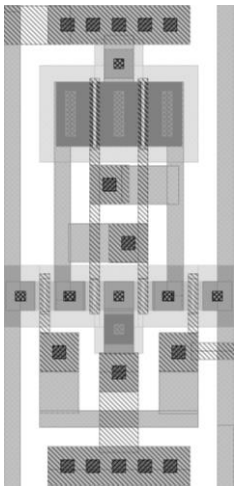


Fig. 4. SRAM cell layout.

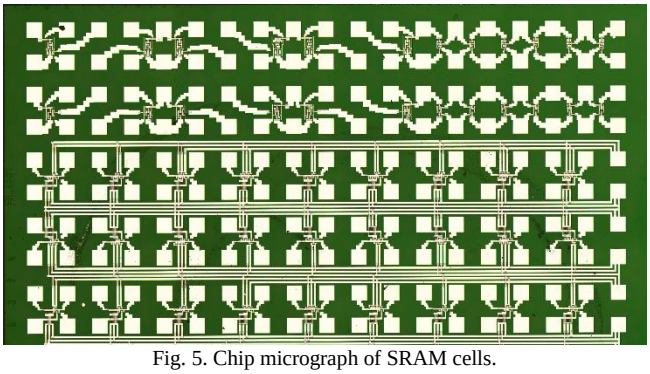


Fig. 5. Chip micrograph of SRAM cells.

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V. Measurement Results

Tables I through V show the effect of the CR and PR on SNM and RSNM. The read noise margin increases with cell ratio. The hold margins are not significantly affected by the changes in cell ratio. This result is expected since the read operation is dependent on the cell ratio. A larger cell ratio requires a larger pull-down network, which means the node storing a logic '0' is robust to any unwanted signals such as noise introduced by the bitlines during the precharging state. The pull-up ratio has a significant effect on all noise margins because it impacts the strength of the cell to retain its stored value, particularly on a node storing a logic '1'. During write operation the bitline is pulled to ground and flips the node data to a logic '0' from a logic '1'. The strength of PR determines the difficulty of writing data or flipping the state of the cell. These cells are significantly affected by the described high P+ contact resistance and do not exhibit any significant change in write noise margin (WSNM) with increasing PR.

Table I: The SNM & RSNM at CR = 0.5.

PR	SNM(V)		RSNM(V)	
	25°C	300°C	25°C	300°C
1	4.13	3.98	1.45	1.42
2	4.47	4.30	1.53	1.49
3	4.39	4.10	1.59	1.51
4	4.44	4.24	1.70	1.68
5	4.53	4.49	1.79	1.73
6	4.72	4.54	1.84	1.76

Table II: The SNM & RSNM at CR = 1.

PR	SNM(V)		RSNM(V)	
	25°C	300°C	25°C	300°C
1	4.21	4.00	1.49	1.46
2	4.51	4.12	1.58	1.43
3	4.43	4.32	1.64	1.57
4	4.49	4.47	1.76	1.64
5	4.54	4.52	1.86	1.79
6	4.66	4.61	1.89	1.84

Table III: The SNM & RSNM at CR = 1.5.

PR	SNM(V)		RSNM(V)	
	25°C	300°C	25°C	300°C
1	4.29	4.26	1.52	1.48
2	4.61	4.53	1.62	1.51
3	4.59	4.49	1.68	1.62
4	4.62	4.57	1.79	1.69
5	4.69	4.63	1.89	1.82
6	4.73	4.69	1.92	1.88

Table IV: The SNM & RSNM at CR = 2.0.

PR	SNM(V)		RSNM(V)	
	25°C	300°C	25°C	300°C
1	4.27	4.21	1.51	1.48
2	4.35	4.28	1.59	1.55
3	4.42	4.39	1.68	1.62
4	4.49	4.43	1.78	1.70
5	4.55	4.52	1.82	1.83
6	4.67	4.61	1.92	1.90

Table V: The SNM & RSNM at CR = 2.5.

PR	SNM(V)		RSNM(V)	
	25°C	300°C	25°C	300°C
1	4.31	4.28	1.58	1.51
2	4.39	4.27	1.65	1.62
3	4.46	4.3	1.77	1.72
4	4.51	4.42	1.83	1.79
5	4.57	4.53	1.85	1.82
6	4.71	4.65	1.94	1.90

Fig. 6 shows the region that is affected by the lower pull-up strength of the inverter. In all of the combinations of CR and PR, the pull-down network always dominates and the pull-up network cannot pull the node to VDD. In the implemented cell designs, the minimum CR is equal to 0.5 which means the pull-down network is at its lowest drive strength and the maximum PR is set to 6.0. A PR of 6.0 indicates that the pull-up network is the strongest. CR and PR values are selected based on the PMOS to NMOS ratio of 5:1 and 6:1. However, due to the unexpected drive strength ratios of fabricated PMOS and NMOS being 23:1 at 25°C and 10:1 at 300°C, the pull-up strength is lower for all the implemented CR and PR combinations. At high temperatures, the device performance gets better as shown in Fig. 1 and Fig. 2. Therefore, a minor increase in the pull-up network's performance can be noticed in Figs. 6 and 7.

All the measurements are performed on a Signatone probe station. A Keysight B1500 DC curve tracer has been used for sweeping the input voltages. Room temperature measurements were performed on all of the SRAM cells and then high temperature measurements were subsequently performed. At temperatures above 300°C, the threshold voltage of NFETs dropped below 1 V and the threshold of PFETs lowered down to -4 V from -8 V (at room temperature), which results in lower SNM for the cells. A lower threshold for NFETs leads to the storage node being pulled down stronger than the PFETs can pull it up.

An SNM of 4.71 V at 25°C and 4.65 V at 300°C demonstrates that the implemented cells have the capability to hold the stored data at high temperatures and the cross-coupled inverters are retaining their bistable states. An RSNM of 1.94 V at 25°C and 1.90 V at 300°C for CR=2.5 and PR=6.0 shows robustness against the noise generated from precharged bitlines during the read operation. However, WSNM cannot be evaluated because of the unanticipated poor drive strength of PFETs. The performance of the SRAM cell is expected to improve significantly with the improvement in the SiC CMOS process.

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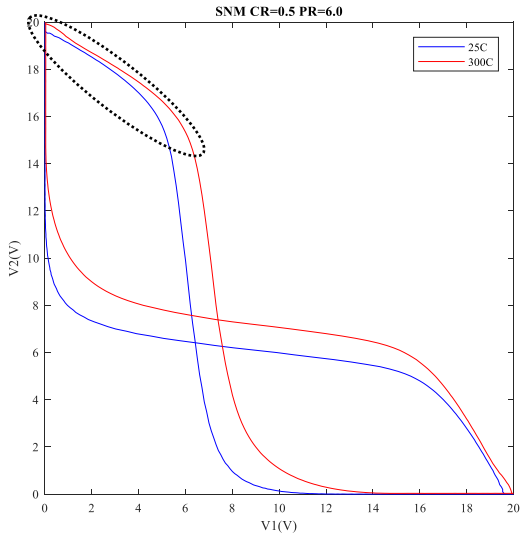


Fig. 6. Region of SNM affected by high P+ contact resistance.

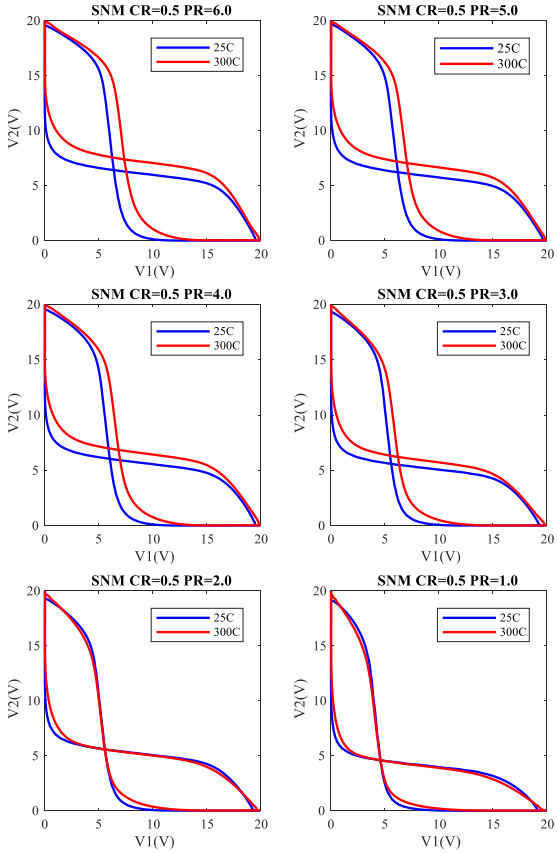


Fig. 7. SNM at 25°C and 300°C.

VI. Conclusion

This work has presented the design and fabrication of a SiC 6T SRAM cell with multiple variants. A few of the key fabrication challenges experienced with the developing 1 µm SiC CMOS process technology have been discussed. Despite the processing issues, the SRAM cells were functional and have been measured between 25°C and 300°C. The highest SNM value of the SRAM variants was better than 4.65 V over the temperature range. Furthermore, the highest RSNM was better than 1.90 V for the same range of temperatures. The results yield an optimum cell size with a CR of 2.5 and PR of 6. As the SiC CMOS process is developed and refined, the performance of the SRAM cells are expected to improve. In particular, an improvement in the P+ contact resistance will yield a noticeable improvement.

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