Ultraviolet LED Multi-Chip Module Based on Ceramic Substrate

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Abstract

A high power ultraviolet (UV) light emitting diode (LED) multi-chip module package based on aluminum nitride (AlN) and alumina (Al_2O_3) is presented. The AlN substrate with a high thermal conductivity of up to 180 W/(m·K) and LED chips based on a copper alloy provide superb thermal management and heat extraction. Efficient cooling is an important prerequisite for the increase of extractable optical power and decrease of thermally induced wavelength shift. A design of a stackable module featuring arrays of 7×2 indium-gallium-aluminum-nitride UV LED chips at 395 nm is developed. This configuration of sub-modules allows for the scalable assembly of line sources with different lengths. Applications using UV LEDs cover market segments such as curing of adhesives, inks and coatings, sterilization of medical equipment and treatment of potable water, as well as various uses in chemical detection, biochemical analytics and spectroscopy.

Thermal and thermo-mechanical modelling of the sub-mount is conducted using finite elements analysis. Die attach using eutectic gold-tin solder, lower melting tin-lead solder and silver-filled adhesive are compared with respect to optical output power and wavelength drift. Mechanical strength and structure of the resulting joints are investigated using shear force measurements, cross-sectioning and micro-tomography. An optical output power of 7.7 W is achieved using a cluster of 14 LED chips at 1050 mA resulting in a peak irradiance of 30.8 W/cm² at the LED surface with respect to the footprint and pitch of the attached chips.

Key words: solid state lighting, ceramic packaging, ultraviolet light emitting diode, ceramics

Introduction

UV-sources are used in a wide field of applications such as the curing of adhesives, inks, coatings and industrial paints, the sterilization of medical equipment and the treatment of potable water. Furthermore such light sources are needed for a various uses in chemical detection, biochemical analytics and spectroscopy. Currently high power mercury gas-discharge lamps are used to cover this wavelength range. Due to the high temperature of the discharge tubes and the infrared (IR) radiation characteristics such lamps find limited use in the processing of temperature sensitive materials, e. g. the curing of paints on plastics. Solid state light sources based on UV-LED however offer a solution for the abandonment of toxic mercury lamps, while providing additional benefits as smaller form factor, increased lifetime and ruggedness, an application tailored emission spectrum with reduced IR emission and added flexibility to UV applications [1], [2]. High power density UV-LED modules are currently under scientific investigation and commercial systems are entering the market. An Al_2O_3 based assembly using 98 densely packed LED chips is shown in [3]. Ceramic materials, such as alumina, aluminum nitride and even low temperature co-fired ceramics (LTCC) can be used in high power packaging due to their high thermal conductivity [4]. Especially applications like water and air disinfection need high power sources in the UVC range (280 nm to 100 nm) [5]. The development of solid state deep UV sources aim at the decrease of emitted wavelength and the improvement of output power and external quantum efficiency [6], [7]. Highly efficient light sources promise to deliver a significant contribution to a global sustainable development.

As efficient cooling is important for the increase of extractable optical power and a minimized thermally induced wavelength shift, thin layer bonding techniques as well as reduced chip-die substrate thickness gain relevance [8]. Soldering processes can provide thin metallic bond layers with good thermal conductivity and high mechanical strength. Gold-tin solder alloys are used in opto-electronic packaging, die-attach and for the assembly of micro-optical systems [9], [10]. High temperature tin-based solder alloys with a high lead content and lead-free drop-in replacements such as Bi-Ag are proposed for the assembly of power circuits [11]. Another die-attach technology is the use of micro and nano-scale silver sinter materials to provide high strength joints with outstanding electrical and thermal conductivity. Silver-sintering die-attach provides interconnects of semiconductor devices that are operable at high temperatures up to 350 °C [12]. The reduction of bond pressure down to 2 MPa and temperatures down to 200 °C, necessary for the processing of sensitive opto-electronic components, is reported [13]. Thermo compression provides a simple yet high temperature process for bonding of components. Thin and therefore thermally high conductive bond layers are feasible [14]. A new approach of Die-attach is reactive multilayer bonding using nano-scaled alternating layers of two materials. Foils or deposited films of nano-engineered materials generate heat by a self-propagating exothermic reaction allowing for a localized reflow of solder. Small and temperature-sensitive components can be joined without thermal or thermo-mechanical damage [15]. The high processing temperatures also allow for welding and thus produce high shear strength joints [16]. Another state-of-the-art bonding technology for die-attach is using silver-filled epoxy resins with the filler particles providing thermal conduction while the epoxy is generating adhesion bonding [17]. Current developments include nano-scaled filler materials to enhance the thermal conductivity of adhesives for packaging of high brightness LED [18]. Die-attach technologies for high temperature applications are an issue beyond solid state lighting. A review on materials for device interconnection technologies for high power electronics is given in [19].

The system presented utilizes a chip-on-board design to provide a multi-chip module package of high power UV-LED on ceramic substrates. LED chips in the UVA range (400 nm to 300 nm) are mounted on stackable aluminum nitride and alumina substrates. Goal of the project is the increase of optical output power by efficient cooling. The scalable design using sub-modules is of advantage to a flexible and customer specific use. Die-attach is conducted using eutectic gold-tin solder in a flux-free processing, tin-lead solder and two silver-loaded adhesives. The thermal behavior is compared by measurement of optical power and wavelength drift. Mechanical strength and microstructure are analyzed by shear force measurements, cross-sectioning and micro-tomography.

Design

Based on the targeted areas of application a design for a stackable multi-chip module is developed. This approach allows for the scalable assembly of line sources with different lengths as well as for the use of single modules for lighting systems. The suggested design offers flexible use in various applications. An array of 7×2 LED-chips per sub-module is designed to provide a line shaped light source for homogenous illumination of a larger two-dimensional surface without complex beam shaping optics. Addressed applications are the curing and polymerization of adhesives, inks, paints and coatings in continuous processes. An alternate design of 3×2 LED-chips per sub-module is proposed for the use as an UV light source for the homogeneous illumination of a digital mirror device (DMD). Such devices find applications in the exposure of offset plates for offset printing. DMD are capable of a fast and cost efficient manufacturing of offset plates in Computer-to-plate (CTP) or Computer-to-conventional-plate (CTCP) processes [20]. These techniques lead to reduced repress time and improved print quality.

A ceramic substrate (either alumina or aluminum nitride) is used as a mechanical system carrier, to provide electrical contact and allow for proper thermal management and cooling of the LED-chips. Substrate dimensions are 12×10 mm², with a thickness of 1 mm for aluminum nitride and 0.38 mm for alumina. The electrical wiring and solder pads are manufactured directly onto the surface of the substrates. The wiring structures are manufactured of W/Ni/Pd/Au layers. Solder land pads with dimensions of 1100×1100 µm² with a spacing of 300 µm are structured on the substrate surfaces (Figure 1). The pads are made of sputtered eutectic gold-tin for soldering with gold-tin solder alloy or thin film gold for the use of adhesives and soldering with a tin-lead solder alloy [10].

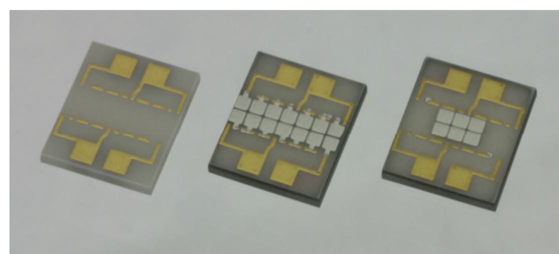

Figure 1: Aluminum nitride substrates with electrical wiring and structured eutectic gold-tin solder layers in two design variants (7×2 LED-chips and 3×2 LED-chips).

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UVA emitting indium-gallium-aluminum-nitride LED-chips SL-V-U40AC by Semiled Inc. with a center wavelength of 395 nm, a chip size of 1070×1070 µm² and a rated typical optical output power of 210 mW to 250 mW are used. The initial design was based on NS375C-3SAA LED-chips by Nitride Semiconductor Co., Ltd. with a chip size of 600×600 µm² but was changed to the former due to considerations of wavelength, optical output power and availability. The Semiled chips are available with a back metal gold layer usable for soldering and adhesive bonding.

Electrical contacting of the front contact is conducted by ultrasonic assisted wedge-wedge wire bonding of Au and AlSi wires. Back-side contacts are connected by the solder or the conductive adhesive to the wiring structures on the substrate. Submodules are mounted to a scalable and liquid-cooled heat-sink by means of indium foil. The use of indium allows for a proper thermal contact and excellent cooling due to its high ductility and its high thermal conductivity of 82 W/(m·K).

Thermo-mechanical and thermal simulations

Based on the design data and the NS375C-3SAA LED-chips thermal and thermo-mechanical analyses are conducted by finite elements simulations (FE). Thermo-mechanical analysis is used to evaluate the stresses to substrate, LED-chips and joining material due to different coefficients of thermal expansion. Thermal analysis provides insight in the capability of the design and material selection on efficient heat removal from the chips. FE analysis is computed using ANSYS 11.0 SP1.

Targeted design goals are 80 mW optical output power and 100 mW respectively. The LED-chips achieve 80 mW optical at 200 mA, 4.5 V and about 9.5% efficiency resulting in a thermal load of 840 mW. 100 mW optical are attained at 350 mA, 5 V with less than 6% efficiency and a resulting thermal load of 1650 mW. A ¼-model with symmetric boundary conditions is used for simulation. Base temperature of the substrate is set to 0°C and a natural convection with 10 W/(m²·K) is applied to all outer surfaces. Table 1 shows relevant material properties used for the simulations. Additionally temperature dependency for Young's modulus, Poisson's ratio and plasticity of the gold-tin solder are modeled.

Modeling soldering using eutectic AuSn with a solder layer of 10 µm is done. Solidification of the solder alloy from solidus to room temperature leads to a shrinking of about 5%. Resulting mechanical stresses within the solder layer are near the yield strength of the material indicating plastic deformation of the solder. Maximum values of 320 MPa for AlN and 337 MPa for Al_2O_3 are calculated. Stresses within the base materials are computed to be 93 MPa for AlN and 95 MPa for Al_2O_3 which is significantly below the ultimate tensile stresses for those materials.

Table 1: Material properties for simulation model (sources: [21], [22], [23] and respective data sheets, (1) ⊥ C-axis).

Property	λ	TCE	E	ρ
Unit	W/K·m	ppm/K	GPa	g/m³
Al_2O_3	24	6.8	340	4.0
AlN	180	4.7	320	3.3
Sapphire	40	5.4(1)	430	4.0
Au80Sn20	58	16	59	14.7
Adhesive	17	30	1.21	3.2

Thermal analysis is conducted to provide results of temperature distribution and heat flux within the sub-assemblies. For the design goal of 100 mW optical output power per chip and a thermal load of 1.65 W chip temperatures are calculated to be 23 K above substrate temperature for AlN and 40 K for Al_2O_3 using 10 µm AuSn solder layers (Figure 2 and Figure 3).

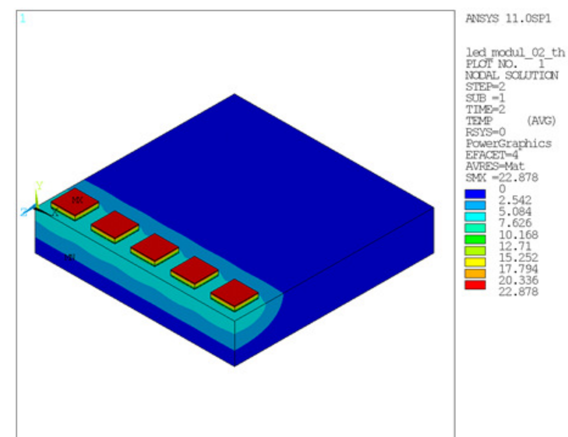

Figure 2: Temperature distribution within LED-chips and AlN substrate (thickness 1 mm) for eutectic AuSn solder (layer thickness 10 µm) and 1.65 W thermal load.

Calculations are repeated with respect to a conductive silver-loaded thermoplastic/thermoset adhesive with a thermal conductivity of 17 W/(m·K). Assumed thicknesses of the adhesive layers are 10 µm and 30 µm respectively. Substrate material is Al_2O_3 with a thickness of 0.38 mm. Thermo-mechanical strain is mainly influenced by the base material and not the adhesive. Equivalent stresses are 43 MPa for both adhesive layer thicknesses.

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Stresses are significantly lower than for the solder attach and thus below the ultimate tensile stresses of the substrate materials. Due to lower Young's modulus of the adhesive – 1.2 GPa compared to 68 GPa for AuSn – the inherent stresses within the adhesive layers are significantly lower than within the solder. The results show equivalent stresses within the adhesive of 3.1 MPa for 10 µm layers and 2.6 MPa for 30 µm layers, respectively.

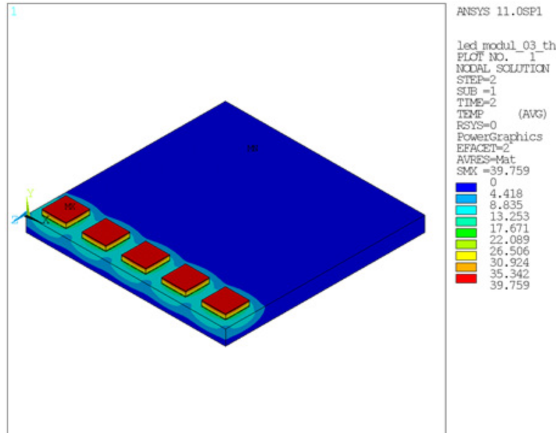

Figure 3: Temperature distribution within LED-chips and Al_2O_3 substrate (thickness 0.38 mm) for eutectic AuSn solder (layer thickness 10 µm) and 1.65 W thermal load.

Thermal analysis for a thermal load of 1.65 W per chip results in chip temperatures of 42 K above substrate temperature for 10 µm layers and 47 K for 30 µm layers (see Figure 4 and Figure 5). These calculations indicate that a proper cooling of the chips could be achieved using thermally conductive adhesives. Thicker adhesive layers increase chip temperature significantly. In the case of thin bonding layers – either solder alloy or adhesive – thermal properties are mainly influenced by the chips and the substrate itself.

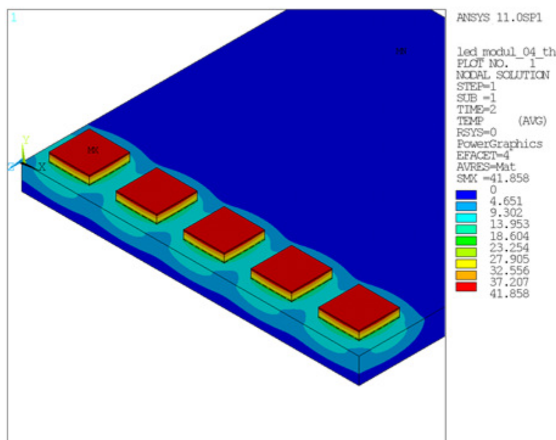

Figure 4: Temperature distribution within LED-chips and Al_2O_3 substrate (thickness 0.38 mm) for silver-filled adhesive (layer thickness 10 µm) and 1.65 W thermal load.

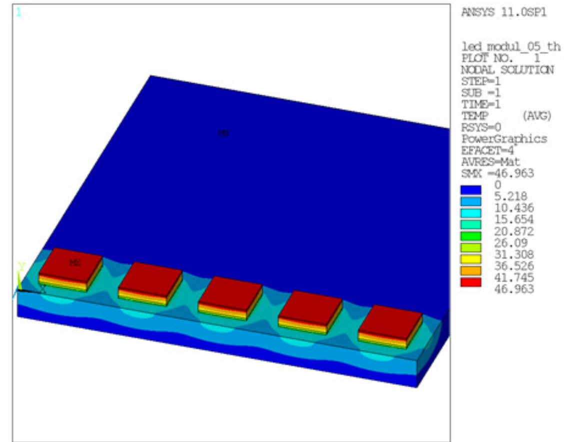

Figure 5: Temperature distribution within LED-chips and Al_2O_3 substrate (thickness 0.38 mm) for silver-filled adhesive (layer thickness 30 µm) and 1.65 W thermal load.

The results of the FE calculations show acceptable thermo-mechanical stresses for both substrate materials and soldering with eutectic gold-tin. The thermal matching of sapphire based LED-chips and the used substrate materials AlN and Al_2O_3 keep the tensile stresses below ultimate yield strength. Thermal results show proper extraction of heat during operation. The high thermal conductivity of AlN of 180 W/(m·K) leads to a lower chip temperature during operation compared to Al_2O_3. Silver-filled adhesives provide similar performance if thin layers could be successfully processed. The results allow the comparison of different die-attach technologies and can be transferred to other chip types.

Experimental – Die Attach

Three different Die-attach technologies are comparatively used: 1) eutectic gold-tin solder and flip-chip-assembly, 2) standard vacuum reflow of a flux enhanced SnPb solder (Figure 6), and 3) two different silver-loaded adhesives. Flip-Chip assembly is conducted using a ficonTEC Flip-Chip-Bonder BL-2000 and a Finetech Fineplacer Lambda, respectively. Reflow during flip-chip-placement is established by using a heated pick-up tool (PUT) and a hotplate with a substrate holder. The use of a substrate hotplate allows a stand-by temperature below solder alloy reflow and the subsequent placement and soldering of single chips by the PUT. LED-chips with a manufacturer-made gold metallization are used for SnPb soldering and adhesive attach. Sputtered eutectic gold-tin is used for additional metallization of LED-chips for flip-chip-attach [10]. An optional increase of solder layer thickness is conducted by application of additional solder volume by means of Solderjet Bumping [24].

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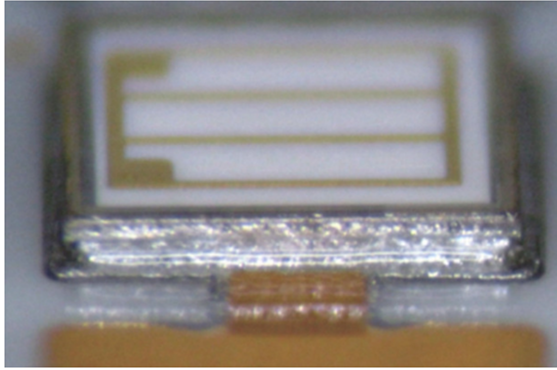

Figure 6: LED-chip soldered to an Al_2O_3 substrate.

Relevant process parameters are temperature profile and reflow regime as well as bonding force (applied pressure during placement and reflow). More than 30 assemblies using testing elements are manufactured for mechanical testing and process optimization. Soldering of chips using less than 10 µm sputtered AuSn layers (as-sputtered, without additional solder applied) did not prove to be reliable joined. Low shear forces and unregular wetting are observed. An additional Ø300 µm solder sphere is applied to provide for an additional solder layer thickness of 12 µm. Fully operational 7×2-chip samples are made for optical testing (Figure 7).

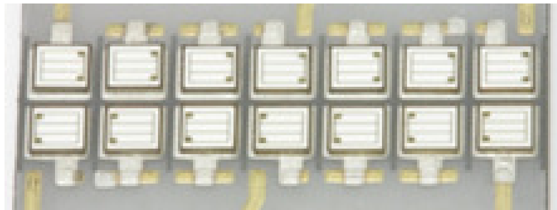

Figure 7: Fully assembled 7×2 UV-LED module.

The third die-attach technology used is adhesive bonding with silver-loaded and thermally conductive adhesives. Although being a well established and commercially used technology the application of highly filled adhesives requires major adaptations of dispense and chip placement technologies. The optimization of the process flow, curing conditions and homogenization of the adhesive is necessary to achieve reproducible thin joint fissures.

Experimental – Analysis of Solder Joints

Mechanical testing of soldered components, both LED-chips and testing vehicles is conducted using shear force measurements. Using components with an additional solder volume, 6 N to 18 N with glass testing elements for variation of process parameters are achieved. LED-chips show a shear force greater than 10 N with the main failure mode being the rupture of chips rather than failure of solder joints or layer interfaces. Cross section views (Figure 8) show a homogenous filling and a solder layer thickness below 30 µm.

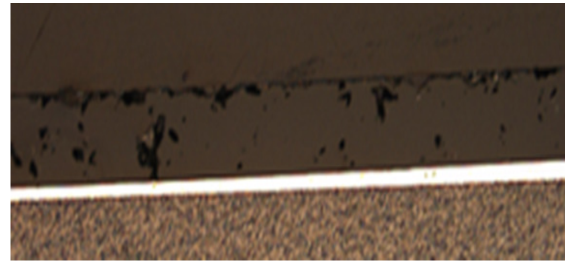

Figure 8: Cross section view of a AuSn soldered LED-chip.

Micro-Computer-Tomography (Micro-CT) analysis confirms a void free and homogenous solder layer for AuSn soldering (Figure 9). In comparison the micro-CT shows significant voiding for the vacuum soldered LED-chips (Figure 10). The increase of thermal resistance of solder joints with a higher fraction of voids is obvious. Flux-free processing of gold-tin solder furthermore eliminates the need for additional cleaning after soldering.

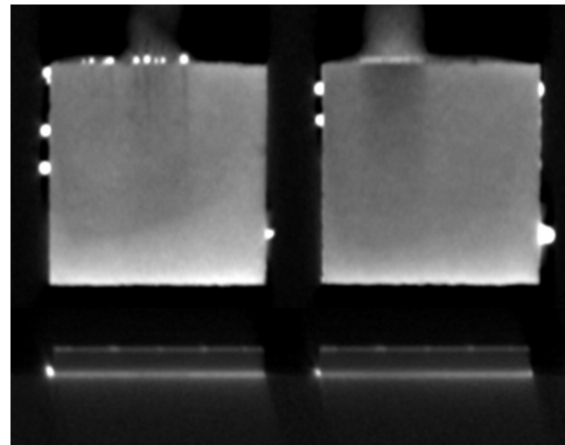

Figure 9: Micro-CT of AuSn soldered LED-chips.

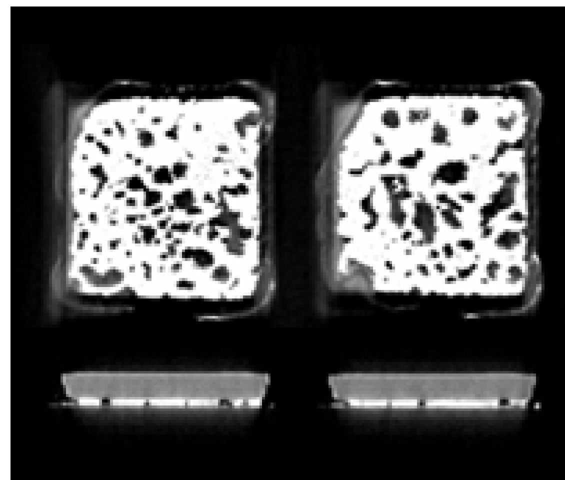

Figure 10: Micro-CT of SnPb soldered LED-chips.

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Optical Measurements

Optical power measurements and wavelength shift are observed using an integrating sphere. A setup of an Ulbricht sphere that allows for the mounting of the proposed ceramics substrate attached to a heat sink is constructed. This structure permits the operation of the LED-chips at high power ratings while diffusing the light for an integrating measurement of total power without concerns about the directional characteristics of the LED assembly. The design of the heat-sink and the substrate clamping lead to approx. 30% NA-loss during measurements. A calibration of the Ulbricht sphere with respect to this fact is used to correct the results.

The results of optical output power of the four die-attach variants – adhesive 1, adhesive 2, SnPb solder, and AuSn solder – are shown in Figure 11. Measurement has been conducted using one channel of 1×7 chips per substrate and for operational currents of 350 mA, 700 mA and 1050 mA. A significant improvement of output power is observed for AuSn die-attach. Adhesive 2 shows a decrease of output power with increased current.

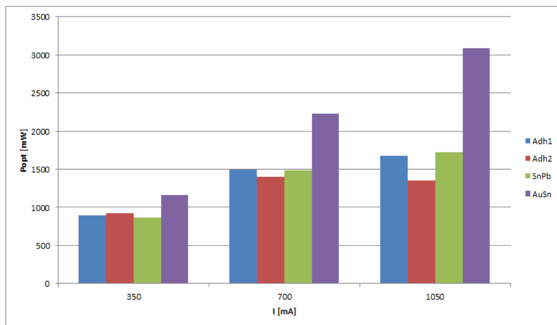

Figure 11: Optical output power of one channel (1×7 chips) for four die-attach variants.

Using both channels of 2×7 chips an optical output power of 7.7 W is achieved at 1050 mA for AuSn soldered assemblies. The resulting peak irradiance is 30.8 W/cm² at the LED surface with respect to the footprint and pitch of the attached chips. The optimized cooling of AuSn-soldered LED-chips is demonstrated by the increased optical output power compared to adhesively joined LEDs (Figure 12).

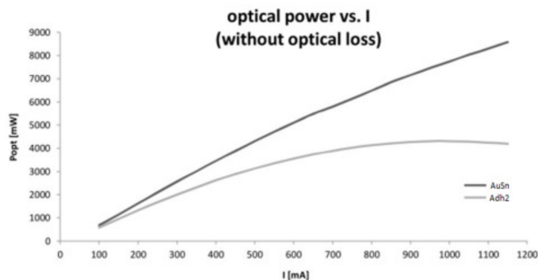

Figure 12: Optical output power of both channels (2×7 chips) for the gold-tin solder (AuSn) and adhesive (Adh2) die-attach.

Additionally the thermally induced shift of emission wavelength can be used to compare different die-attach technologies with respect to thermal transfer capabilities. Better cooling corresponds to a lower chip temperature and thus to a lower wavelength shift. Both soldering techniques show improved behavior compared to the adhesives (Figure 13). Gold-tin solder layers show a lower drift than the void-prone SnPb solder.

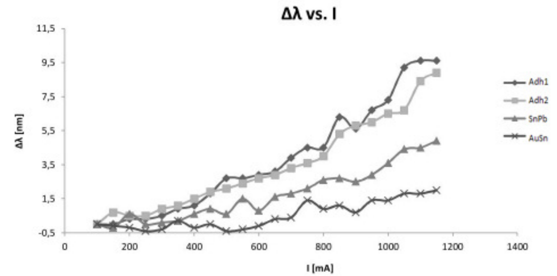

Figure 13: Wavelength shift over current for four die-attach variants.

Summary and Outlook

The assembly of a UV-LED multi-chip module using different die-attach technologies has been demonstrated. Finite element analysis proves acceptable thermo-mechanical stresses and the realization of thermally high conductive joints using solder alloys and new highly conductive silver-loaded adhesives if thin layers could be processed.

The design of a multi-chip sub-module is flexible and versatile to use. Line-shaped light sources are possible by stackable modules. A six-module assembly is demonstrated. Easy scaling of optical output power as well as a simplified servicing by changing single modules add to the customer benefit. Measurements of optical output power and low thermally induced wavelength drift as well as analysis of solder layer structure show the performance of thin gold-tin solder layers. A 14 chip module attains 7.7 W optical output power and a respective peak irradiance of 30.8 W/cm². Long term behavior and the investigation of reliability over life time are the next steps to confirm the usability of the proposed module design and die-attach technologies.

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