Modeling of the Punch-Through Effect in Normally-On SiC JFET used in High Temperature Inverter for Aerospace Application

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Abstract

This paper presents a qualitative description of the punch-through mechanism in Silicon Carbide (SiC) JFET from Infineon/SiCED. A detailed one-dimensional analytical expression is derived for the current-voltage characteristic of the punch-through effect in the SiC JFET. The proposed model based on physical parameters is validated with experimental results for low current level.

Keywords: SiC JFET, Punch-through, Gate Driver and Aerospace

1 Introduction

Integration of power converters (i.e. voltage source inverter) in actuator housing is a new trend in the aerospace industry. Thus complexity and mass of the aircraft has to be reduced [1]. Such converters are located in harsh environment with ambient temperature reaching 225 °C. Moreover, to reduce cable size the HVDC (High Voltage Direct Current) level will be increased to 540 V in future aircrafts [2]. Therefore, the next generation of aerospace converter should be designed to sustain temperature up to 225 °C and be able to switch voltage up to 540 V.

Wide BandGap (WBG) semiconductors such as Silicon Carbide (SiC) have demonstrated the possibility to develop highly compact and integrated power converter working at junction temperature above 250 °C [3-5]. SiC devices such as diode, enhancement mode JFET (normally-off), depletion mode JFET (normally-on), MOSFET and BJT are commercially available. However, at the time of writing, the depletion mode JFET is the most mature three terminals SiC device for high voltage and high temperature application. At Ampere Laboratory and Hispano-Suiza (SAFRAN Group), the depletion mode SiC JFET from Infineon/SiCED has been selected to demonstrate the first generation of high temperature converters [6-7].

To predict the system behavior (design of EMI filters, assessment of the junction temperature or switching losses), it is necessary to model the switching device.

Several papers are dealing with the modeling of SiC JFET components [8-9] but none of them integrate the behavior of the gate-to-source junction during the punch-through effect. Is this phenomenon not meaningful? Let's look at the raison that motivates the modeling of the punch-through effect.

First of all, punch-through happens when the two below conditions are met,

- Depletion region around the gate meets the depletion region around the source;
- A high reverse voltage, greater than the punch-through voltage, is applied between the gate terminal and the source terminal.

When a punch-through is triggered, excessive holes cross the gate-to-source potential barrier, and punch-through current flows through the gate terminal. Punch through arises in Infineon/SiCED depletion mode SiC JFET because of the two P^+ gates structure as depicted in figure 1.

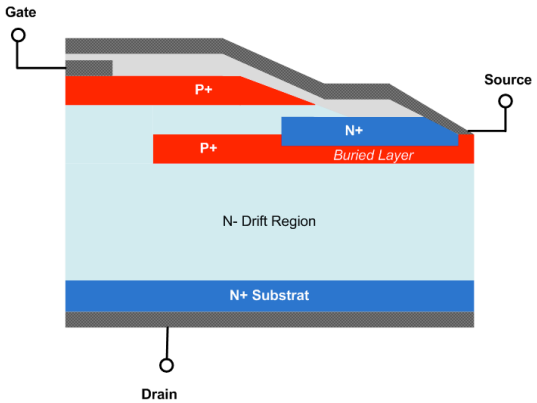

Figure 1: Cross-section of SiC JVET from Infineon/SiCED

One other important characteristic of the punch through is the increase of the threshold voltage with temperature. As the pinch-off threshold decreases with temperature, the blocking voltage margin also decreases with temperature.

Figure 2 represents the variation of the pinch-off voltage (i.e. measured at a drain-to-source current of 10 µA) and the punch-through voltage (i.e. measured at a source-to-gate current of 200 µA) with temperature. It can be seen that the blocking voltage margin is equal to 9 V at 25 °C and decreases to 4.7 V at 225 °C.

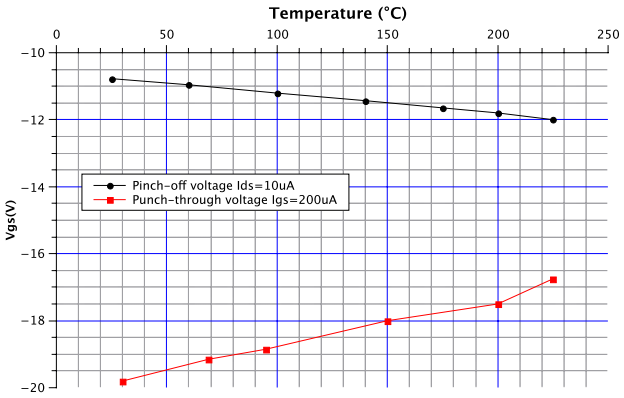

Figure 2: Variation of the punch-through voltage and the pinch-off voltage from 25 °C to 225 °C of 1.2 kV 60 A (3.2 x3.2 mm^2) SiC JFET from Infineon/SiCED

In [10], it is reported that punch-through is initiated during high dv/dt switching due to the Miller capacitance of the JFET. At high temperature with lower blocking voltage margin, this will become more critical.
A second aspect is the use of the punch-through effect as a Transient Voltage Suppression (TVS) diode (low leakage current and capacitance). Indeed, as we will see in the third section, the reverse characteristic of the JFET exhibits a sharp knee at voltage below the punch-through voltage.
Thus, it is necessary to determine the punch-through current-voltage characteristic.
To provide the reader a clear understanding of the punch-through mechanism, the first section is dedicated to a qualitative and graphical explanation of this physical effect. The equations used to derive the punch-through model are presented. The variation of the barrier height with the gate-to-source voltage is also described. In a second part is proposed a one-dimensional model of the punch-through current versus the gate-to-source voltage. In a third section is provided experimental results that validate the punch-through model.

2 Punch-Through Analysis

The punch-through effect is a well-known phenomenon that was studied in bipolar transistors forty years ago [11-12] and used later to develop protection devices against voltage spike (lightning strike, inductive load, ESD) [13-14] or microwave mixers and detector diodes.
The punch-through arises in short-channel P^+NP^+ or N^+PN^+ sandwich structure (i.e. before avalanche breakdown). As explained in the introduction and displayed in figure 1, the Infineon structure presents a P^+NP^+ sandwich structure between the gate and source. The structure consists of two highly homogeneously doped P^+-type regions N_{ag} and N_{as} between a homogeneously doped N region N_d. One of the P^+-type region is connected to the gate terminal and the second buried P^+-type region is connected to the source terminal. The P^+NP^+ sandwich structure is depicted in figure 3. The width of the lateral (N-type) channel is equal to 2a.
To simplify the analysis, the voltage drop in the P^+-type region is assumed to be negligible since the P^+ region is highly doped (abrupt junction). Moreover all quantities are independent of time and depend only on the y axis. Evolution of the electric field and voltage potential in the P^+NP^+ are shown for three different states,

- No applied gate-to-source voltage across the P^+NP^+ sandwich structure: non-biased condition;
- Pinched-off lateral channel. The JFET is turned off;
- Punched-through lateral channel.

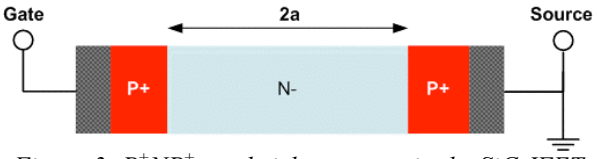

Figure 3: P^+NP^+ sandwich structure in the SiC JFET from Infineon/SiCED

For each state, electric field and the potential relationships across the P^+NP^+ are derived.

2.1 Non-Biased Condition

No electric field is externally applied across the P^+NP^+ structure. Both PN junctions are reverse biased. The electric field and potential in the P^+NP^+ structure with a gate-to-source voltage of zero volts are represented in figure 4. W_1 and W_2 represent the depletion width in the P^+N junction and in the NP^+ junction respectively. U_b represents the barrier height of the P^+NP^+ structure.

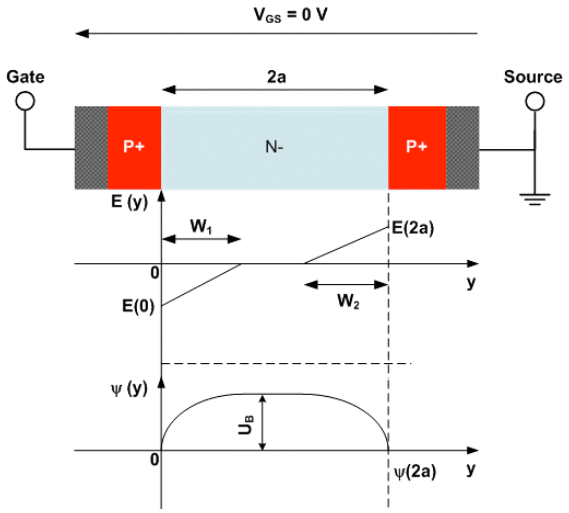

Figure 4: Variation of the electric field and the potential across the P^+NP^+ structure with a non-bias condition

From the Poisson equation, the electric field is given by,

$$\nabla E = \frac{\rho}{\varepsilon} \quad (1)$$

With ρ the charge density in Coulomb and $\varepsilon = \varepsilon_0\varepsilon_r$ the permittivity of SiC (e.g. 88.5 pF/m)
The potential ψ is defined by,

$$\nabla\psi = -E \quad (2)$$

To simplify the analysis, a one-dimensional variation is assumed (uniform distribution),

$$\frac{dE(y)}{dy} = -\frac{d^2\psi(y)}{dy^2} = \frac{\rho}{\varepsilon} \quad (3)$$

For y > 0, the charge density ρ is equal to $-qN_D$ (donors: electron) Thus, we can write,

$$\frac{dE(y)}{dy} = -\frac{q \cdot Nd}{\varepsilon} \quad (4)$$

Equation (4) is integrated with $E(W_1) = 0$. The electric field E for $W_1 > y > 0$ is given by,

$$E(y) = \frac{q \cdot Nd}{\varepsilon} \cdot (y - W_1) \quad (5)$$

Equation (5) is integrated with $\psi(0) = 0$. The potential ψ for $W_1 > y > 0$ equals,

$$\psi(y) = -\frac{q \cdot Nd}{\varepsilon} \cdot \left(\frac{y^2}{2} - W1 \cdot y \right) \quad (6)$$

Between W_2 and 2a, the electric field E and the potential ψ are given by,

$$E(y) = \frac{q \cdot Nd}{\varepsilon} \cdot (y - (2a - W2)) \quad (7)$$

And,

$$\psi(y) = -\frac{q \cdot Nd}{\varepsilon} \cdot \left(\frac{y^2}{2} - (2a - W_2) \cdot y + \frac{(2a)^2}{2} - 2a \cdot W_2 \right)$$

(8)

Equations of the electric field and potential in a non-biased pn junction have been derived for a P^+NP^+ structure. These Equations are used to determine the barrier height in the P^+NP^+ structure.

2.2 Lateral Channel Pinched-off

The increase of the negative gate-to-source voltage yields the expansion of the P^+N and NP^+ depletion regions (i.e. increase of W_1 and W_2). When the gate-to-source voltage V_{GS} is equal to the pinch off voltage $V_{pinch\text{-}off}$ both depletion regions are in contact (i.e. $W_1 + W_2 = 2a$). The channel is completely depleted, and only positive ionized charges remain in the N region. The current through the channel reaches zero and the JFET is turned-off. The electric field E and potential ψ across the P^+NP^+ sandwich structure are sketched in figure 5. y_0 corresponds to the distance at which the electric field E is equal to 0 V and the potential ψ is maximum and equal to the barrier height U_b.

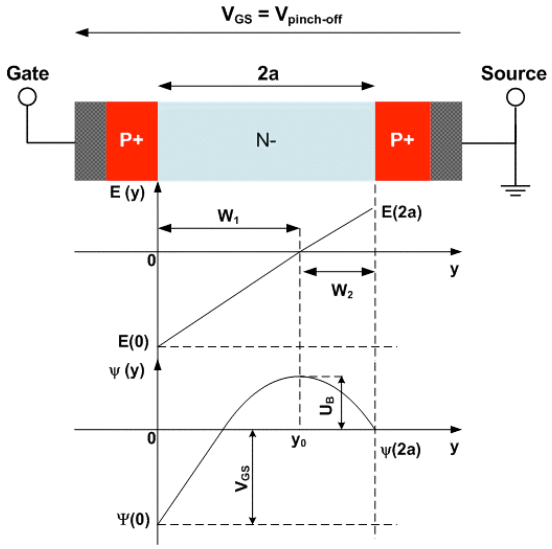

Figure 5: Variation of the electric field and the potential across the P^+NP^+ structure with pinched-off channel

From (5), it can be found that with $E(y_0) = 0$,

$$E(y) = \frac{qN_d}{\varepsilon}(y - y_0) \quad (9)$$

With the reduced quantity $V_p = \frac{qN_d a^2}{2\varepsilon}$ [15], we have,

$$E(y) = 2\frac{V_p}{a^2}(y - y_0) \quad (10)$$

As $E(y) = -\frac{d\psi(y)}{dy}$, integrating (10) with $\psi(y_0) = U_b$, gives,

$$V(y) = U_b - V_p\left(\frac{y - y_0}{a}\right)^2 \quad (11)$$

The gate-to-source voltage V_{gs} is given by,

$$V_{gs} = \psi(0) - \psi(2a) \quad (12)$$

With,

$$\begin{cases} \psi(0) = U_b - V_p\left(\frac{-y_0}{a}\right)^2 \\ \psi(2a) = U_b - V_p\left(\frac{2a - y_0}{a}\right)^2 \end{cases} \quad (13)$$

Using (13), the gate-to-source voltage is transformed to,

$$V_{gs} = 4V_p \frac{(a - y_0)}{a} \tag{14}$$

The barrier height U_b can be obtained using,

$$\psi(2a) = 0 = U_b - V_p\left(\frac{2a - y_0}{a}\right)^2 \tag{15}$$

Thus,

$$U_b = V_p\left(\frac{2a - y_0}{a}\right)^2 \tag{16}$$

With $y_0 = a\left(1 - \frac{V_{gs}}{4 \cdot V_p}\right)$

Substituting (16) in (14), the barrier height U_b is equal to,

$$U_b = V_p\left(1 + \frac{V_{gs}}{4V_p}\right)^2 \tag{17}$$

As expected, the increase of the negative gate-to-source voltage leads to the diminishing of the barrier height.

2.3 Lateral Channel Punched-through

When the negative gate-to-source voltage is increased further, the barrier height U_b is reduced and the junction NP^+ becomes forward biased. A hole current starts to flow in the P^+NP^+ structure. Holes diffuse against the field from the P^+ region connected to the source to the N channel. High electric in the channel attracts hole and drift with the field to the P^+ region connected to the gate.

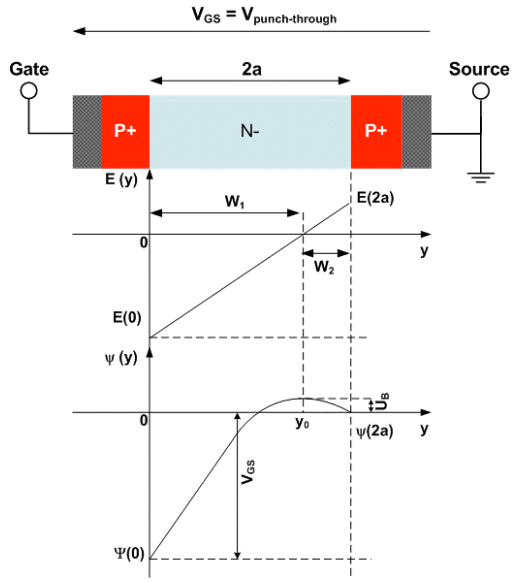

Figure 6: Variation of the electric field and the potential across the P^+NP^+ structure in punch-through

Figure 6 represents the electric field and potential across the P^+NP^+ sandwich structure.
From equation (17), we can notice that when the gate-to-source voltage V_{gs} reaches four times the voltage V_p, the barrier height is equal to zero and the position at which the parabola is maximum correspond to the weight of the channel 2a.

The next chapter provides a one-dimensional current-voltage characteristic of the punch-through effect. Equations presented in this section are used to derive the hole current in the P^+NP^+ structure.

3 Current-Voltage Characteristic of the Punch-Through Effect

As presented in 2.3, the punch-through current raises due to the reduction of the barrier height U_b. In the following, it is assumed that no carrier recombination or carrier generation happens in the N region. Thus, the current density is constant,

$$\frac{dJ_p}{dy} = 0$$

Furthermore, the hole concentration is assumed constant.
The hole current density is obtained using the drift-diffusion relationship,

$$J_P = +q\mu_p p \cdot E - q\mu_p V_T \frac{dp}{dy} \tag{18}$$

With q the elementary charge ($1{,}602*10^{-19}$C), μ_p hole mobility ($m^2.V^{-1}.s^{-1}$), p hole concentration (m^{-3}) and V_T the thermal voltage (k_B*T/q : 25 mV at 25 °C)
The variation of the hole mobility with temperature (Kelvin) (Masetti Model) is given by,

$$\mu_p(T) = 15.9 + \frac{124 \cdot \left(\frac{T}{300}\right)^{-2}}{1 + \left(\frac{N_A}{1.76 \cdot 10^{19}}\right)^{0.34}}$$

The first term in equation (18) corresponds to the drift mechanism and the second term to the diffusion mechanism. If we assume that the hole mobility is constant in the N channel and that the hole velocity does not saturate due to high electric field, we can write,

$$J_P = -q\mu_p p \cdot \frac{d\psi(y)}{dy} - q\mu_p V_T \frac{dp}{dy} \tag{19}$$

By introducing the following equation,

$$\frac{d}{dy}\left(p \cdot e^{\left(\frac{\psi(y)}{V_T}\right)}\right) = \frac{dp}{dy} \cdot e^{\left(\frac{\psi(y)}{V_T}\right)} + \frac{p}{V_T} \cdot e^{\left(\frac{\psi(y)}{V_T}\right)} \frac{d\psi(y)}{dy} \tag{20}$$

Multiplying both sides of (20) by $e^{\left(\frac{\psi(y)}{V_T}\right)}$, we obtain,

$$J_P \cdot e^{\left(\frac{\psi(y)}{V_T}\right)} = -q\mu_p \left(p \cdot \frac{d\psi(y)}{dy} e^{\left(\frac{\psi(y)}{V_T}\right)} + V_T \frac{dp}{dy} e^{\left(\frac{\psi(y)}{V_T}\right)} \right) \quad (21)$$

By identification, we get,

$$J_P \cdot e^{\left(\frac{\psi(y)}{V_T}\right)} = -q\mu_p \left(V_T \frac{d}{dy} \left(p \cdot e^{\left(\frac{\psi(y)}{V_T}\right)} \right) \right) \quad (22)$$

Equation (22) is integrated between 2a > y >0. The one-dimensional hole density current-gate-to-source voltage characteristic equals,

$$J_p = \frac{-q\mu_p V_T N_A \left(1 - e^{\left(\frac{V_{gs}}{V_T}\right)}\right)}{\int_0^{2a} e^{\left(\frac{\psi(y)}{V_T}\right)} dy} \quad (23)$$

Where,

$$\int_0^{2a} e^{\left(\frac{\psi(y)}{V_T}\right)} dy = e^{\frac{U_b}{V_T}} \int_0^{2a} e^{-\frac{V_P \cdot (y-y_0)^2}{V_T \cdot a^2}} dy \quad (24)$$

$\int_0^{2a} \cdot e^{-\frac{V_P (y-y_0)^2}{V_T \cdot a^2}} dy$ represents the integration of a Gaussian distribution function. In order to obtain an analytical expression of the Gaussian function, the error function erf defined by (25) is used.

$$erf(x) = \frac{2}{\sqrt{\pi}} \cdot \int_0^x e^{-t^2} dt \quad (25)$$

With the following relationship proposed in [16],

$$\int e^{-c x^2} dx = \sqrt{\frac{\pi}{4c}} erf(\sqrt{c}\, x) \quad (26)$$

Integration of the equation (22) from y = 0 to y = 2a using (26) with $c = \frac{V_p}{V_t \cdot a^2}$ gives,

$$\int_0^{2a} e^{-\frac{V_P (y-y_0)^2}{V_T \cdot a^2}} dy = \sqrt{\frac{\pi V_t}{4V_p}} \cdot a \cdot \left(erf\left(\sqrt{\frac{V_P}{V_T \cdot a^2}} \cdot (2a - y_0) \right) - erf\left(\sqrt{\frac{V_P}{V_T \cdot a^2}} \cdot -y_0 \right) \right) \quad (27)$$

Using equation (27), the hole current density equation obtained in (22) becomes,

$$J_p = \frac{-q\mu_p V_T N_A}{\sqrt{\frac{\pi}{4}} \cdot L_D \cdot \left(erf\left(\cdot \frac{(2a - y_0)}{\sqrt{2} \cdot L_D} \right) - erf\left(\frac{-y_0}{\sqrt{2} \cdot L_D} \right) \right)} \left(1 - e^{\left(\frac{V_{gs}}{V_T}\right)}\right) \cdot e^{-\frac{U_b}{V_T}} \quad (28)$$

Where L_D is the debye length defined by,

$$L_D = \sqrt{\frac{\varepsilon \cdot k_B \cdot T}{q^2 \cdot N_D}} \quad (29)$$

The above equation can be approximated using the fact that the erf(x) function is equal to 1 for values of x greater than 2 and -1 for x greater than -2. The erf(x) function is represented figure 7. Thus if $\sqrt{\frac{V_P}{V_T \cdot a^2}} \cdot (2a - y_0) > 2$ and $\sqrt{\frac{V_P}{V_T \cdot a^2}} \cdot -y_0 < -2$, the equation (27) is reduced to,

$$\int_0^{2a} \cdot e^{-\frac{V_P (y-y_0)^2}{V_T \cdot a^2}} dy \approx \sqrt{\frac{\pi V_t}{V_p}} \cdot a \quad (30)$$

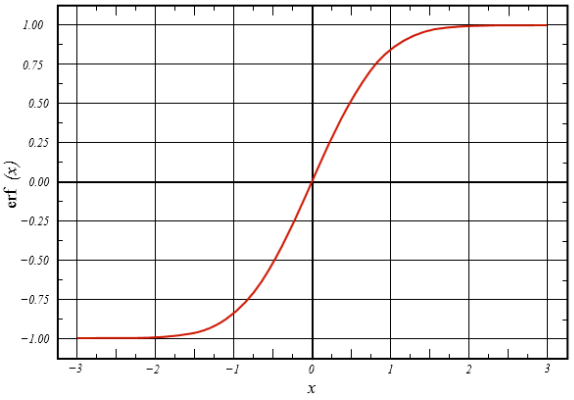

Figure 7 : representation of the erf function between - 3 < x <3

Substitution of (28) into (23) yields an approximate equation of the punch-through current in the P^+NP^+ structure,

$$J_p \approx \frac{-q\mu_p V_T N_A}{\sqrt{\pi}\cdot L_D\cdot} \cdot e^{-\frac{V_p}{V_T}\cdot\left(1+\frac{V_{gs}}{4V_p}\right)^2} \cdot \left(1-e^{\left(\frac{V_{gs}}{V_T}\right)}\right) \qquad (31)$$

The above equation is valid for $y_0 < 2\sqrt{2}\cdot L_D$. The current-voltage characteristic is obtained by multiplying the hole current density J_p by the area of the gate-to-source junction A_{gs} (m). From (31), we can write,

$$I_{gs} \approx \frac{-q\mu_p V_T N_A \cdot A_{gs}}{\sqrt{\pi}\cdot L_D\cdot} \cdot e^{-\frac{V_p}{V_T}\cdot\left(1+\frac{V_{gs}}{4V_p}\right)^2} \cdot \left(1-e^{\left(\frac{V_{gs}}{V_T}\right)}\right) \qquad (32)$$

4 Experimental Results and Discussion

Experimentations have been carried out to validate the proposed model of the punch-through effect. Validation of the proposed model is achieved for low current level (i.e. below 3 mA). The influence of the gate resistance is also demonstrated.

The reverse bias characteristic of the SiC JFET from Infineon/SiCED is plotted in figure 8 for ambient temperatures from 25 °C up to 225 °C.

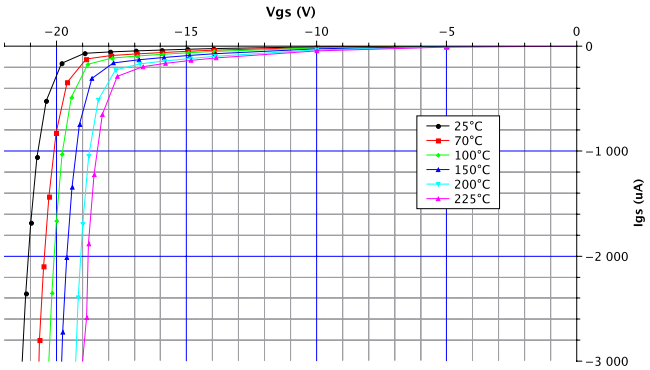

Figure 8: Reverse bias I-V characteristic of the 1.2 kV 60 A SiC JFET from Infineon/SiCED for several temperatures

From figure 8, it can be seen that the punch-through threshold exhibits a positive thermal coefficient of 15.25 mV/°C. We can also see that the junction leaks more at high temperature but the knee is still stiff.

Figure 9 shows the comparison between the analytical one-dimension expression presented in the equation (32) and experimental results at 25 °C. The punch-through hole current is well modeled; slight discrepancy of the punch-through threshold voltage is due to channel width 2a approximation (i.e. obtained from parameters extraction). Furthermore, it can be observed that the leakage current below the punch through voltage in experimentation is higher. This is due to the generation-recombination mechanism that is not taken into account in the proposed model.

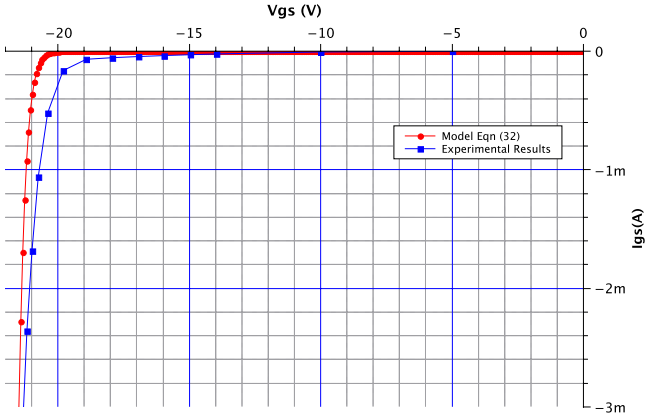

Figure 9: Comparison model (eqn (32)) and experimentation for 1.2 kV 60 A (3.2 x 3.2 mm^2) SiC JFET from Infineon/SiCED at 25 °C

A SABER model of the punch effect has been developed and integrated in the JFET model proposed in [9]. The influence of the internal gate resistance is displayed in figure 11.

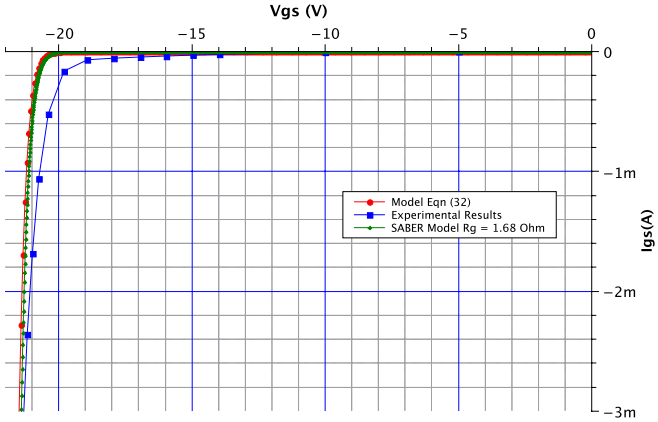

Figure 11: Influence of the internal gate resistance of the JFET

A slight difference of the I-V characteristic with & without the internal gate resistance of the JFET is noticeable. The difference will increase with punch-through current.

At higher punch-through current level (i.e. greater than 1 A), preliminary result shows a higher dynamic resistance, which may be due to space charge limitation current [17-18] and hole velocity saturation [19-20]. The space charge limitation begins when the charge carrier density, hole in our case, becomes greater than the ionized charge density in the N-type region. The space charge limitation opposes further decrease of the barrier height U_b. Moreover for electric field greater than 10^5 V/cm, the carrier mobility depends on the electric field across the P^+NP^+ structure and the velocity is now given by,

$$v_p(E) = \mu_p(E)\cdot E = \frac{{\mu_p}^{LF}\cdot E}{\left(1+\left(\frac{{\mu_p}^{LF}\cdot E}{{v_p}^{SAT}}\right)^{\alpha}\right)^{\frac{1}{\alpha}}} \qquad (33)$$

Where μ_p^{LF} is the low field hole mobility (70 cm^2/Vs), v_p^{sat} the saturation hole velocity ($2x10^7$ cm/s at 25 °C) and α a fitting parameter.

For instance, in the 3.2 x 3.2 mm^2 version of the Infineon/SiCED SiC JFET the electric field is greater than 10^5 V/cm for gate-to-source voltage greater than -20 V.

The high current I-V characteristic is shown in figure 12. At the time writing, the punch-through model is not validated for such high current level.

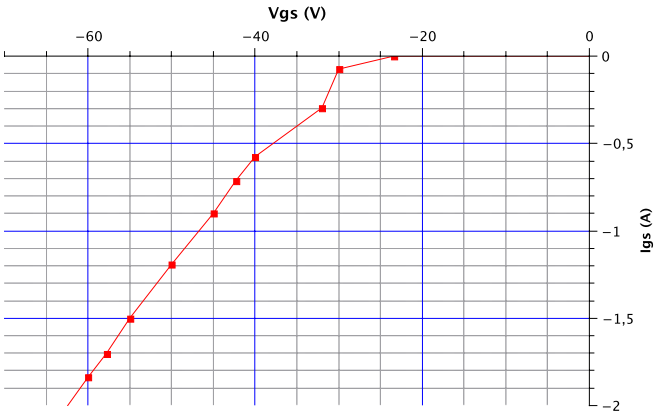

Figure 12: Reverse bias I-V characteristic of the 1.2 kV 20 A SiC JFET (2.4 x 2.4 mm^2) from Infineon/SiCED for punch-through high current at 25 °C

Next version of the punch-through model will take into considerations such factors.

5 Conclusion

The paper presents the punch-through effect in SiC JFET from Infineon. A one-dimensional I-V characteristic model of the punch-through effect is proposed and validated for low current level. High punch-through current level needs to be investigated and in particular the hole current limitation. The next step is to include the temperature dependency of the hole mobility and thermal voltage to predict the variation of the punch-though I-V characteristic with temperature.

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