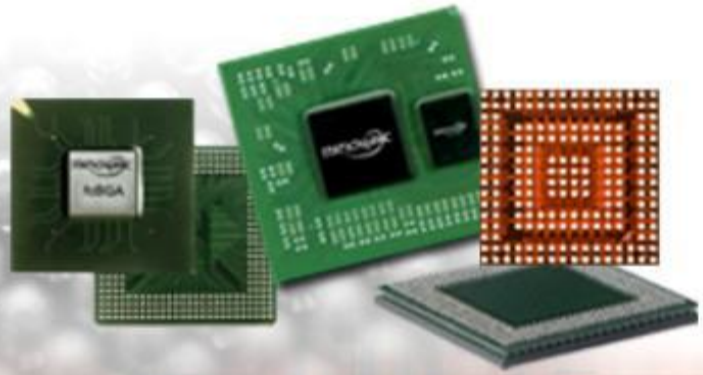
Next Generation eWLB *(embedded Wafer Level BGA)* : Advanced 3D SiP Packaging Solution

S.W. Yoon, Yaojian Lin, **Tom Strothmann** and Marimuthu, ***STATSChipPAC***

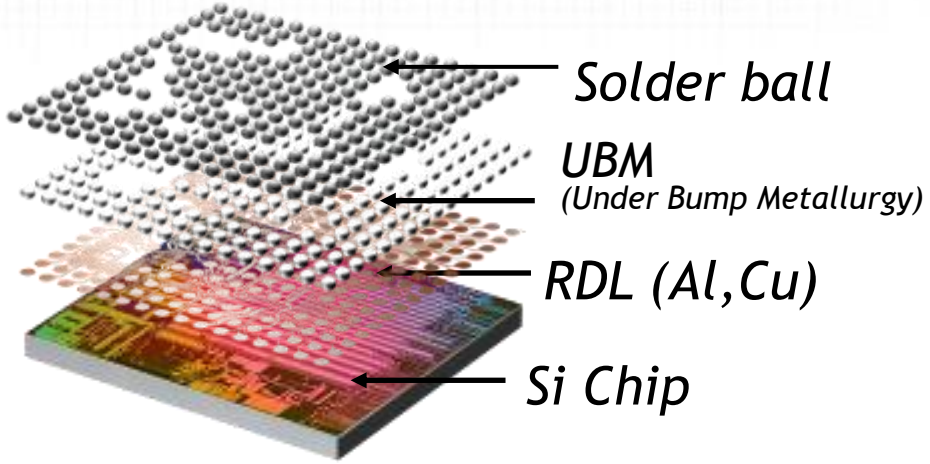
Yonggang Jin, *Jerome Teysseyre, *Xavier Baraton, ***STmicroelectronics***



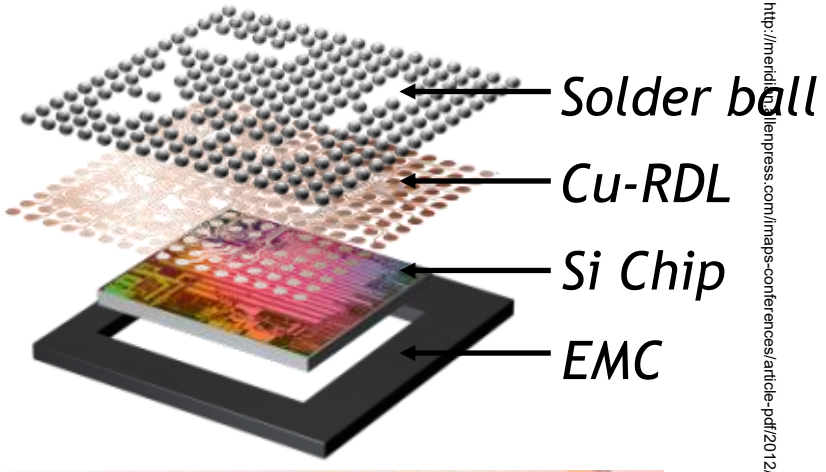
March 2012

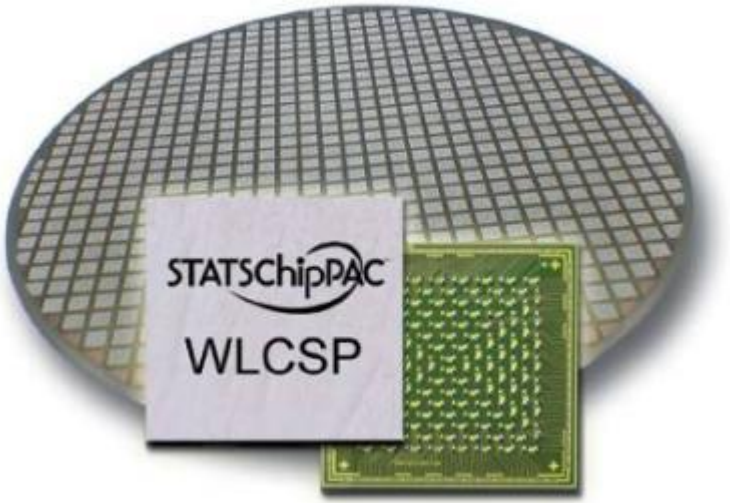
2D Package Structure (Fan-In vs Fan-Out)

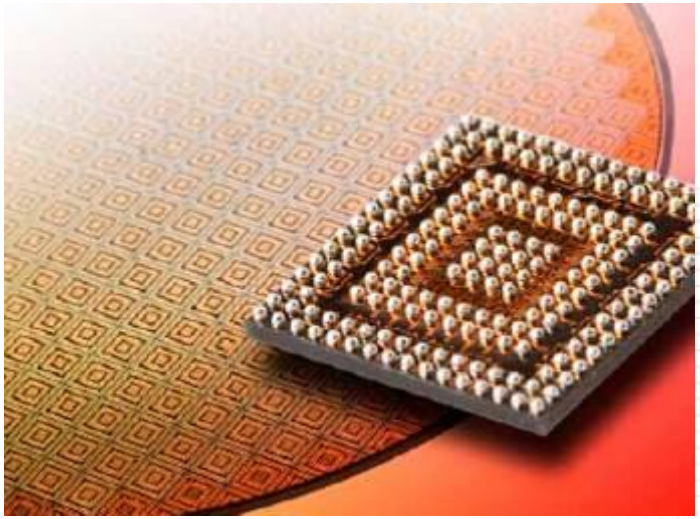
FI-WLP



FO-WLP (eWLB)

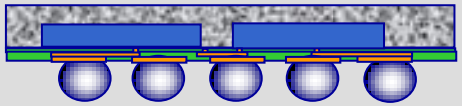




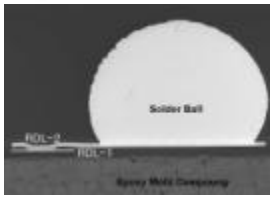


Next Generation eWLB-2011

More than one chip is embedded

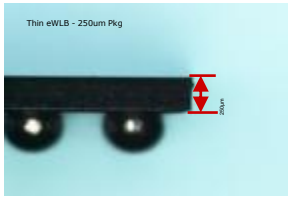


Qualified



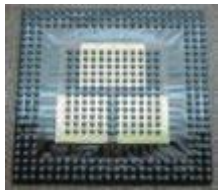
More than one metal layer can be present in both sides

Qualified



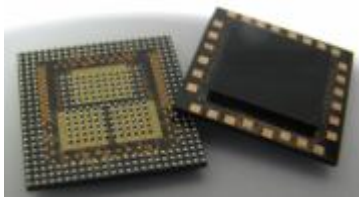
Package thickness is reduced to 0.5mm (body thickness;0.45->0.25mm)

Qualified



Package size is increased to 12x12mm

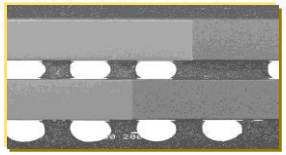
Qualified



Both sides of reconstituted wafer have isolation and metal layers, connected by means of conductive vias in the plastic portion of the wafer

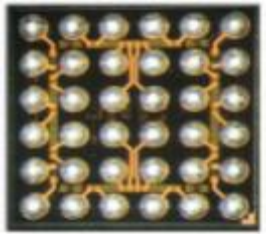
Qualified

Next Generation eWLB-2012



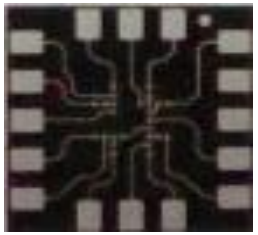
Thin 3D SiP : Both sides of reconstituted wafer have isolation and metal layers, connected by means of conductive vias in the plastic portion of the wafer

Qualified



Small die/package
Die size<1x1mm2

Qualified

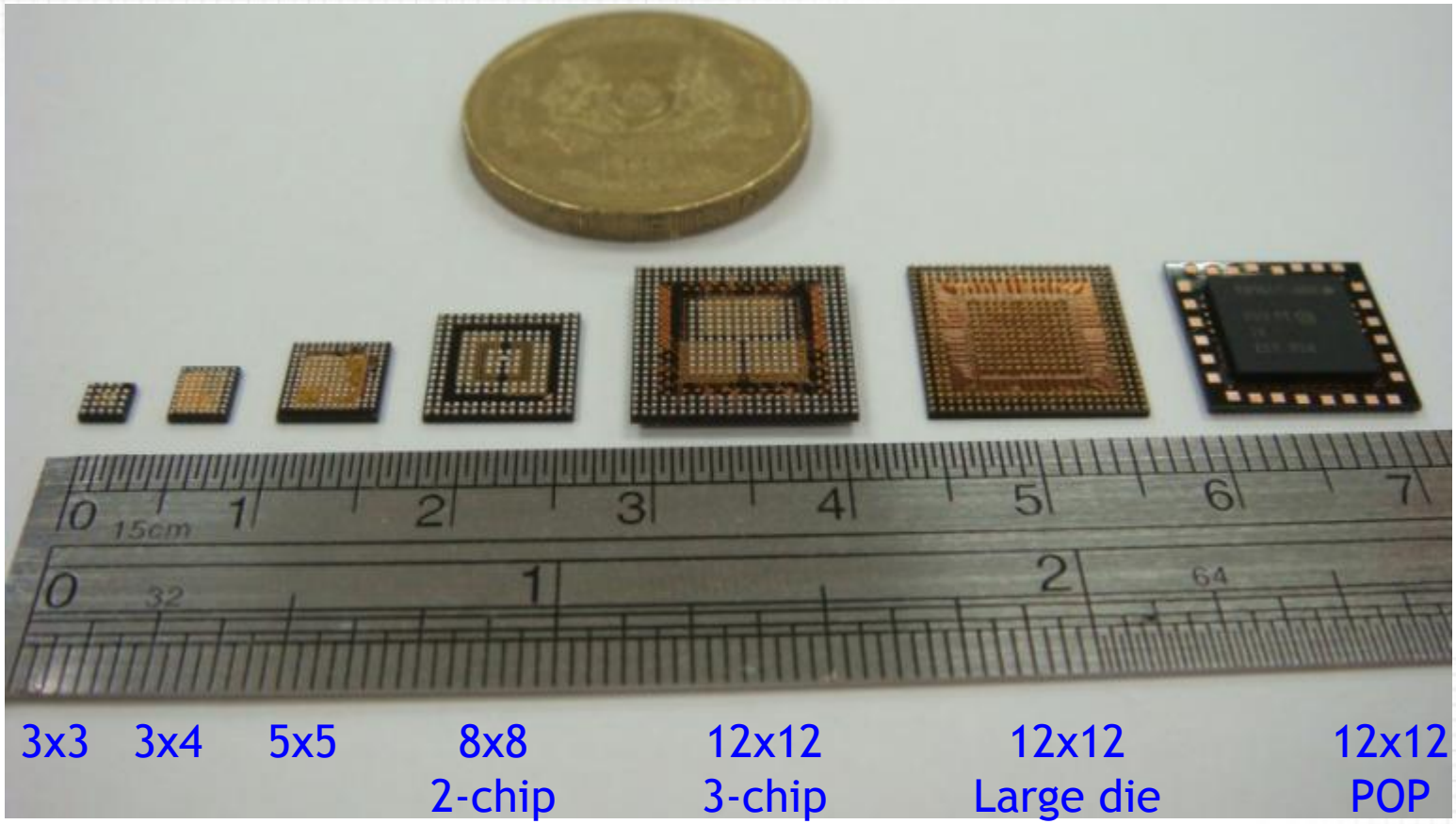


eWLB Land Grid Array

High Power, High Thermal Performance

Qualified

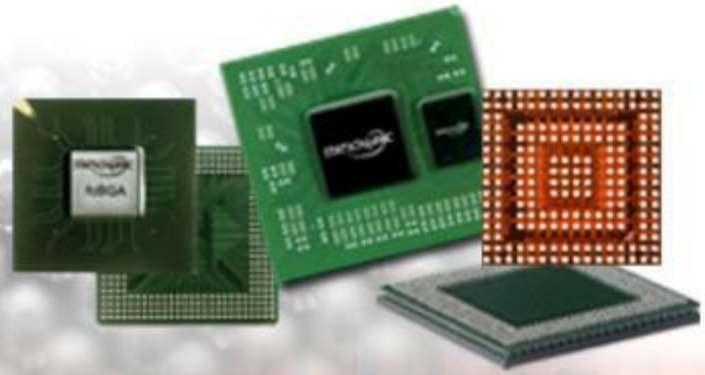
Next Generation eWLB Packages



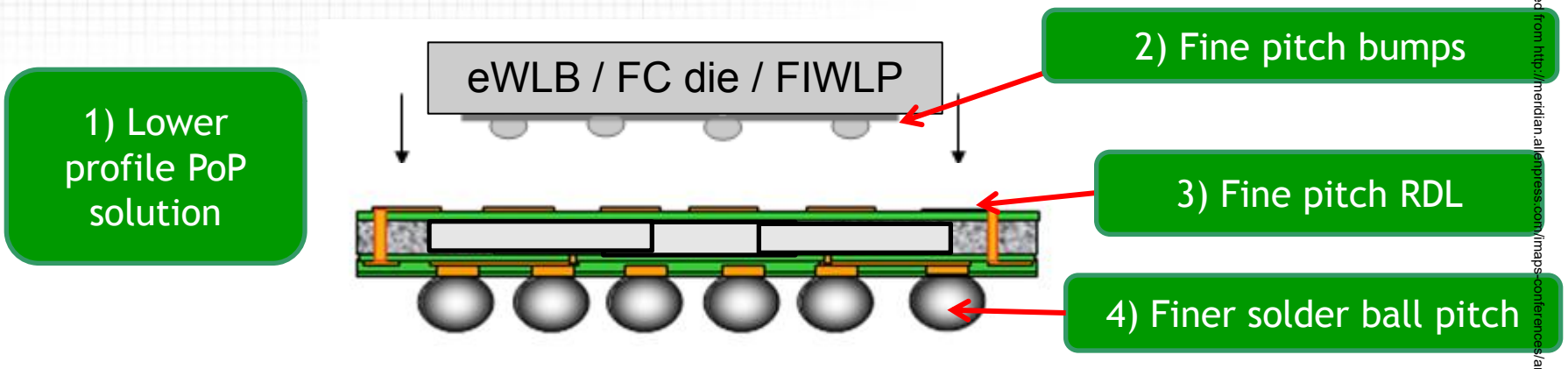
Various types and size of next generation eWLBs

STATSChipPAC

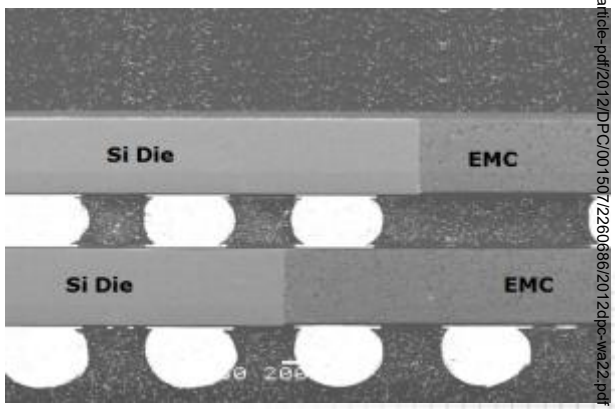
3D SiP eWLB Technology



Double-side eWLB for 3D packaging

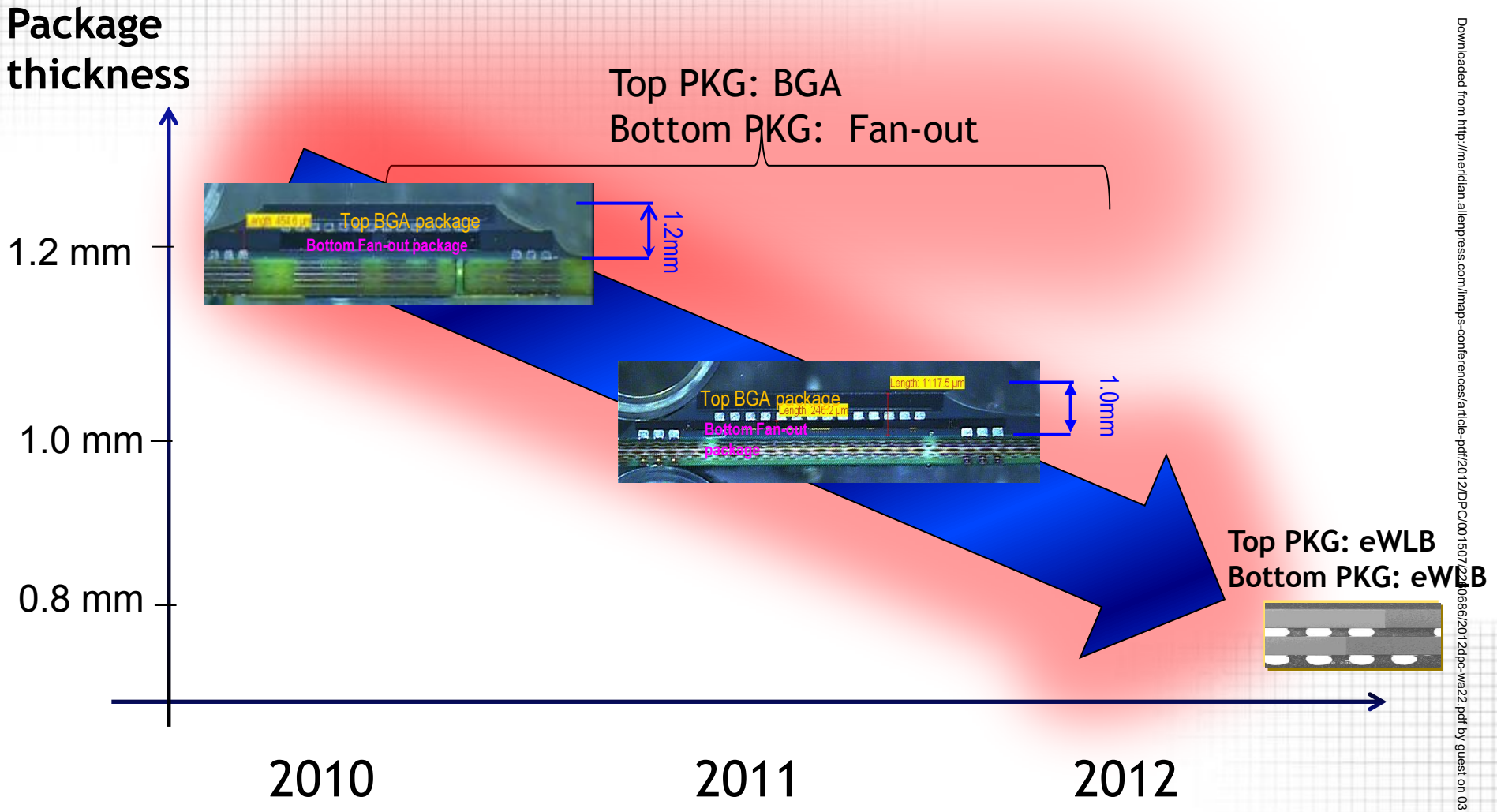


PKG top (bare die, flipchip,eWLB)	0.3-0.5mm
eWLB bottom (thin eWLB)	0.5mm
Total	**0.8 - 1.0mm**



- Lower profile – embedded and thinner
- Higher assembly/SMT yield - smaller warpage
- *Improved flipchip SJR (eWLB CTE is much less than organic substrate)*

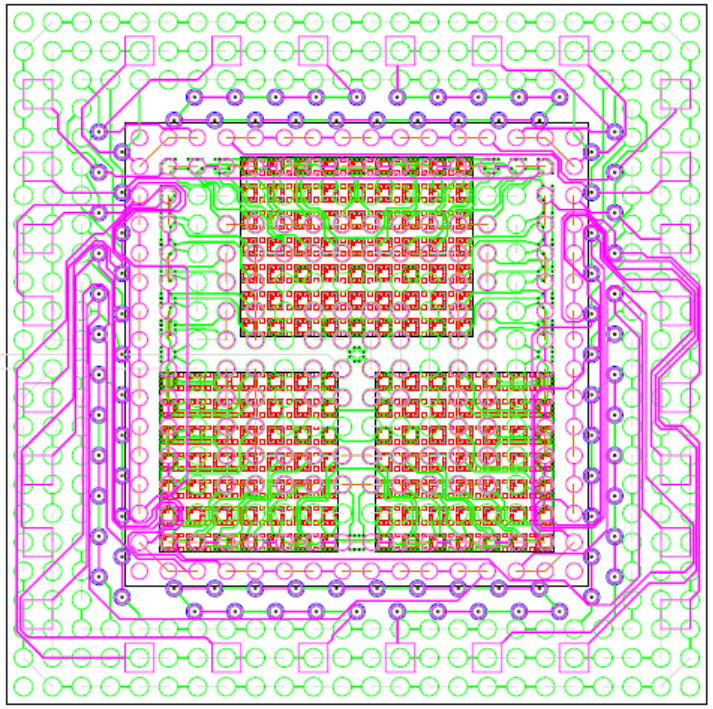
3D SiP eWLB Thickness Roadmap

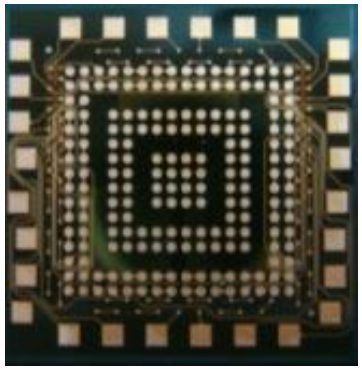


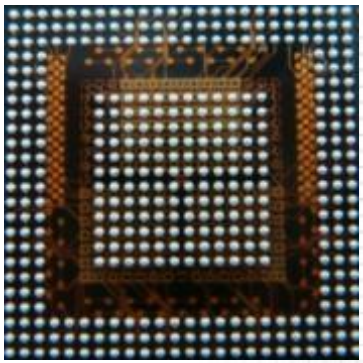
3D SiP Double-side eWLB PoP

Test Vehicle Description

- PKG: 12x12mm, 0.5mm ball pitch
- Die : 3-die, 2 (3x3mm) + (3x4mm)
- *Double-side RDL*
  (1L Top and 1L Bottom)
- I/O : 396 (bottom), 192 (top)
- Solder ball: 0.3mm, SAC305
- Thickness: 450um top package
  450um/250um bottom package







3D SiP Double-side eWLB PoP

Reliability : Component Level

Table. Package Level Reliability Results of thin eWLB packages.

*** Tested by ball shear test and O/S test**

Condition			Status
MSL1 JEDEC-J-STD-020D	MSL1, 260C Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon JESD22-A104	-40C to 125C	1000x	Pass
HAST (w/o bias) after Precon JESD22-A118	130C / 85% RH	96hrs	Pass
High Temperature Storage (HTS) JESD22-A103	150C	1000h	Pass
BST after Multiple Reflow	260C Reflow	20x	Pass

3D vertical interconnects :Preformed via Option

Preformed vias can be placed in eWLB package fan-out area as a multi-die structure

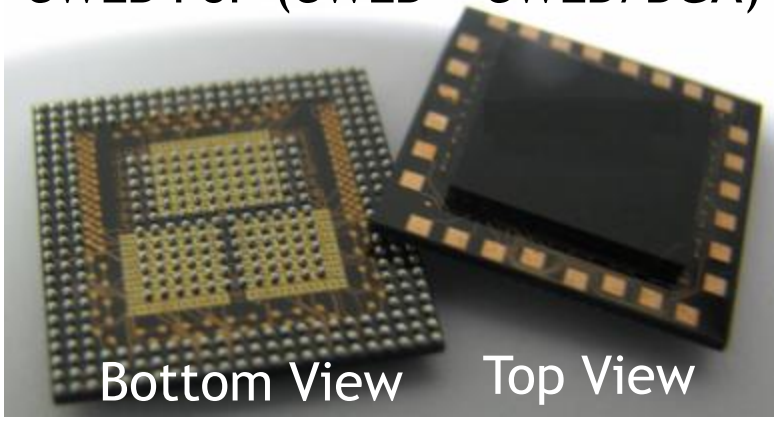
Pros

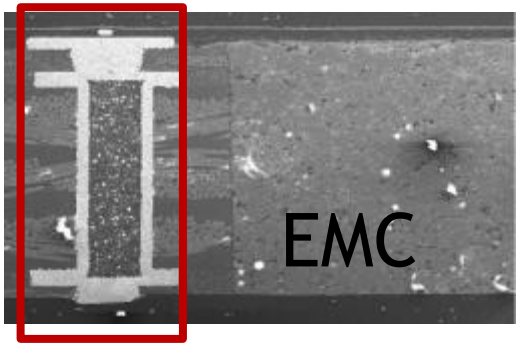
- Little technology development required
- Leverages mature PCB infrastructure
- Enables 2S RDL structures

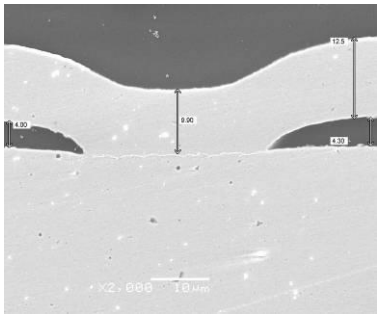
Cons

- Custom arrangement of vias more difficult
- Cost is higher than alternative structures

eWLB PoP (eWLB + eWLB/BGA)



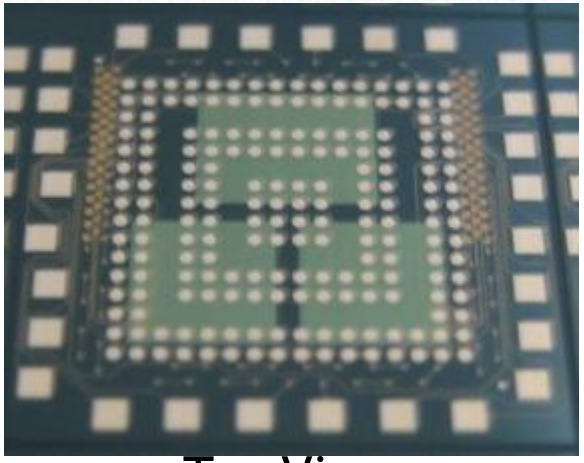




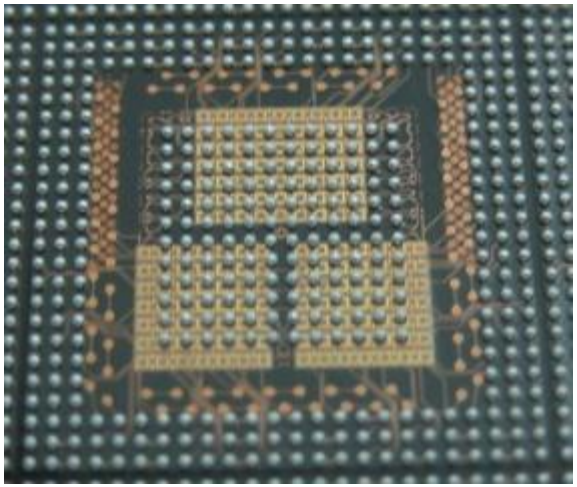
Vertical Via and via contact with Preformed Via

3D SiP Double-side eWLB PoP

2-sided eWLB

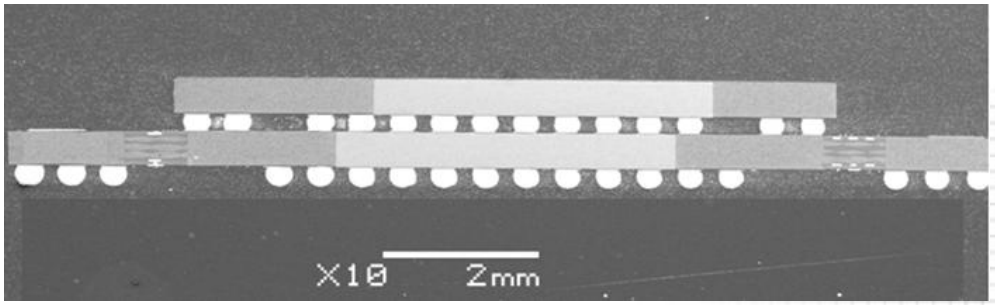


Top View



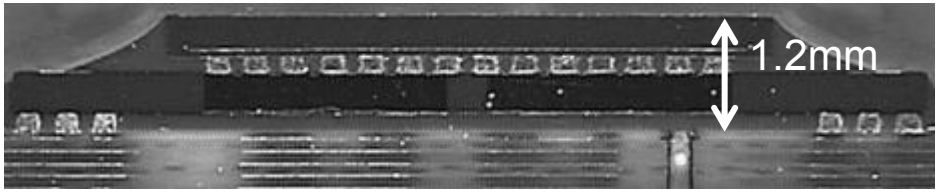
Bottom View

Bottom package 2S eWLB – 12x12mm, 3 die
Top package 1S eWLB – 8x8mm, 2 die
(Total 5 dies)

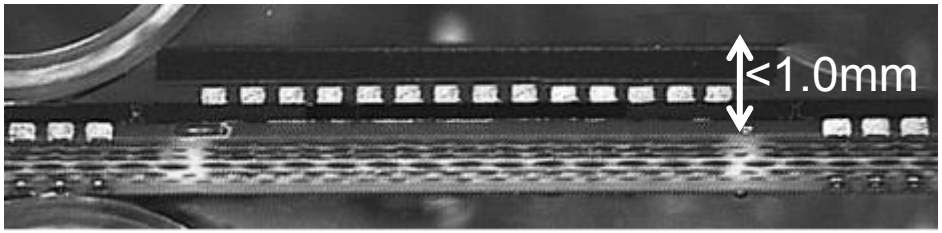


eWLB PoP (eWLB + eWLB)
Total PKG height ~ 1.2 mm

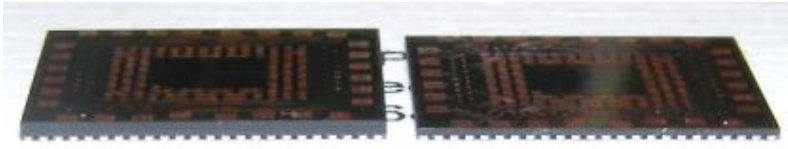
3D SiP Double-side eWLB PoP : less than 1.0 mm PoP height



250um Thin Bottom 3D PKG



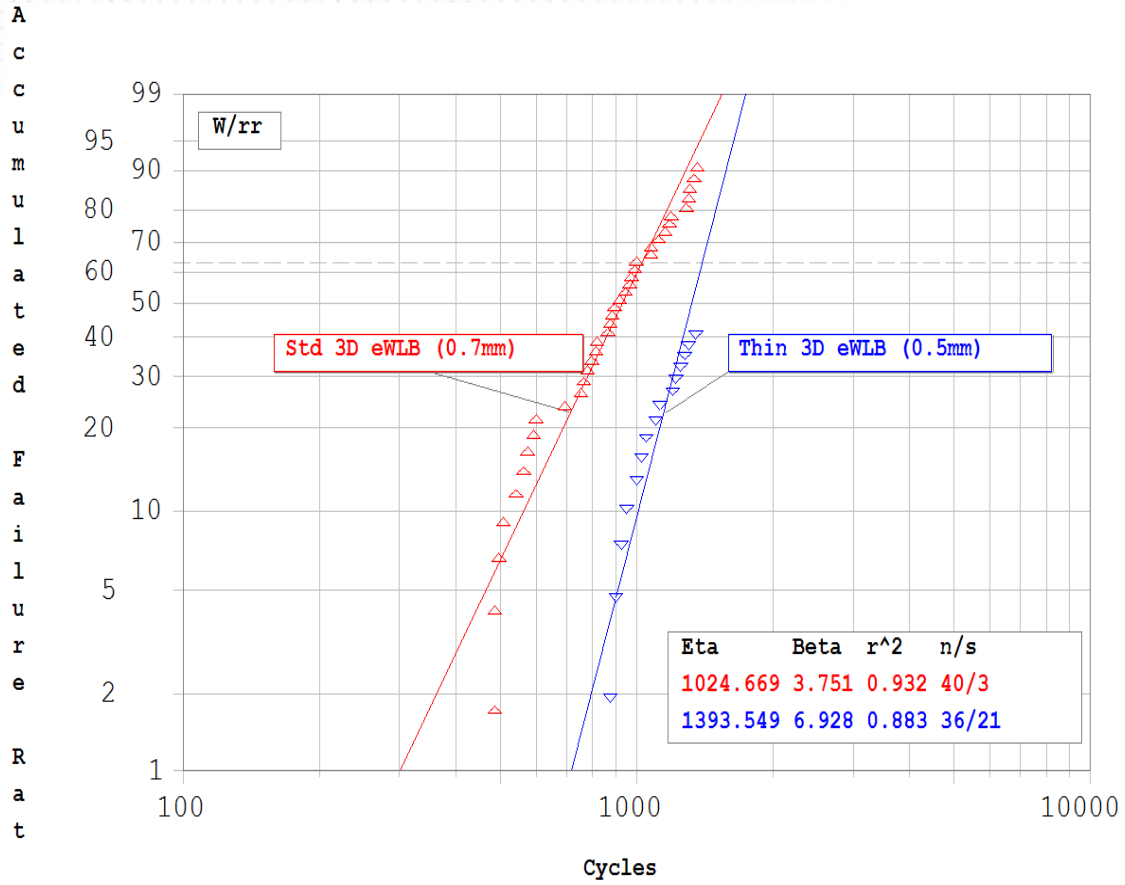
Low profile 3D eWLB PoP (12x12mm PoP-bottom package) with less than 1mm thickness including solder balls.



450um 250um

Picture of 3D eWLB PoP packages; Total less than 1.0 mm package height (including solder balls)

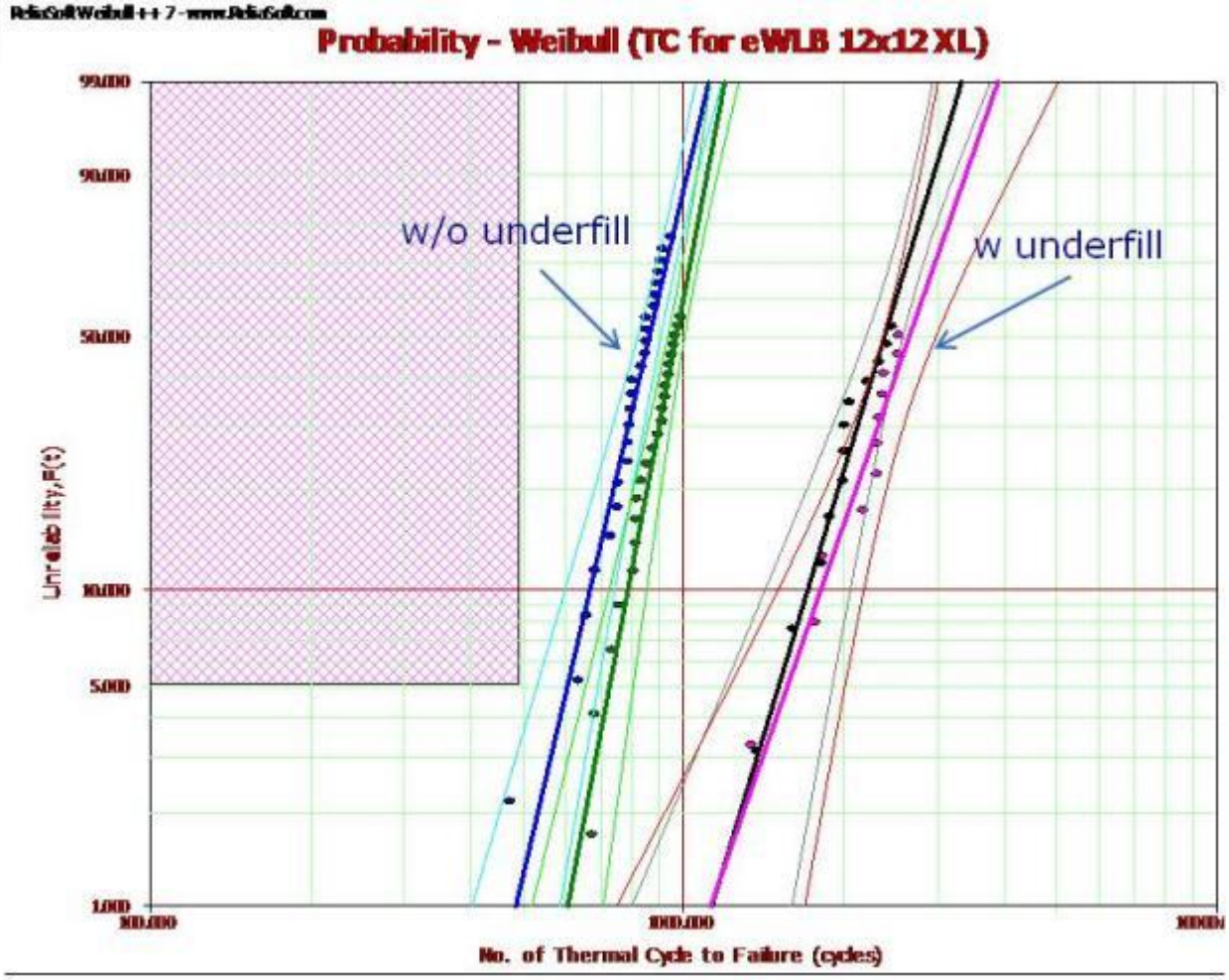
3D SiP Double-side eWLB PoP Board Level Reliability TCoB (without Underfill)

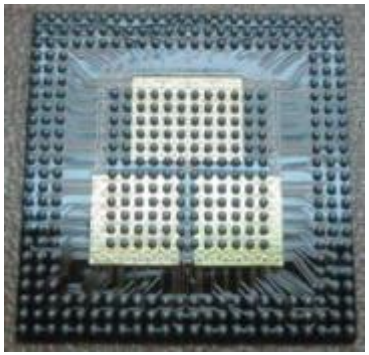


Thinner package showed 40% improved TCoB compared to standards

TCoB improvement with board level underfill

Board level underfill improved TCoB over 2 times

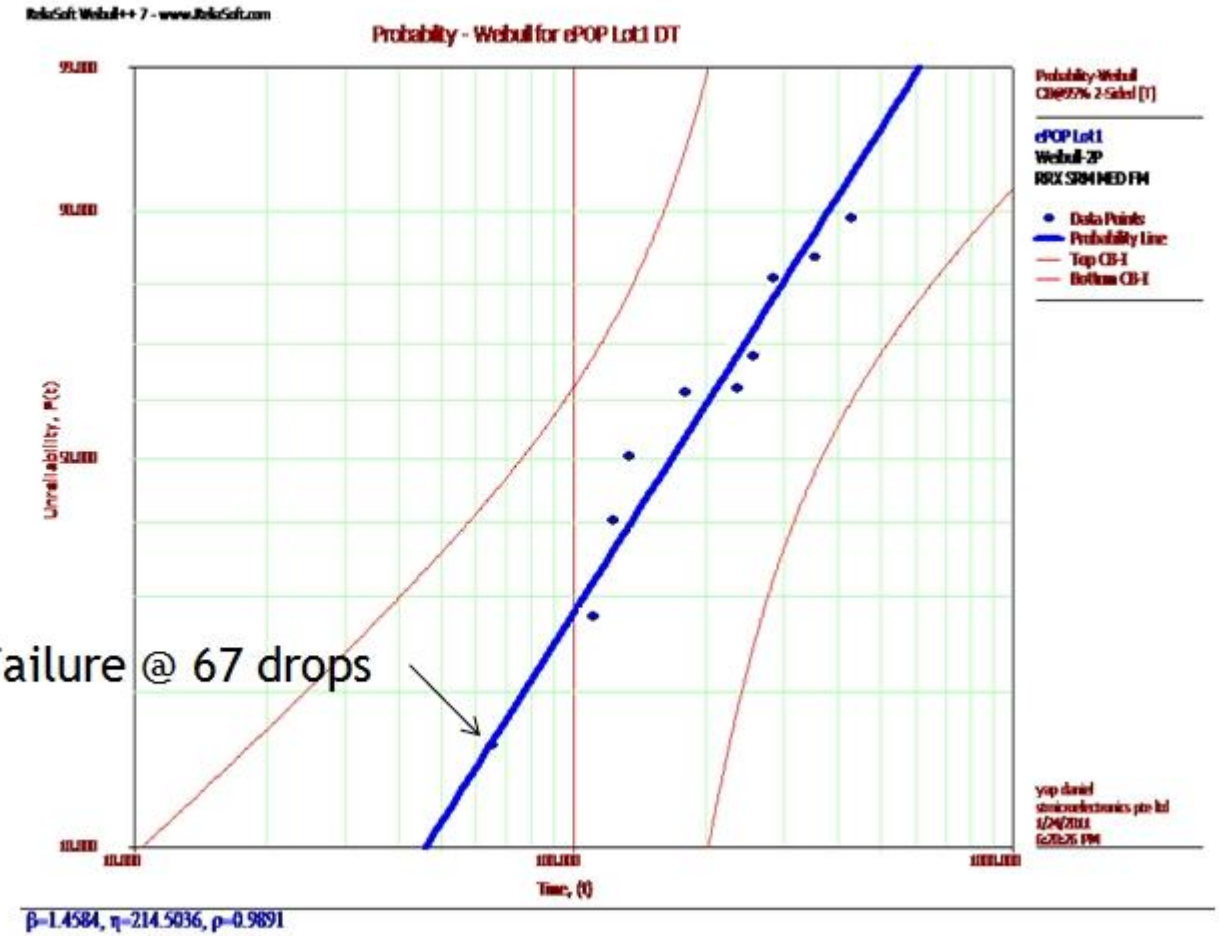




12x12mm eWLB with 3-die

3D SiP Double-side eWLB PoP

Board Level Reliability; Drop (without Underfill)

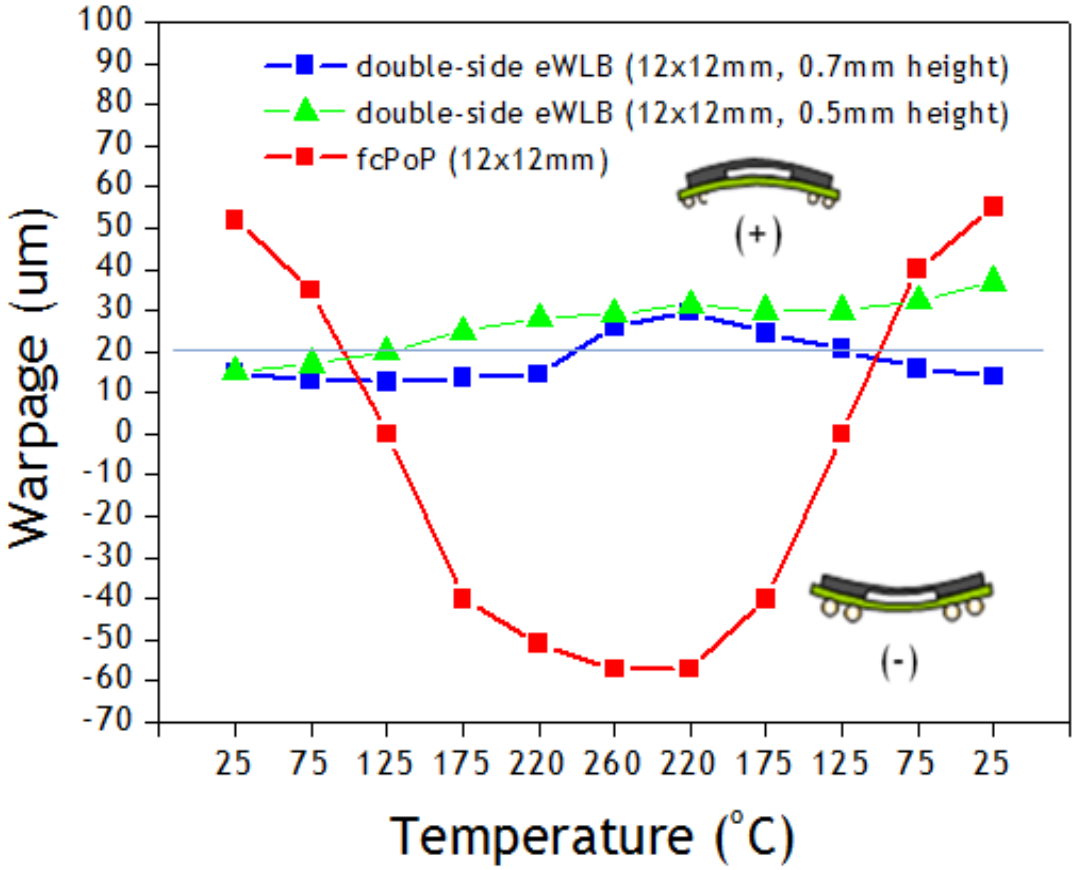


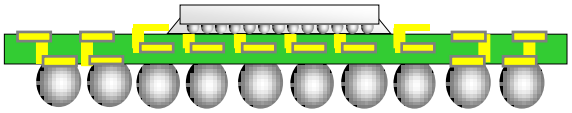
First Failure @ 67 drops

12x12mm eWLB Stacked Package

3D SiP Double-side eWLB PoP

PoP bottom PKG Warpage Behavior

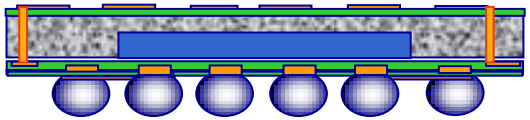




fcFBGA-PoP-b,12x12mm, 516I/O

Substrate thickness 0.43 mm

Die 8x8 mm



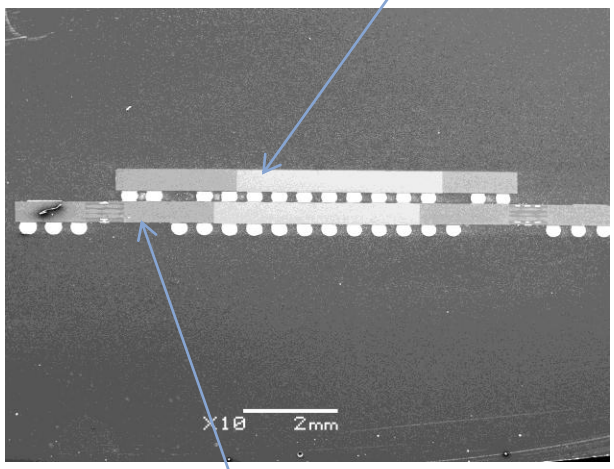
eWLB 12x12mm, 396I/O

PKG height 0.7 mm / 0.5 mm

3D SiP double-side eWLB shows stable warpage behavior with reflow profile so it provides advantage in PoP process, including improved yield and finer top ball pitch

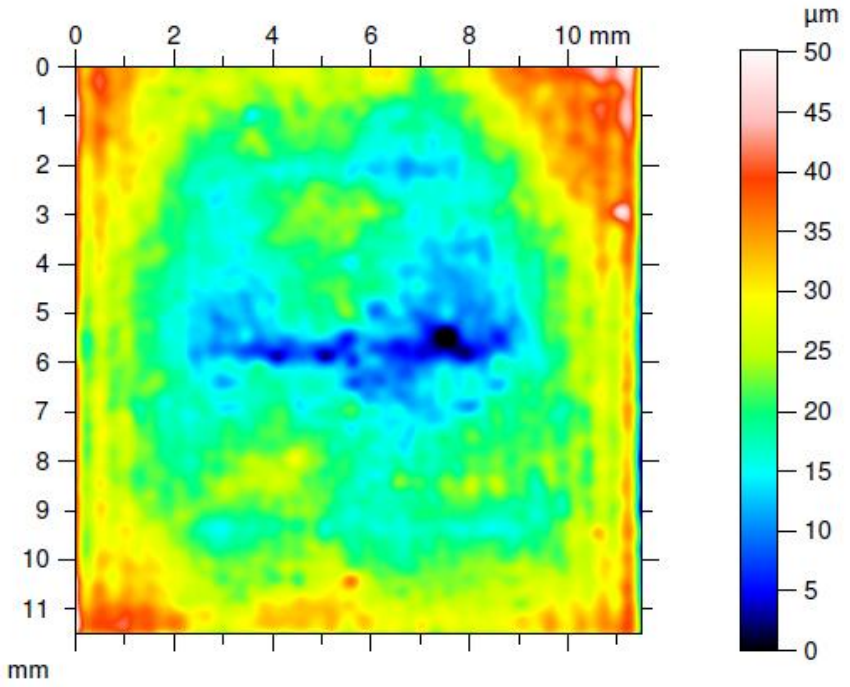
3D SiP Double-side eWLB PoP
PoP stacked PKG Warpage behavior

Top package: eWLB 8x8, 2 dice



Bottom package: eWLB 12x12, 3 dice

TDM of package



Max warpage: 50um

Topography and Deformation Measurement

Summary

- Next generation eWLBs are qualified for large die, small die, multi-die, 2L RDL and 3D SiP double-side eWLB.
- 3D SiP double-side eWLB shows good reliability both for component and board level.
  - Low warpage behavior supports improved PoP assembly process yields.
- eWLB fan-out technology enables novel 3D PoP structures
  - Double sided PoP for addition of RDL layers on top of bottom die
  - Top RDL layers can enable single or multi-die placement for top packages
- 3D eWLB PoP technology achieves
  - Heterogeneous die integration and higher IO density in a significantly smaller footprint than is possible today with standard PoP and flip chip technology.
- The maximum benefits of eWLB PoP can be achieved through a co-design process with customers to optimize the functional performance of this ultra thin 3D package.

STATSChipPAC

Thanks!

Questions Welcome