Development of 2.5D and 3D IC Fabrication and Assembly Technologies

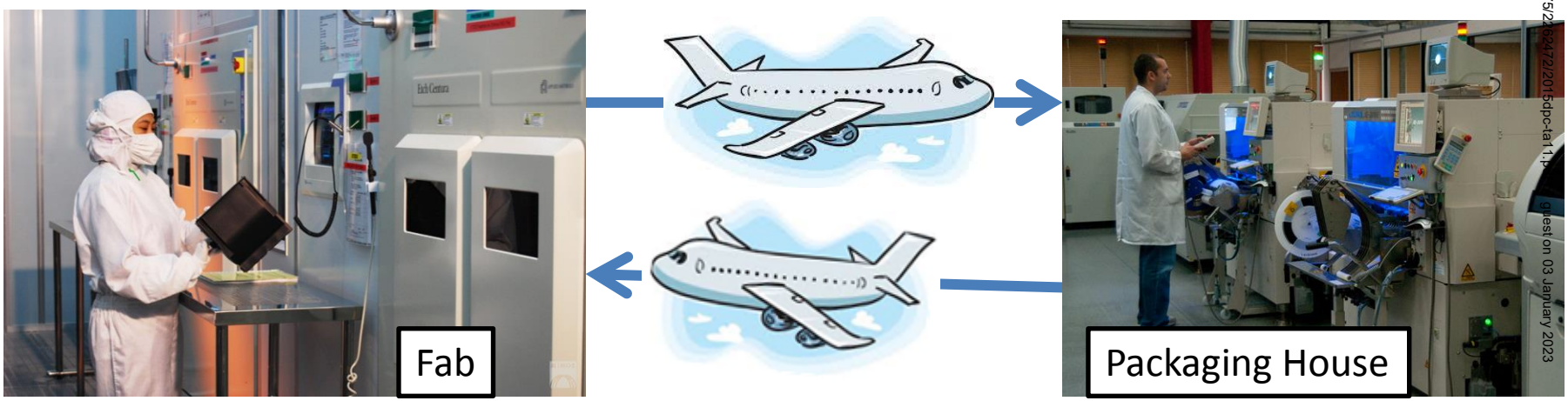
Guilian Gao, Hong Shen, Sangil Lee, Bong-Sub Lee, Scott McGrath, Liang Wang, Charles Woychik, Cyprian Uzoh, Grant Villavicencio, Roseann Alatorre, Sitaram Arkalgud

OUTLINE

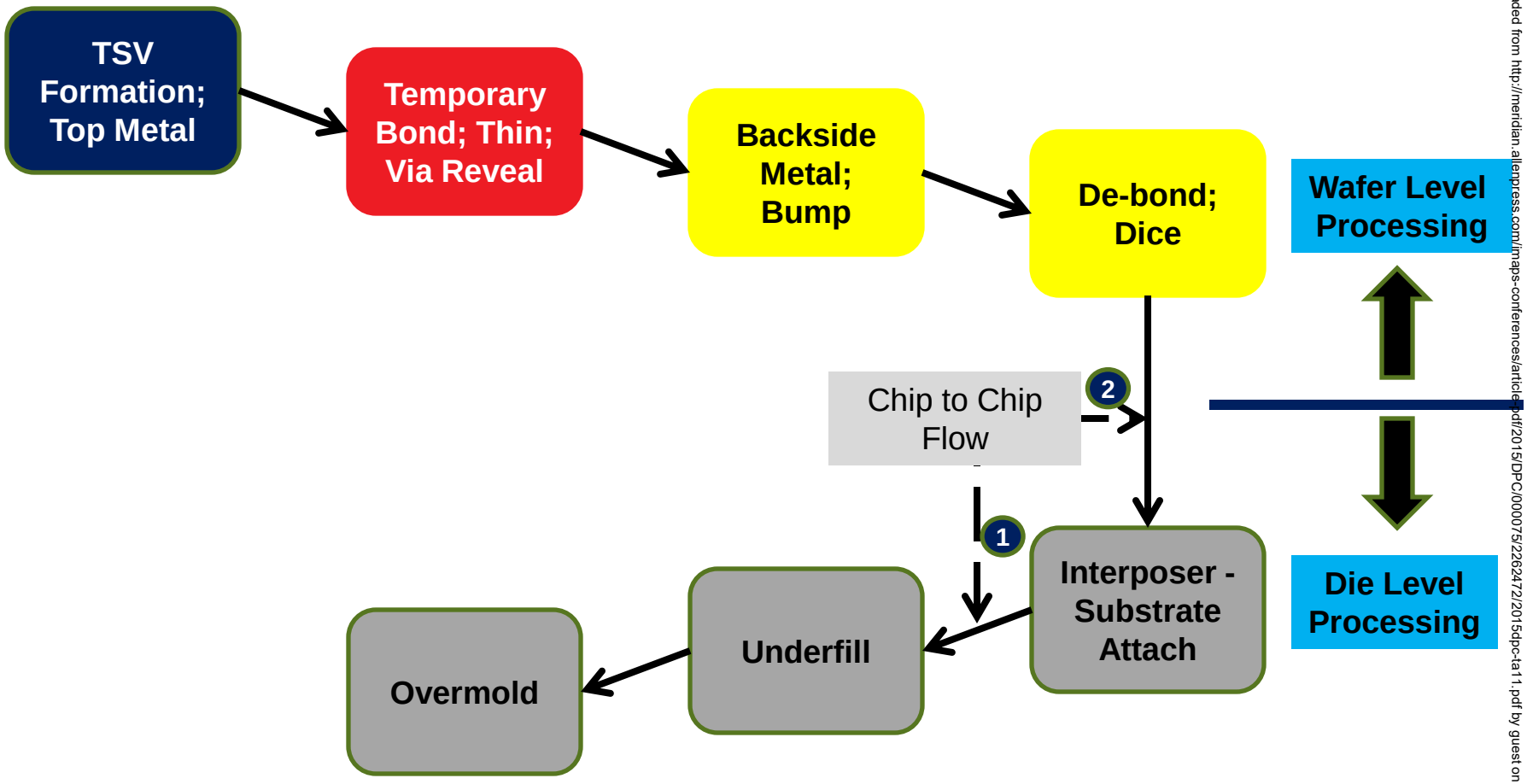
- Introduction
- Thin silicon wafer handling challenges and solutions
- Fine pitch inter-connection and solutions
  - Solder capped µbump assembly
  - Cu to Cu direct bonding
- Design, materials and process considerations
- Summary

Introduction

- Traditional Packaging Mode:
  - Wafer fab completes all wafer processing
  - Singulated die gets assembled at packaging houses
- 2.5D and 3D packaging
  - Traditional mode still applies to some assembly flows (chip to chip)
  - Some assembly flows requires round trip to wafer fab (chip to wafer)
  - Different flow has different challenges

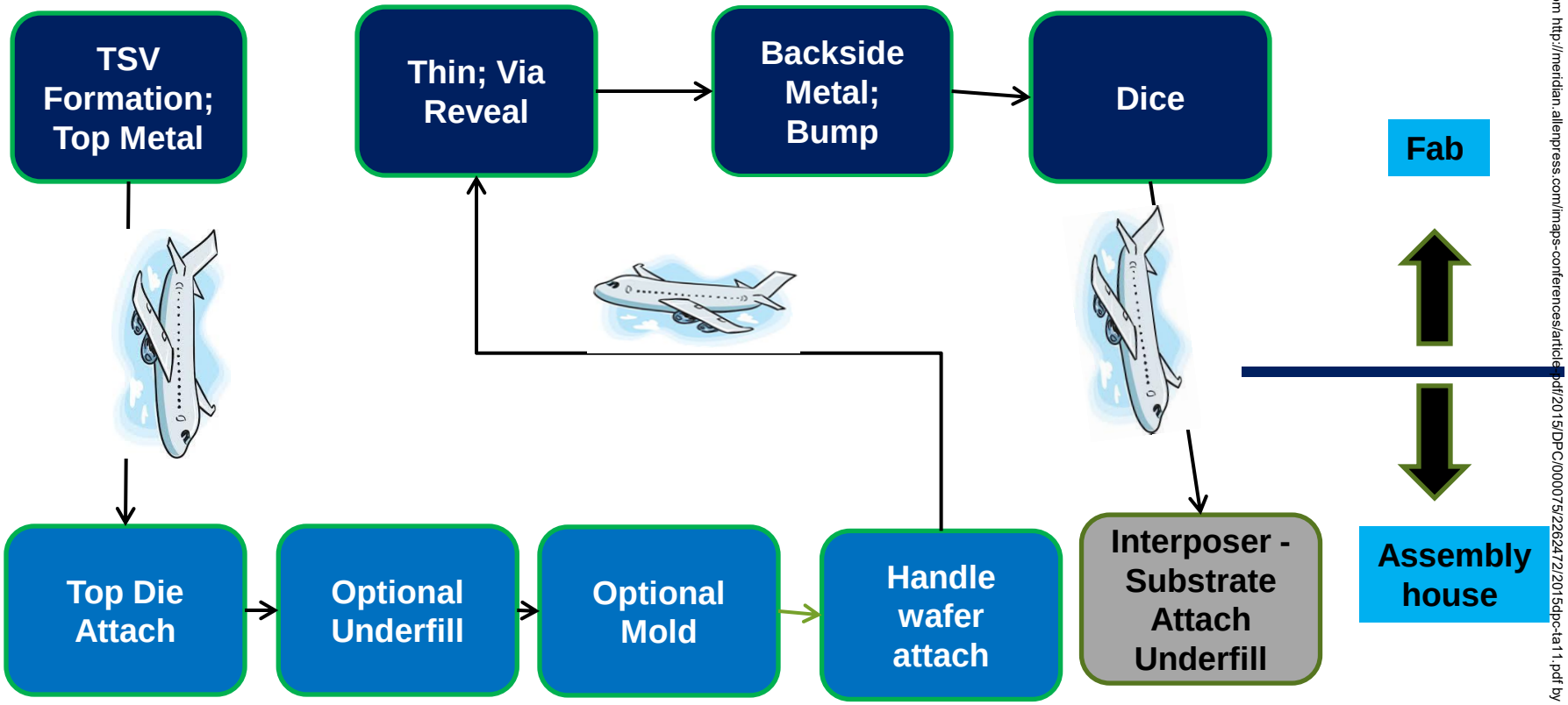


Chip to Chip (Fab Process First) Flow



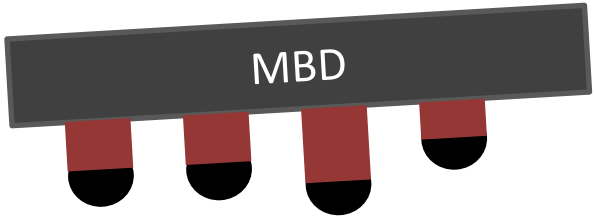
- Fits conventional assembly mode better
- Temporary bond/de-bond (TBDB) processes are extra steps that add cost
- TBDB also imposes low temperature backside processing ➔ oxide and PI quality impact

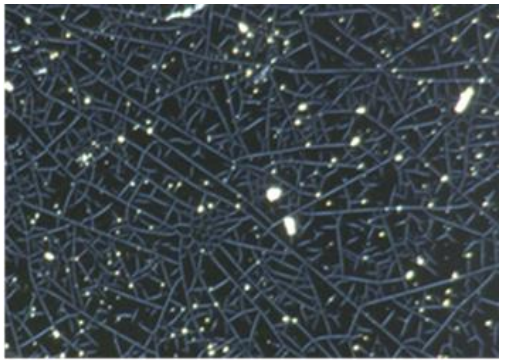
Chip to Wafer (Fab Round-Trip) Flow



Challenges

- Thin silicon
  - Wafer handling and temporary bonding
- MBD attach:
  - Solder bonding: very small assembly window
  - Cu-to-Cu bonding: new process
- Low temperature passivation materials
  - Marginal properties
- Multiple materials with large CTE mismatch
- Tight gap cleaning and underfill





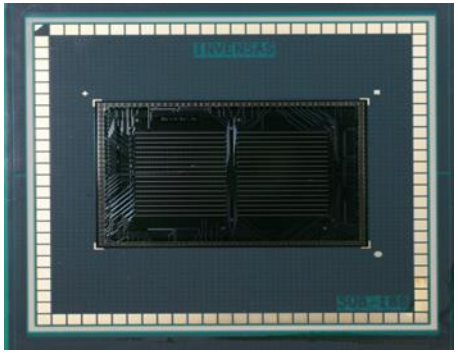
Assembly Flow Exploration at Invensas

Flow 1 (C2C)

Thin interposer to Substrate attach

µBump Die to Interposer attach

Underfill Interposer & µBump Die, overmold

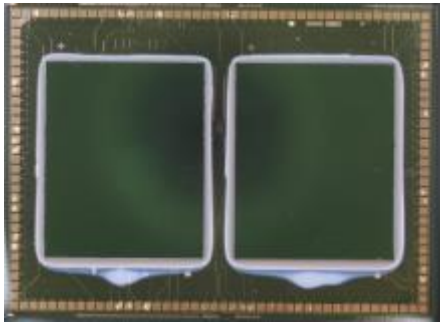


Flow 2 (C2C)

µBump Die to thin Interposer attach, underfill

Interposer to substrate attach

Underfill Interposer to substrate, overmold

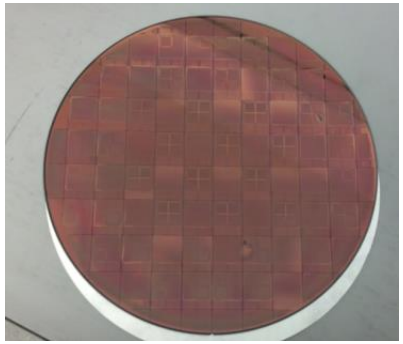


Flow 3 (C2W)

µBump Die to thick Interposer wafer attach, (underfill, mold)

Carrier wafer attach, Wafer level backside processing

Dice, attach to Substrate



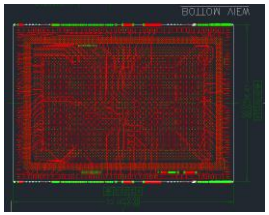
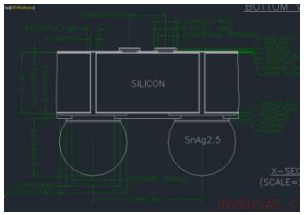
High throughput, high yielding, low warpage assembly process with high reliability is a must!

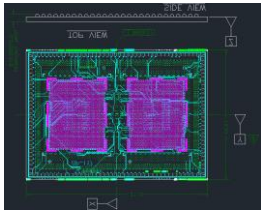
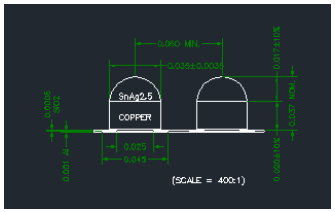
Comparison of Assembly Flows

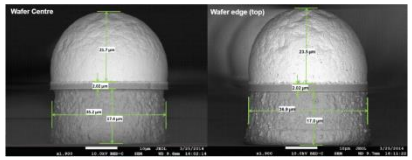
Key Attribute	Flow 1 (C2C)	Flow 2 (C2C)	Flow 3 (C2W)	Note
	Interposer to Sub Attach (solder)	µbump die to interposer attach (solder), Underfill	µbump die to interposer attach (Cu-Cu or solder), underfill mold	
	µbump die to interposer attach (solder)	Interposer module to sub attach (solder)	Wafer backside processing	
	Underfill	Underfill	Dice, interposer module to sub attach (solder), underfill	
Require thin wafer handle?	Yes	Yes	No	Cost, temperature restriction, yield loss
Temp bond/de-bond	Yes	Yes	No	Cost, temperature restriction, yield loss
Warpage control in assembly				
Stress in FC ball				

Test Vehicles

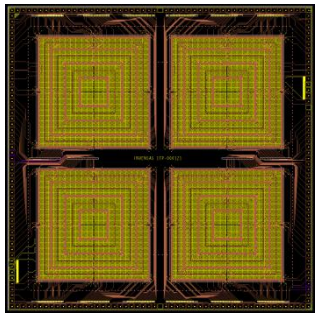
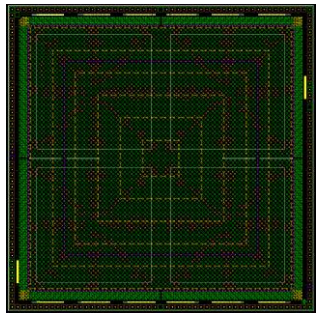
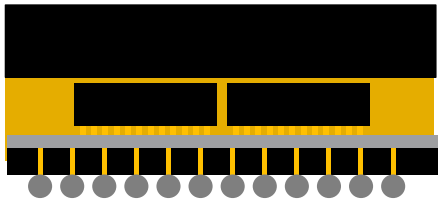
Chip to Chip Test Vehicle



Chip to Wafer Test Vehicle

	Chip - Chip	Chip - Wafer
Interposer Size (mm2)	27x19	24x24
TSV Dimensions (um)	10x100	5x50
# of TSVs	8615	4000
FC Bump Pitch (um)	180/250	180/250
# of FC bumps	7076	8872
Top Die Size (mm2)	10x12	9x9
# of Top Dies/Interposer	2	4
Min Micro-bump Pitch (um)	60	30
# of Micro-bumps/die	7744	32098
Bond Metallurgy	Solder capped Cu pillar	Cu-Cu direct bond

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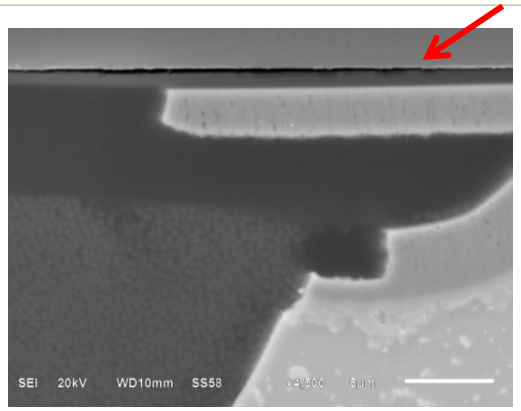
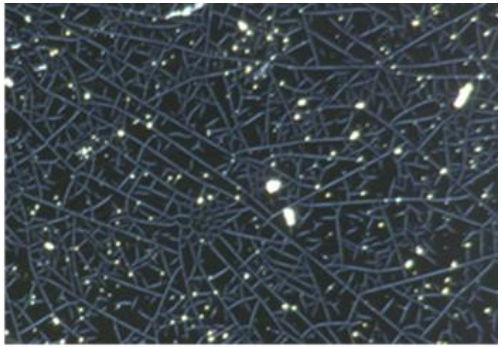
Temporary Bonding/ De-bond Problems

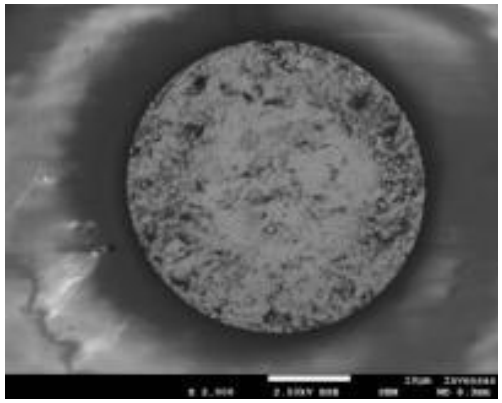
- Extra Cost
- Restricts backside processing temperature
  - Low temperature oxide/ nitrides tends to have poorer adhesion
  - Low temperature PI has marginal properties
  - Bonding adhesive residue can interfere with soldering
- Ongoing challenges, no good solutions yet



LTO delamination in X-section



LTPI cracking After flux cleaning



Carbonaceous Contamination On bond solder pad

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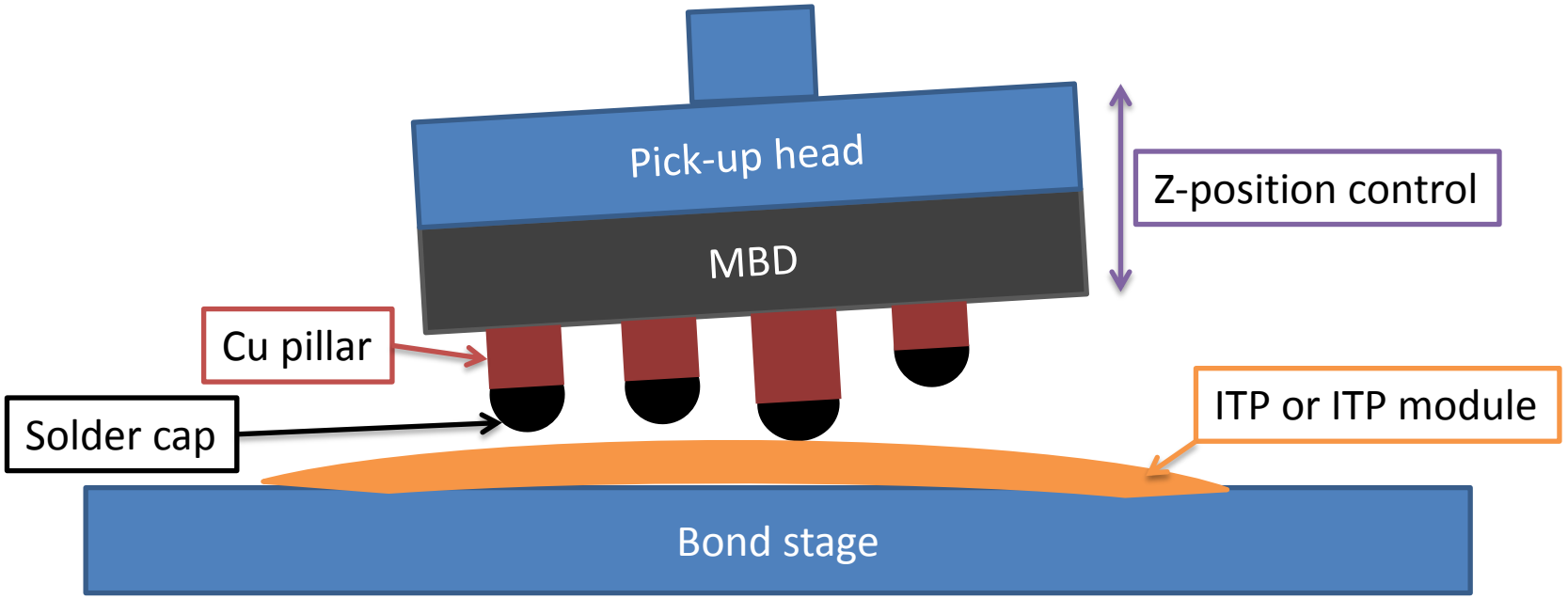
Assembly Window for µbump Die Solder Attach

- MBD bump co-planarity ← In-coming part quality
- In-situ ITP or ITP module warpage ← Assembly flow
- Non-parallelism between head and stage
- Z-position control accuracy ← Bonder capability

< 1/10 of thickness of human Hair



Flipchip & Microbump Process Windows

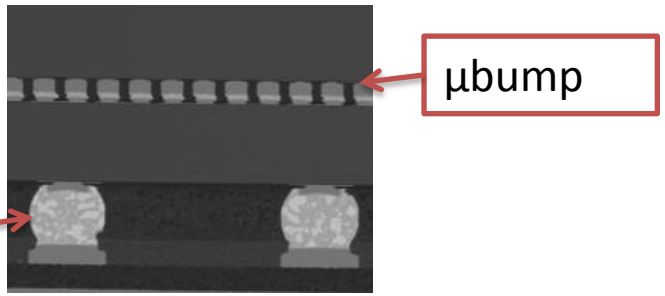
Flip Chip

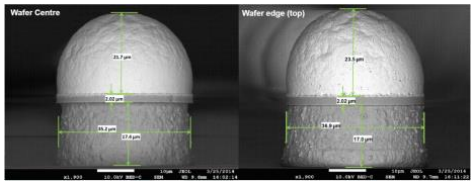
- Large pads → easy to align
- Large pitch → easy to avoid shorts
- Large solder volume
  - → more room to stretch or collapse

Microbump die

- Small pads → harder to align
- Small pitch → harder to avoid shorts
- Very small solder volume
  - → Very little room to stretch or collapse

	FC	Microbump	Comments
Pitch (um)	180	45	
Diameter (um)	90	25	
Solder Volume (um3)	381,510	4,089	4/3πr3 (FC) or 2/3πr3 (half sphere for microbump)
Equivalent Column Height (um)	60	8	
Min Compressed Column Height before Bridging(um)	17	3	(Diameter)^2*Eq Col Ht/((Pitch -10)/2))^2
Minimum Solder Collapse for Joint Formation (um)	2	2	Assumed
Acceptable TTV Window (um)	71	7	



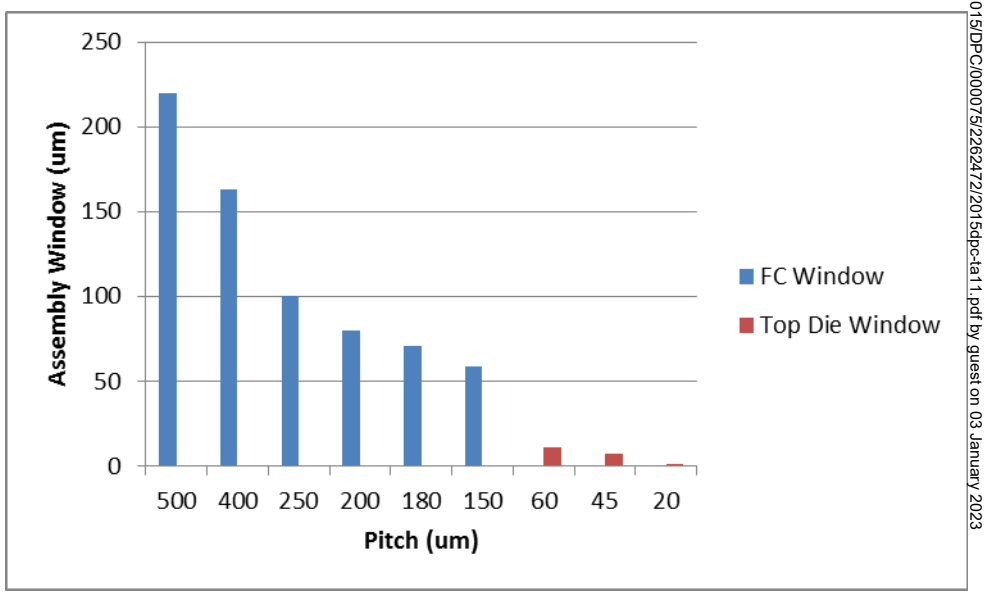


Solder capped Cu pillar microbumps

Bump Scalability Assessment – Solder Volume

Pitch (um)	Ball diameter (um)	Volume (um3)	Equiv Column Height (um)	Compressed Column Height (um)	FC Window	Top Die Window
500	300	14130000	200	78	220	
400	200		133	35	163	
250	125		83	23	100	
200	100		67	18	80	
180	90	381510	60	17	71	
150	75		50	14	59	
60	35		12	5		11
45	25		8	3		7
20	10		3	2		1

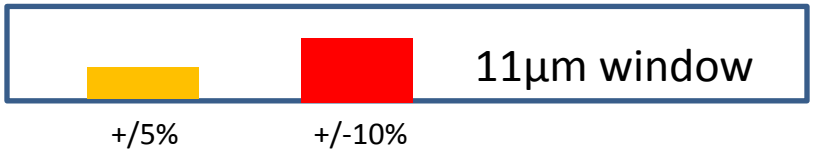
- TCB microbump assembly window is extremely tight
- Solder volume, TTV and bond tool capability have a large impact



Impact of Incoming MBD Co-planarity

- **Controlling in-die bump height uniformity is critical for assembly**
- Cases in study
  - Case 1: MBD with 45µm pitch and 25µm diameter bumps: 7µm window
  - Case 2: MBD with 60µm pitch and 35µm diameter bumps: 11µm window
- Total bump height: 35µm
- +/- 5% variation: 3.5µm
- +/- 10% variation: 7µm

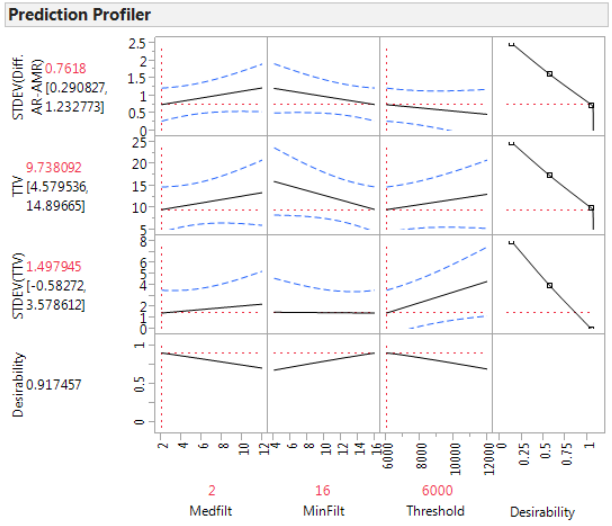
Case 1

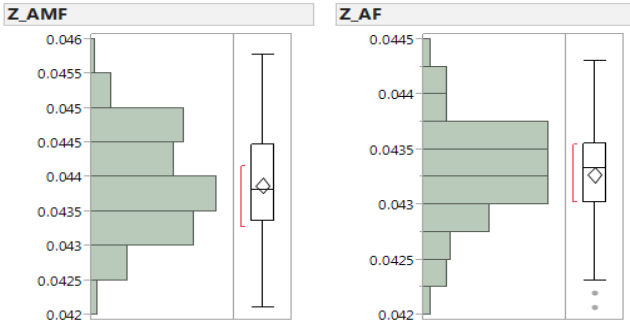


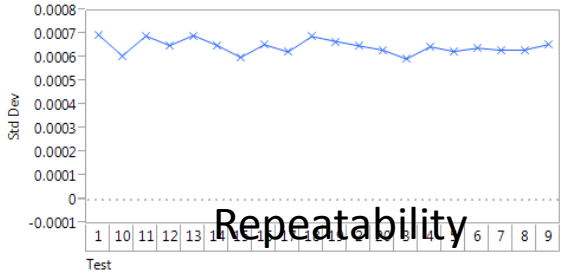
Case 2

Solution to Height Variation: Control by Inspection

- Leveraged a in-house low-cost inspection tool
- Capable of inspecting 3900 bumps in critical area with <0.5um accuracy
- Area multi-focus mode v. Auto-focus mode.
  - AMF mode—8 minutes per die
  - AF mode—15 hours per die



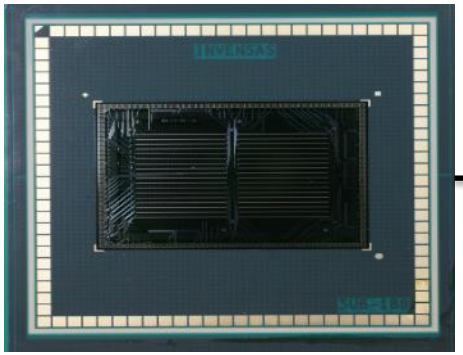


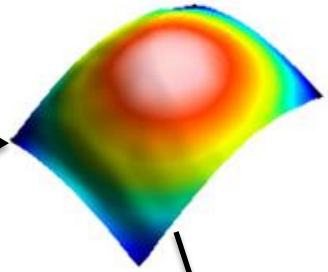


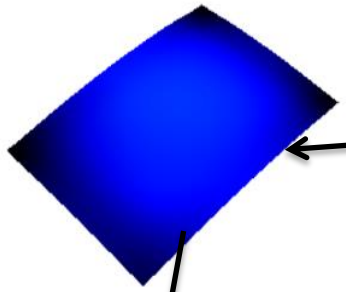
Challenges and Solutions for Microbump Inspection (Poster Session)

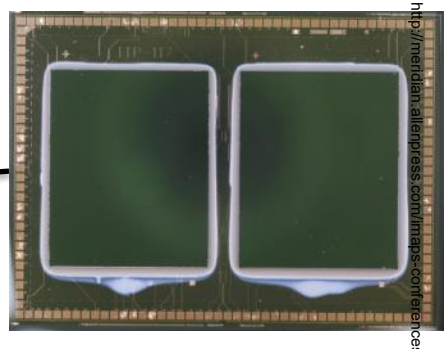
Hong Shen, Invensas Corp. (Xuan Li, Gabe Guevara and Sitaram Arkalgud)

Comparing Flow 1 and Flow 2



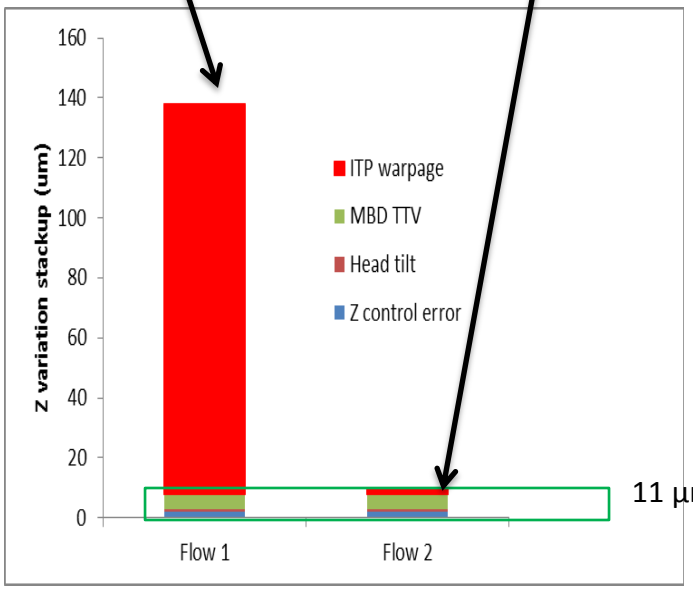






Flow 1

Very high warpage
Due to CTE mismatch
Between ITP and
Organic substrate

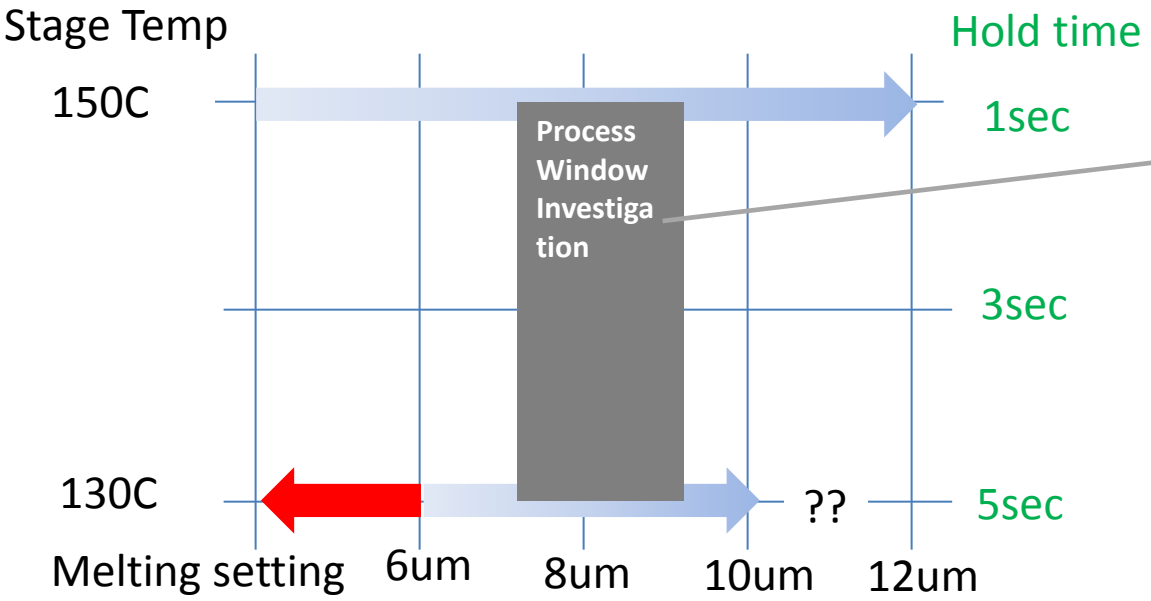


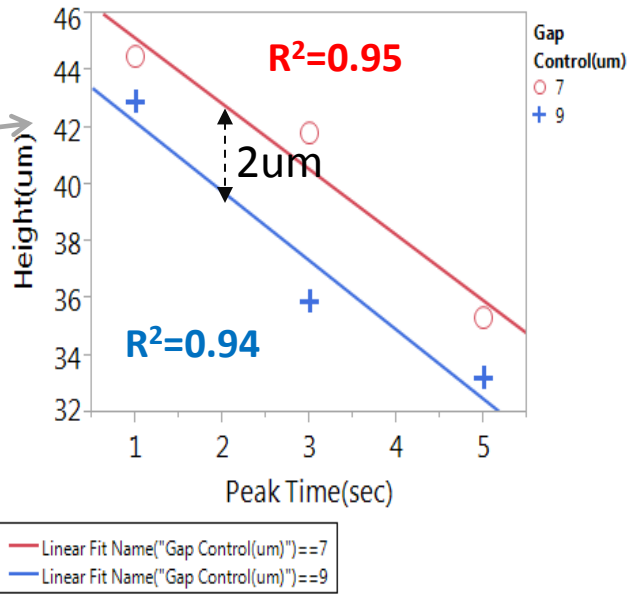
11 µm window

Flow 2

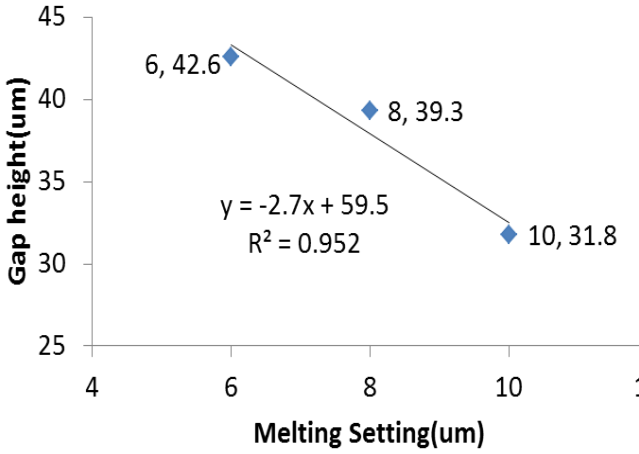
Low warpage
Due to CTE match
Between ITP and MBD

DOE on the TCB Process for µbump Die Attach

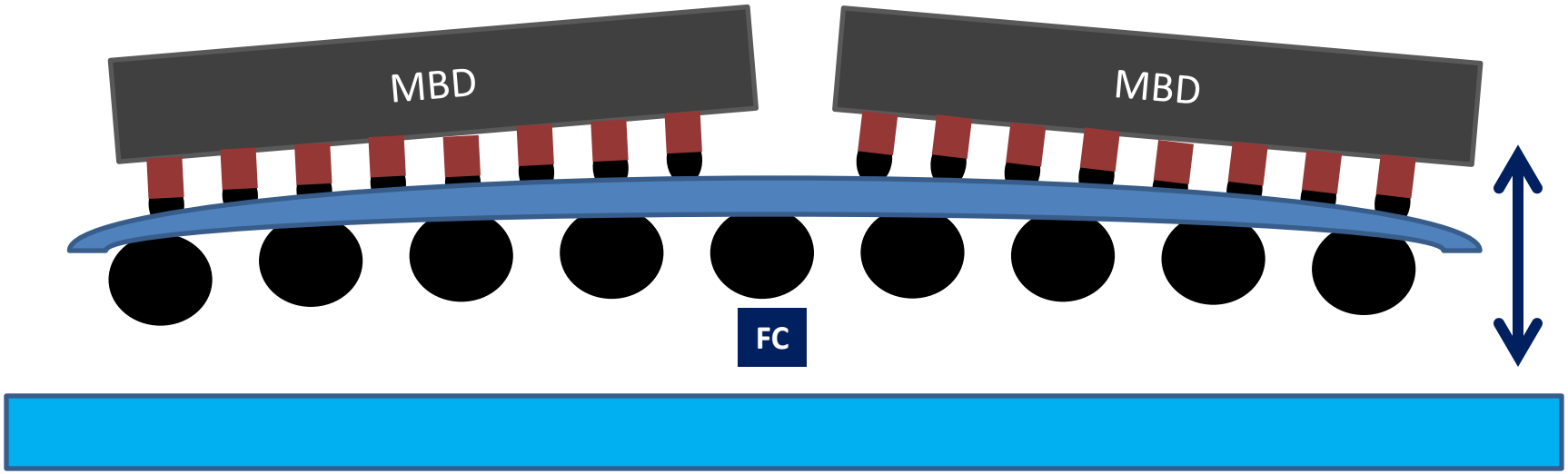




DOE on multiple process parameters
To establish good assembly process window

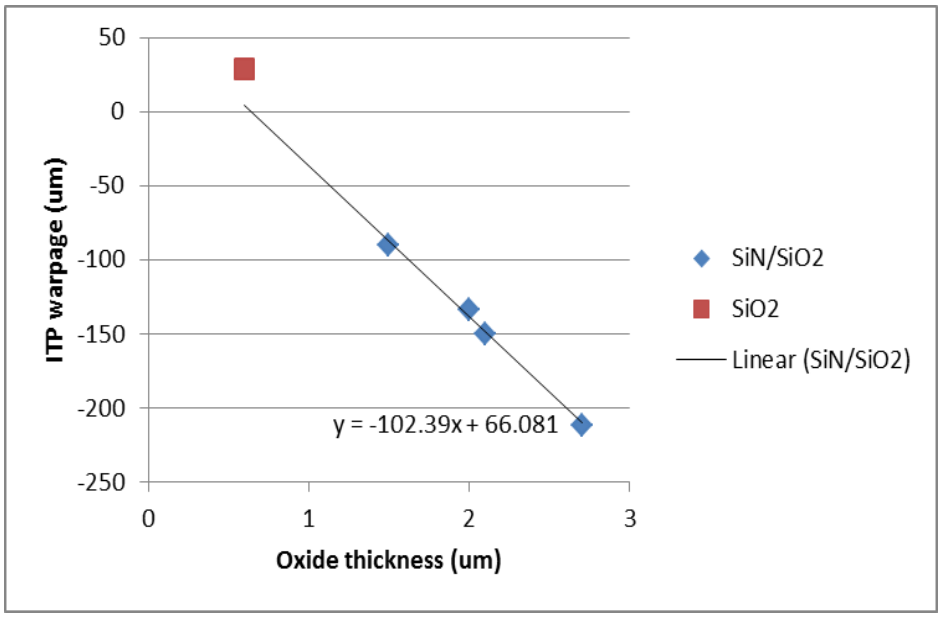


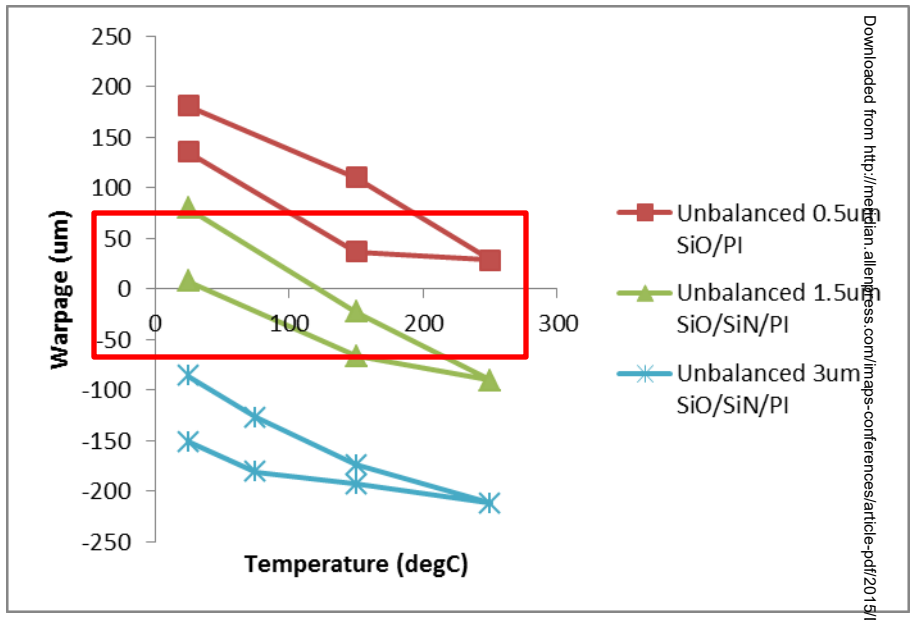
Interposer to Substrate Attach (Reflow)



- No active warpage control
- Maintaining a flat interposer at reflow temperature is critical to ensure contact at all bond pads
- Positive warpage (smile) at reflow results in opens at the corners
- Negative warpage (frown) at reflow results in opens at center

Chip-to- Chip Flow: Thin Interposer Warpage with Temperature

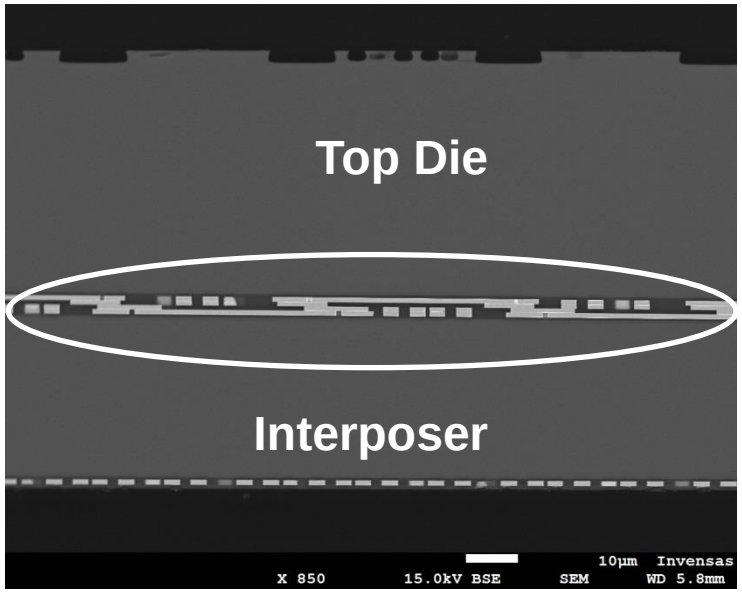


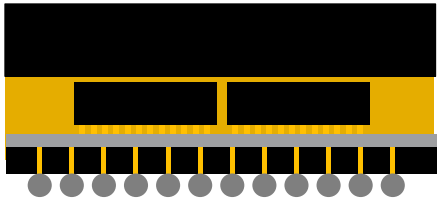


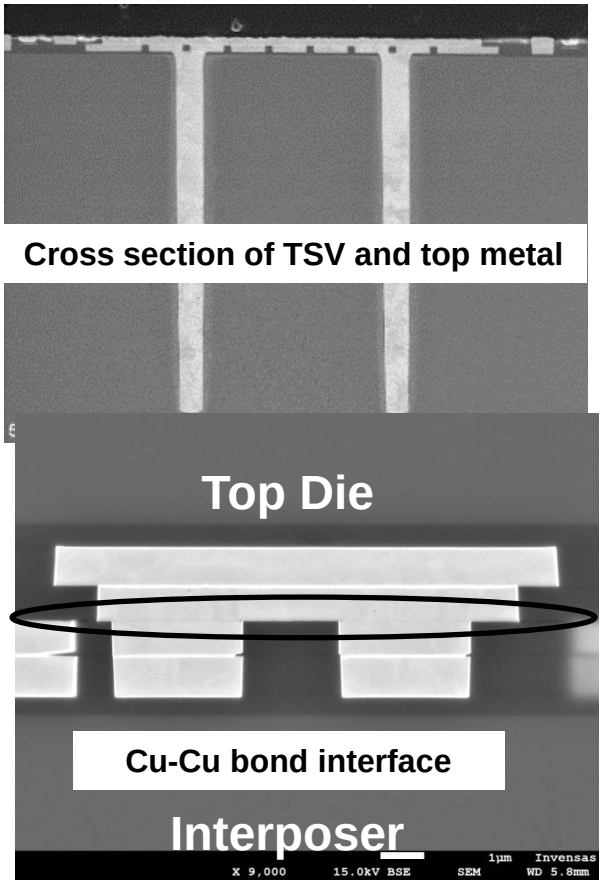
Pitch (um)	Ball diameter (um)	Volume (um3)	Equiv Column Height (um)	Compressed Column Height (um)	FC Window
500	300	14130000	200	78	220
400	200		133	35	163
250	125		83	23	100
200	100		67	18	80
180	90	381510	60	17	71
150	75		50	14	59

- As deposited warpage of a 100 um interposer varies considerably with dielectric thicknesses (~ 100um warpage/um of dielectric thickness)
- Warpage during thermal cycling (slope) affected by bottom PI thickness (unbalanced)
- Warpage at reflow temperature needs to be within assembly window

Chip to Wafer Assembly with Cu-Cu Direct Bonding

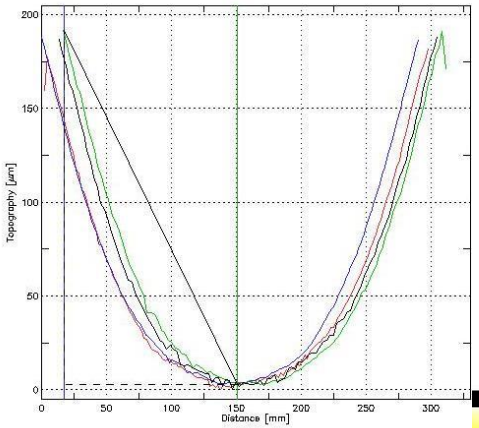


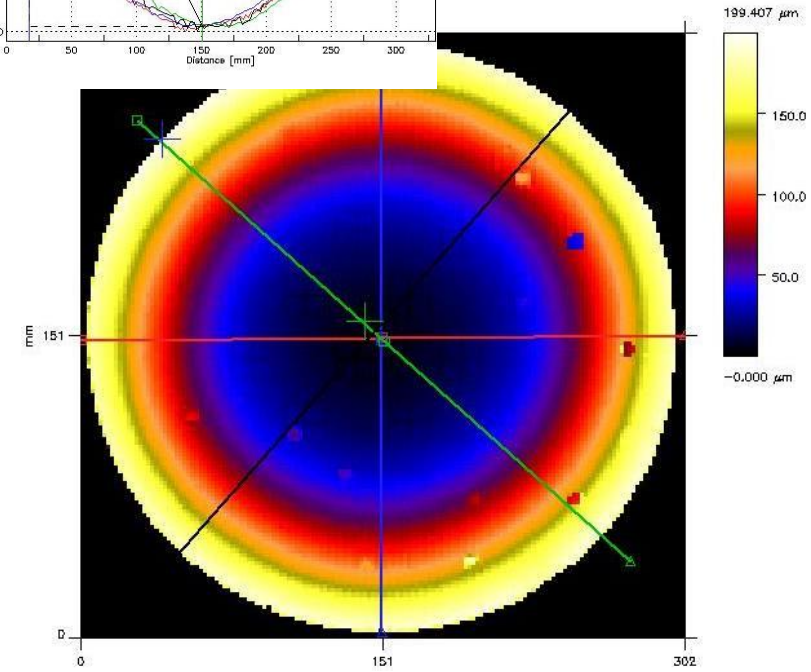


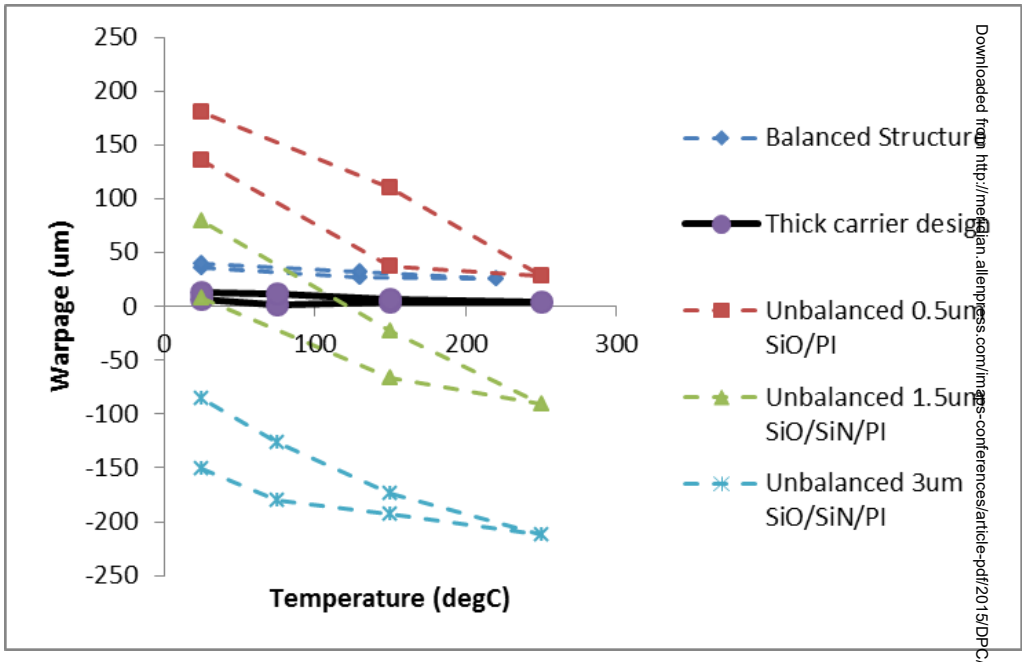


- Cu – Cu bonding avoids solder volume issue with scaled microbumps and underfill
- Surface planarity, throughput and defectivity become critical concerns

Chip – Wafer Flatness



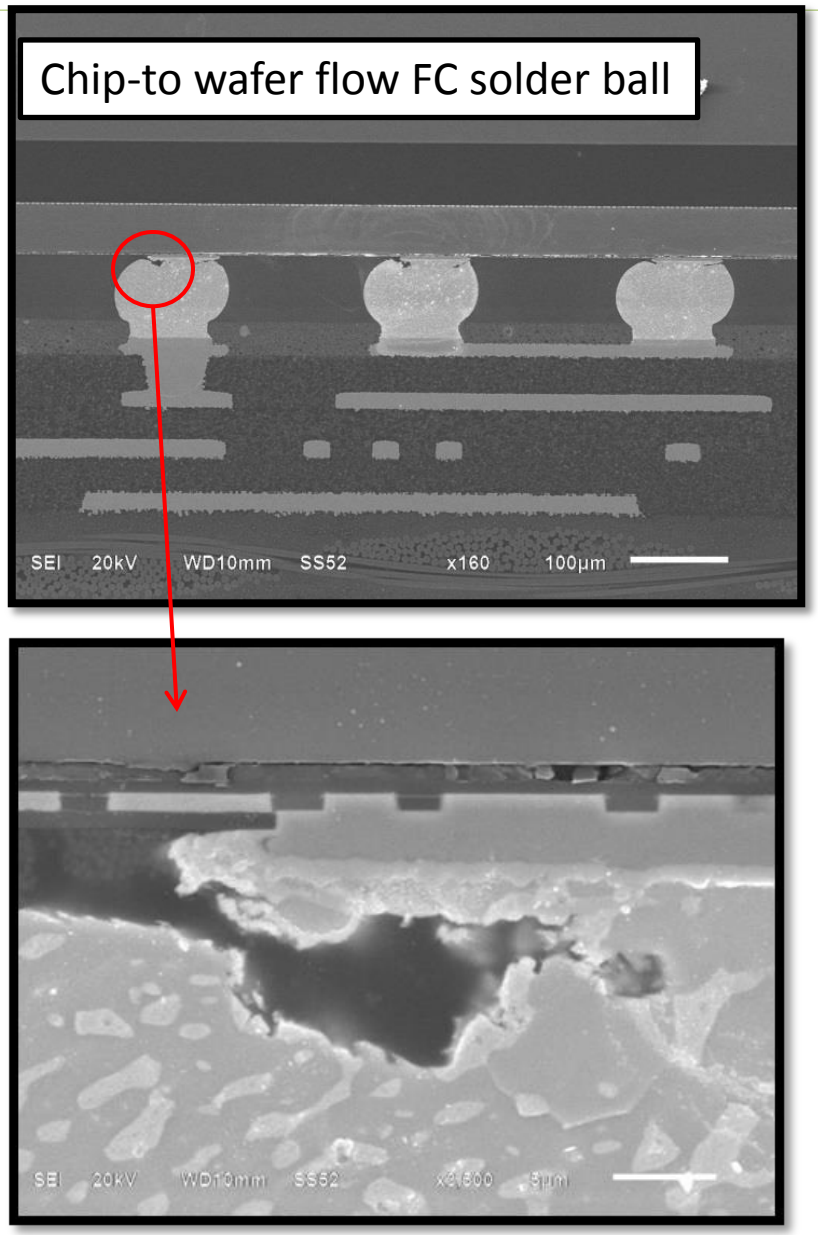




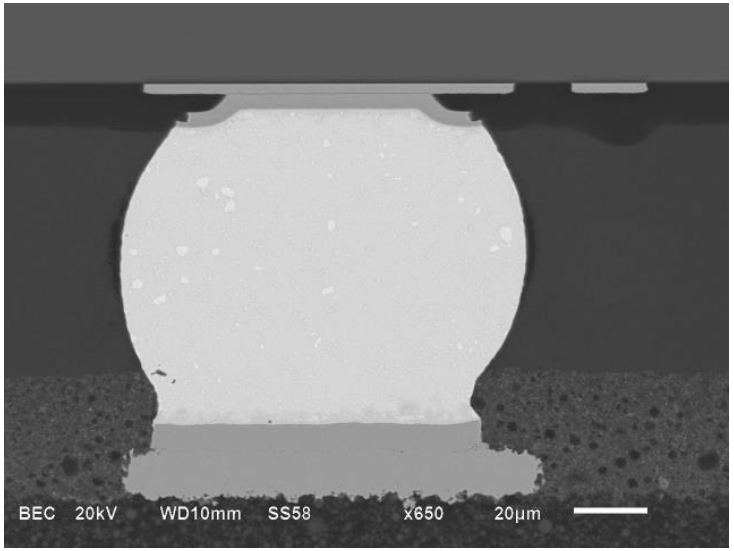
- Using a permanent handle wafer reduces wafer bow to < 200um across 300mm wafer
- Interposer flatness is dominated by thick Si handle cap – almost zero

Chip-to-Wafer Flow: Very High Stress in FC joints

Thick Si cap reduces warpage
But creates high stress in FC joints



Chip-to-chip flow FC solder ball



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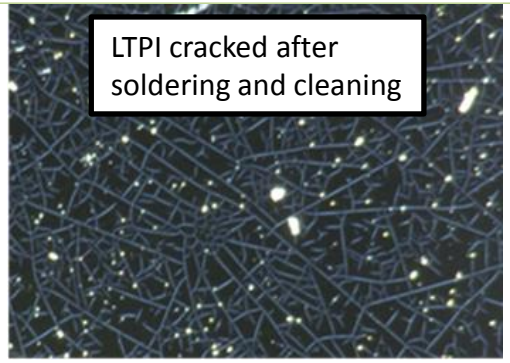
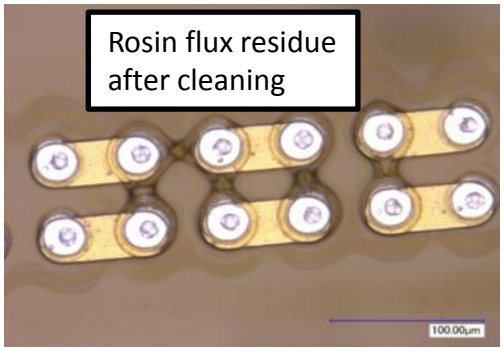
OUTLINE

- Introduction
- Thin silicon wafer handling challenges and solutions
- Fine pitch inter-connection and solutions
  - Solder capped µbump assembly
  - Cu to Cu direct bonding
- Design, materials and process considerations
- Summary

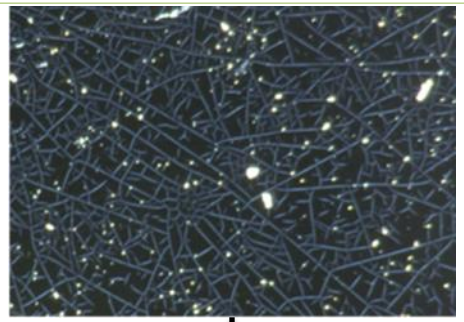
Design, Materials, and Process Considerations

- Low temperature curable polyimide
  - Poor chemical, thermal and mechanical properties
- Flux selection and cleaning
  - Tight gap, hard to remove residue
- Underfill selection, design optimization and cure
  - Tight gap, hard to fill, easy to form voids





Low Temp Curable PI Inferior to High Temp PI



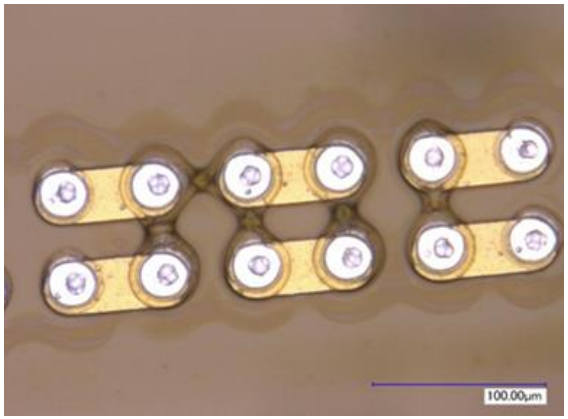
Material	Volatile content	H_2O Absorptn	Chem. Resistance	Adhesion	Tensile strength
LTPI #1	5	5	Fail	1	2
LTPI #2	6	6	Fail	NT	NT
LTPI #3	3	3	Pass	1	Brittle, no elongation
HTPI #1, 350°C cure	1	1	Pass	2	1
HTPI #2, 320°C cure	2	4	Pass	NT	NT

* 1--Best, 6--worst
** NT: Not Tested

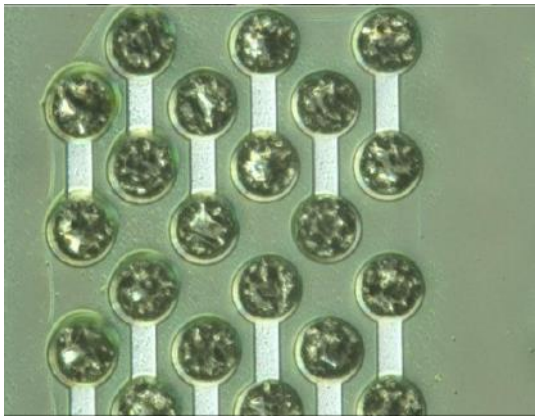
*Guilian Gao et, al, "Process Compatibility of Conventional and Low-Temperature Curable Organic Insulation Materials for 2.5D and 3D IC Packaging – A User's Perspective" , *Proc. ECTC 2014, p1810*

Flux Selection and Cleaning Considerations

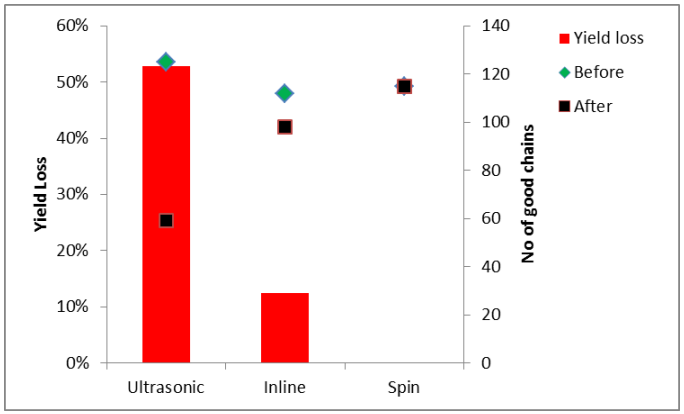
- High solid content rosin flux residue very hard to remove from the narrow gaps.
- Rosin-free low solid content no-clean flux residue easier to remove
- Ultrasonic cleaning caused high E-test yield lost
- Inline clean caused some yield loss
- Spin clean does not cause any yield loss



Rosin flux residue after cleaning



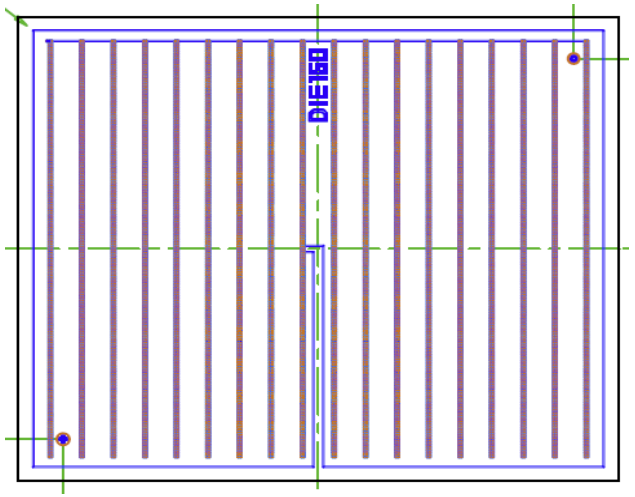
Rosin-free low solid flux residue before cleaning



E-test yield loss after flux cleaning using different methods

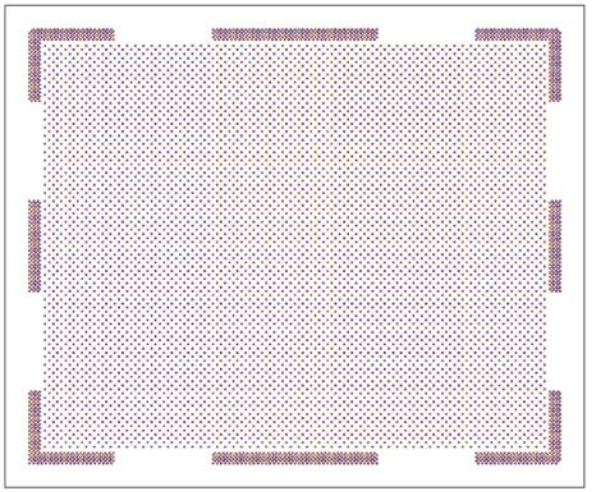
Good Design → Void-Free Underfill

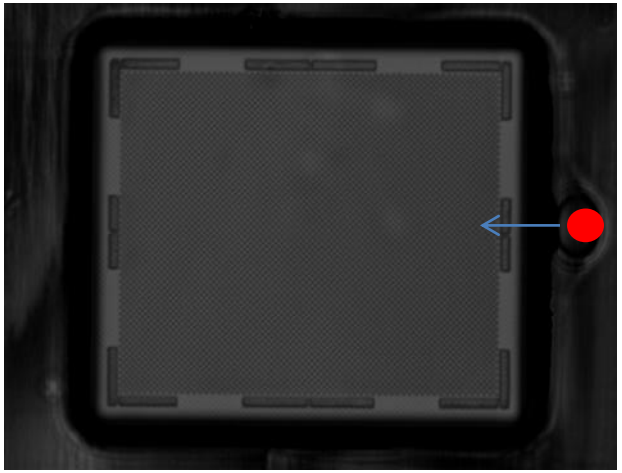
Large gaps between µbumps causes fast flow along the die edge → Underfill voids



Dispensing

Uniform µbump array in the center
Air escape channels along edge
→ Void-free underfill





Dispensing

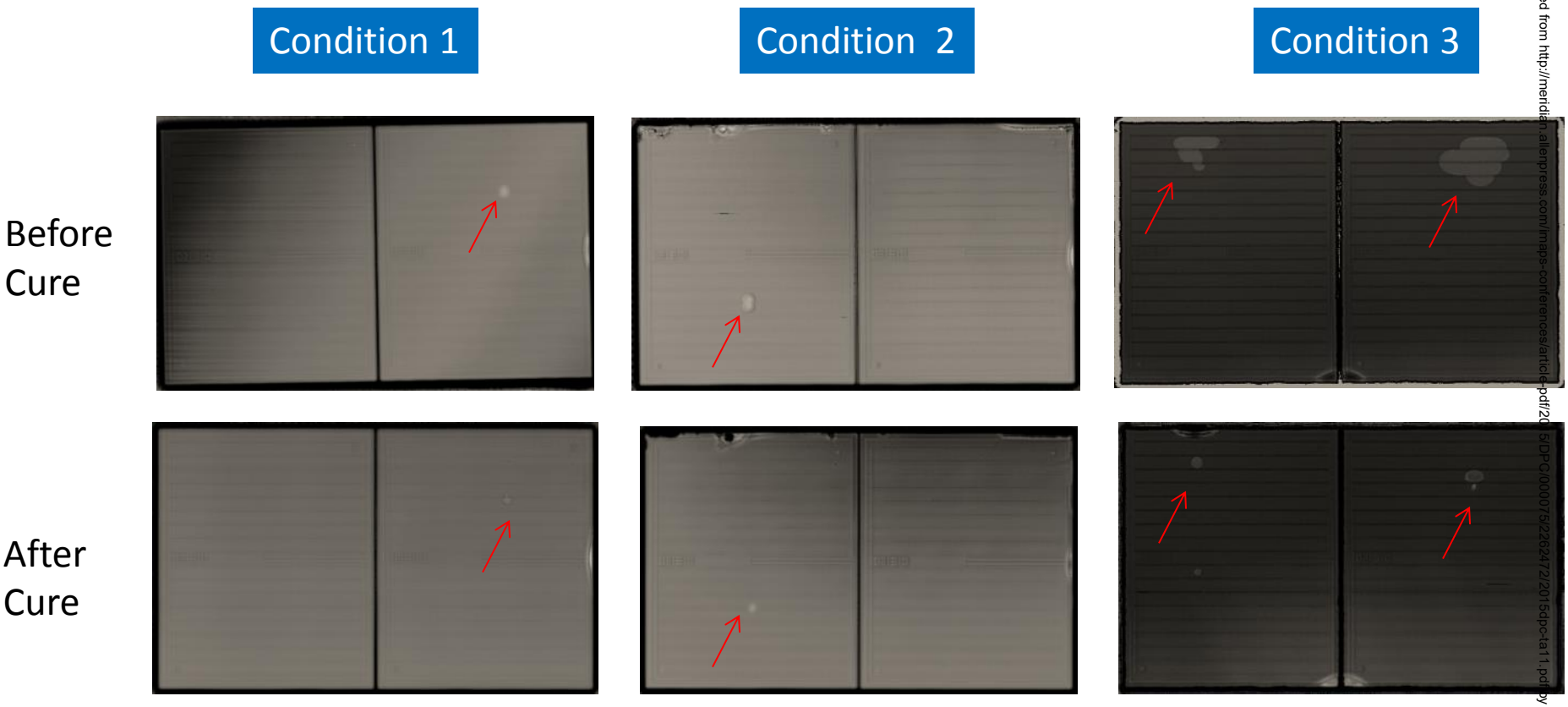
Curing in Vacuum Oven Enlarges Voids

Vacuum Oven, vacuum ON- entire cure cycle

Before Cure

After Cure

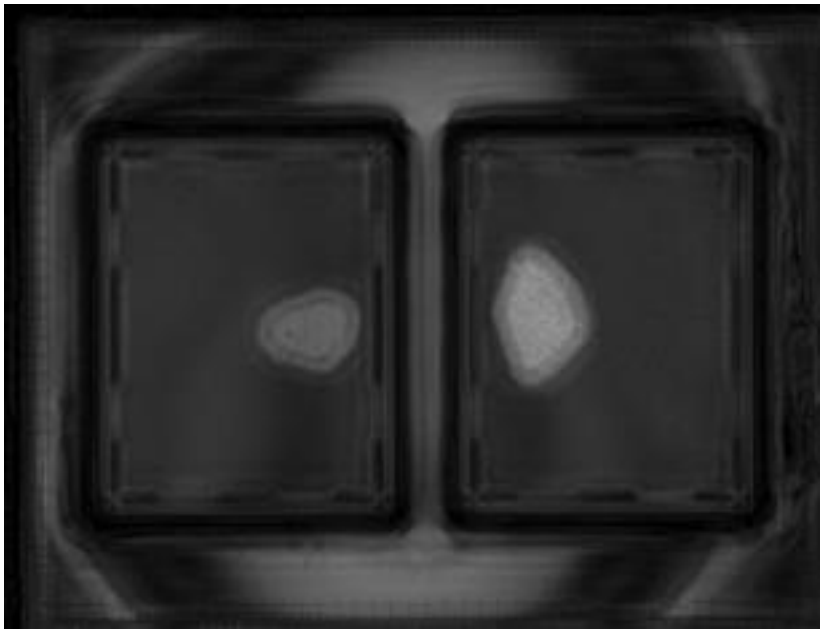
Vacuum Chamber Conditioning Prior To Cure Reduces Voids



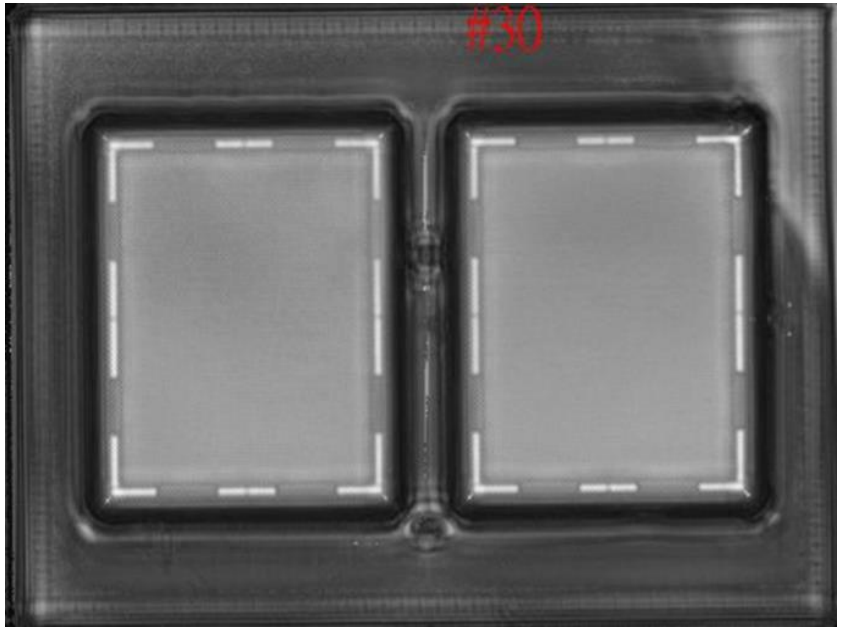
10 minutes pre-condition at 90°C and 2 torr of vacuum gives best results

Pulsed Pressure Cure Eliminates Voids

- Voids produced on purpose with a special dispensing pattern
- Curing in a pressure chamber
- A special pulsed pressure modulation profile was used for curing
- X-section of the cured sample showed no filler separation



Conventional oven cure

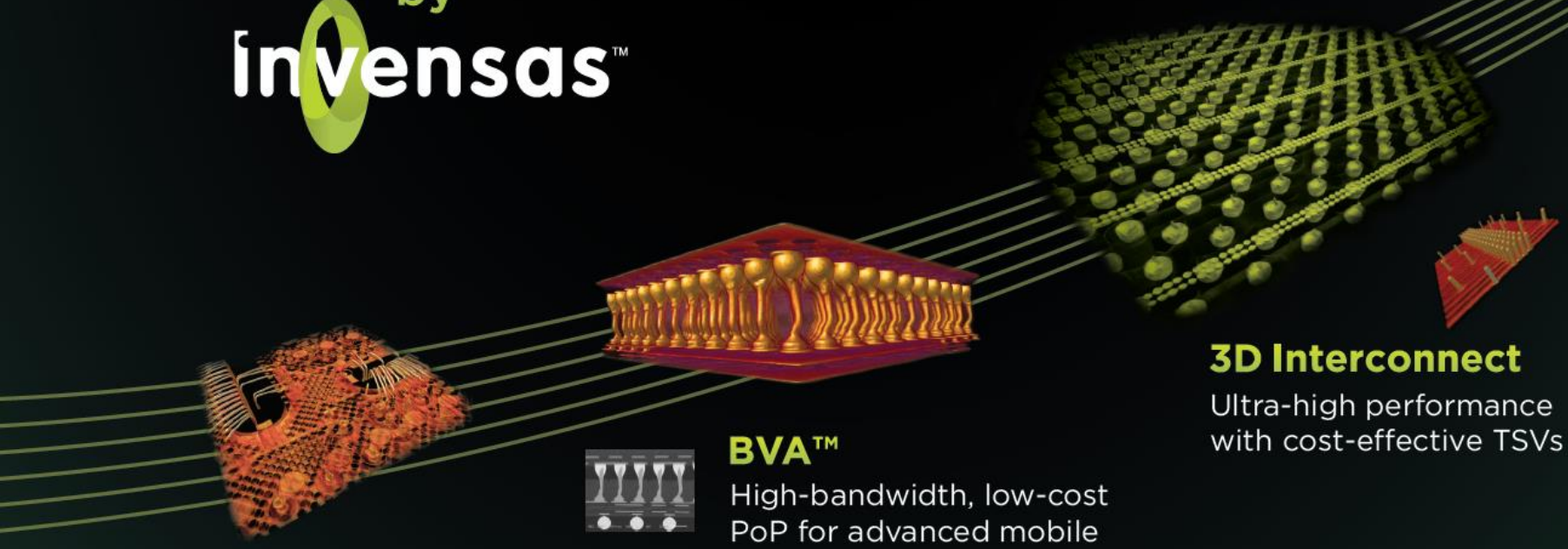


Pulsed pressure cure

Summary

- Choice of process flow strongly affects final yield
  - For chip to chip assembly flows, attaching µbump die to thin interposer is preferred for warpage management
  - For the chip to wafer assembly flow with Cu-Cu bonding, the thick handle wafers was very effective in keeping the part flat during assembly
  - A permanent carrier in a chip – wafer integration eliminates temporary bond/de-bond steps
- Microbump assembly window and pitch scalability considerations need to include:
  - Solder volume
  - Incoming height variations
  - Equipment capability and control
- Materials and process considerations
  - No-clean flux or fluxless process is preferred for fine pitch, low gap
  - Pulsed pressure curing of underfill is very effective in eliminating voids

Interconnectology by Invensas™



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