Flip Chip and Wafer Level Packaging Past, Present and Future

IMAPS Device Packaging Conference 2011

March, 2011

Presentation Goals

Understand the history of flip chip

and

Wafer Level Packaging

Presentation Goals

Apply this learning to TSV and other new packaging technologies

E&G's Rule of Technology Change

No One Uses a New Technology Unless They Have To

IBM Solid Logic Transistor (SLT)

- IBM SLT was the first flip chip device using bumps
  - Introduced in 1964 in the IBM 360 Model 40 computer
  - Glass passivation to eliminate need for hermetic package
  - Evaporated 90PbSn solder
  - Three Cu balls
    - To control standoff
    - 350µm pitch
  - Abrasively diced

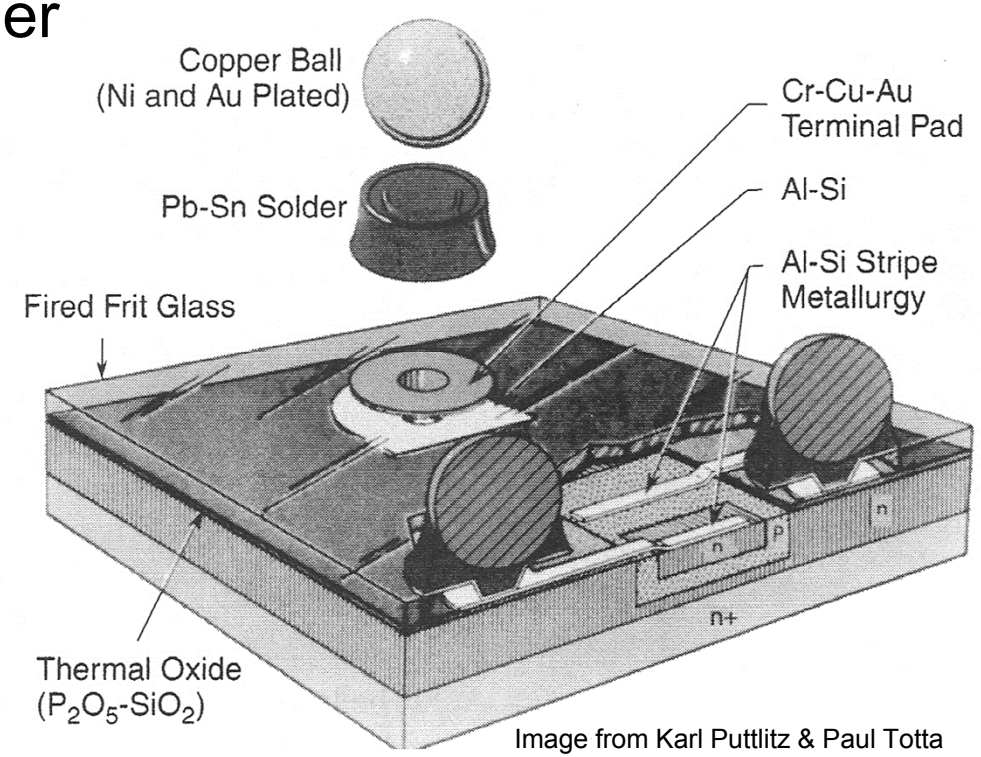
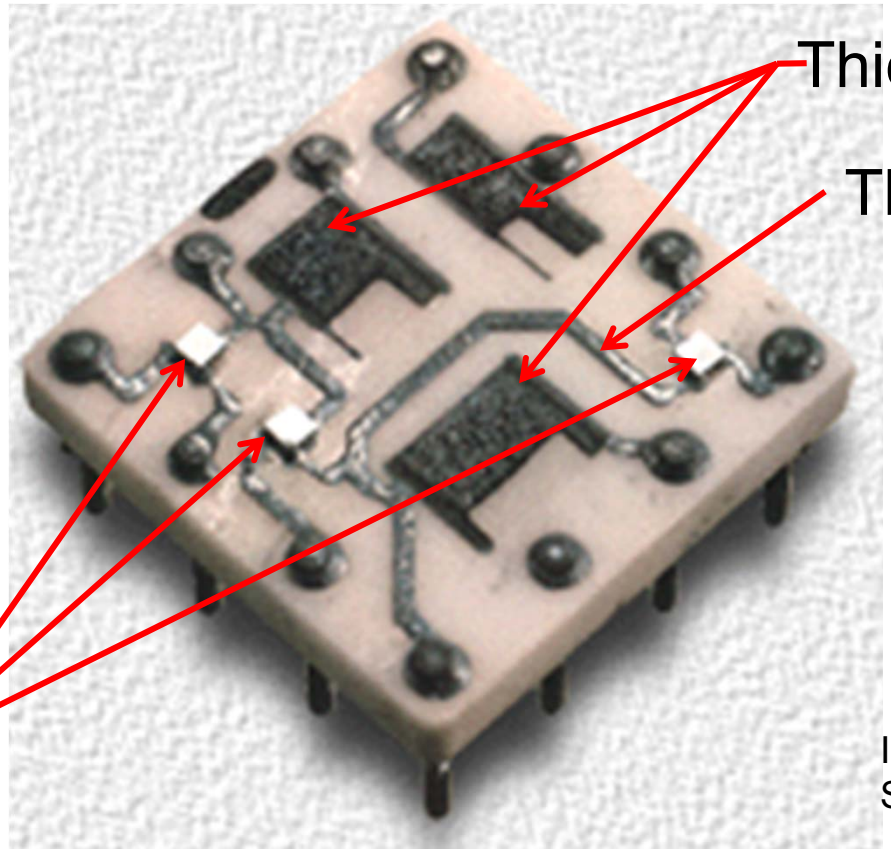


Image from Karl Puttlitz & Paul Totta
"Area Array Interconnection Handbook"

SLT Module (likely a flip-flop)

Ceramic PGA with Al cap and potted bottom side seal



Images courtesy of
Stanford University Infolab

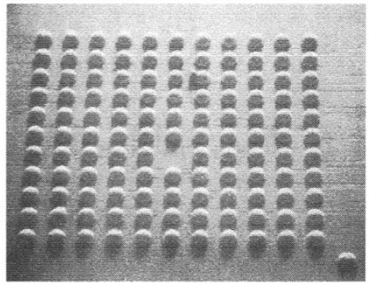
Why did IBM use FC for SLT?

- Many discrete transistors needed to make computer
  - ICs were not considered to be viable yet
  - Needed a low cost & reliable method to make computers
- Wire bonding was a manual process
  - No vision systems (human eye thru microscope)
  - No servo systems (positioning by human hand)
  - No auto looping (operator controlled)
- Wire bonds were not reliable enough
  - Thermocompression only
  - Purple plague, variable bond strengths

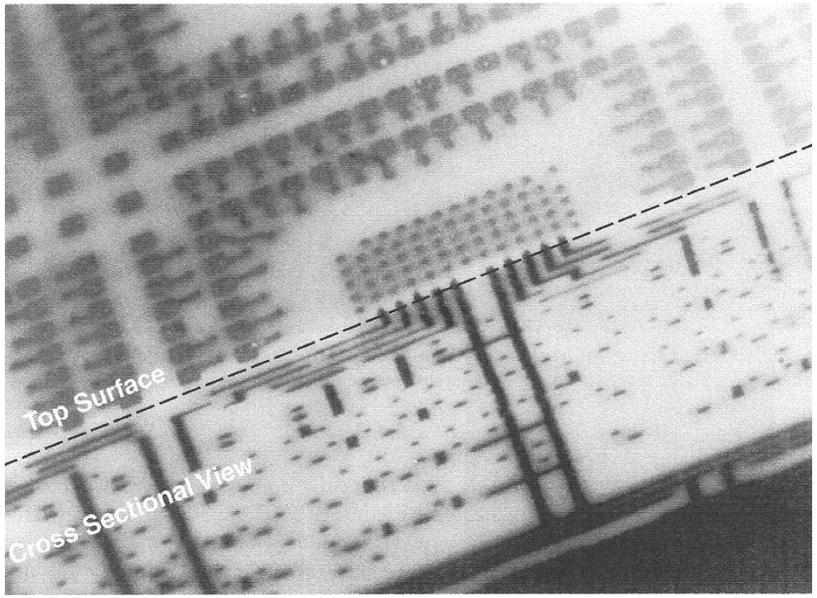
Flip Chip in the 1970s

- Delco began using flip chips for automotive
- IBM launches MST (Monolithic System Technology) - 1970
  - First flip chip IC, 3-4 circuits with 12 bumps on 300µm pitch
  - C4 (Controlled Collapse Chip Connection) solder bump
- Bump layout
  - Peripheral → Staggered Peripheral → Full Array
- Substrate technology to provide adequate wiring
  - Thin film on ceramic
  - Multi-layer thin film on ceramic
  - MLC (Multi-layer Ceramic) – 1979
    - Required to escape full array bump layouts

Flip Chip in the 1980s



- IBM used Bipolar Logic
  - Significantly faster than CMOS
  - Increasing requirement to interconnect multiple chips
- Development of IBM's MLC MCMs (Multi-chip Modules)
  - 9 chips → 36 chips → 121 chip TCMs (Thermal Conduction Modules)
  - 8 layers to 85 layers of MLC wiring
  - Glass ceramic MLC with TF layers
- 250µm → 225µm pitch
  - 121 bumps → 800+ bumps
- Hitachi electroplating
  - Paper published in 1981
  - Ti – Cu – Ni stack
  - Same basic structure as today



Images from Karl Puttlitz & Paul Totta
"Area Array Interconnection Handbook"

Key FC Enabling Technologies

- Underfill developed in 1984 by Hitachi
  - For flip chip on ceramic reliability improvement
- SLC (Surface Laminar Circuit) by Tsukada-san of IBM Japan
  - First high-volume build-up layer technology on organic
  - Development began in 1987, first products shipped in 1990
- Tsukada-san combines SLC and underfill
  - Initially for DCA then for FCIP
  - Development began in 1989, first DCA products shipped in 1992
- Commercial flip chip placement machines developed
  - Zevatech Micron 2 in ~1993
  - Universal GSM in ~1995

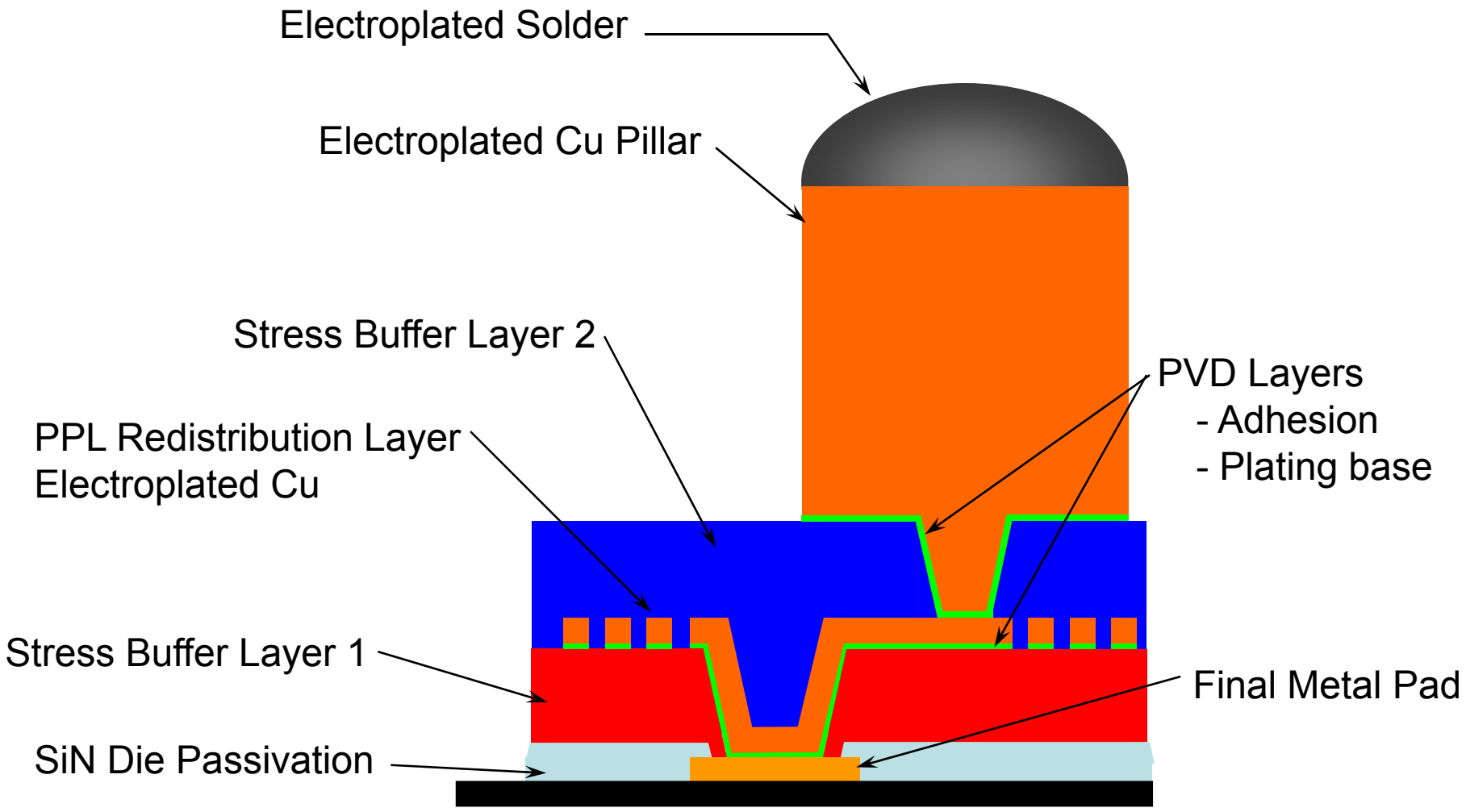
Flip Chip in the 1990s

- IBM switches from Bipolar to CMOS logic in 1992
  - Bipolar required ten TCMs to make a processor
  - CMOS enabled four processors on one TCM
- Flip chip expands beyond mainframes
- Viable bumping subcon infrastructure develops
  - Flip Chip Technologies formed in February 1996
    - Licenses ASE, SPIL, Amkor, National, and STATS from 1999-2002
  - Unitive spun out of MCNC in July 1996
- Intel microprocessor conversion in 1999
  - OLGA (Organic Land Grid Array) package
- Development of viable 63SnPb bumped flip chips

Why the Conversion to Flip Chips

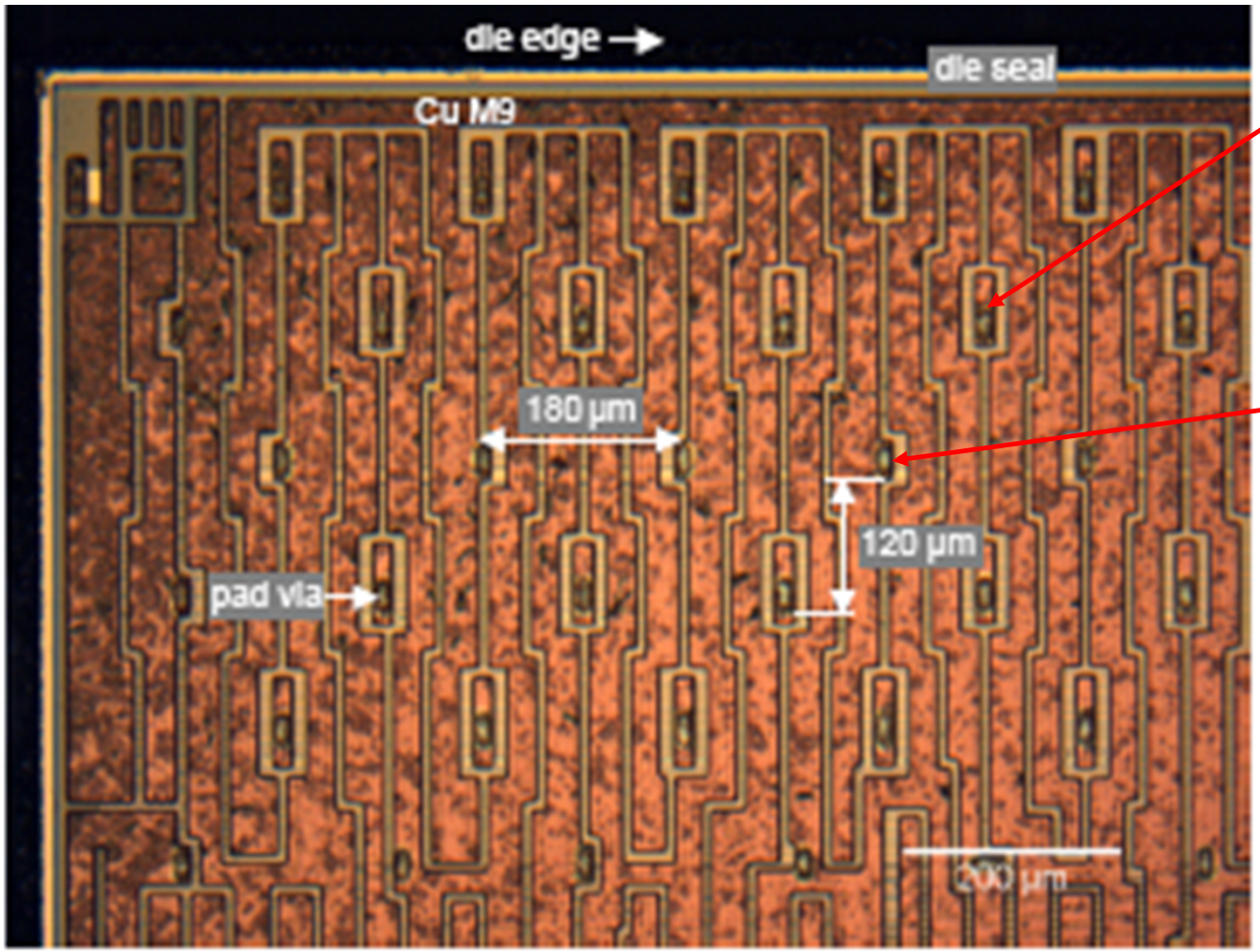
- Power & Ground Distribution
  - Primary driver for conversion in 1990s
  - Needed a low inductance delivery of 50-100+ amps to minimize SSN (Simultaneous Switching Noise)
  - Need to deliver correct voltage to center of ever larger chip sizes
  - Intel's current use of thick PPL (Post Passivation Layer) Cu
- I/O Count
  - ASICs and µPs were becoming I/O constrained
- High Speed serial I/O became a driver in early 2000s
  - Signal integrity due to very fast edge rates
  - DDR4 DRAM is next major conversion

Copper Pillar Bump on PPL RDL



Representative of Intel's 32nm structure

Westmere 32nm PPL RDL Wiring

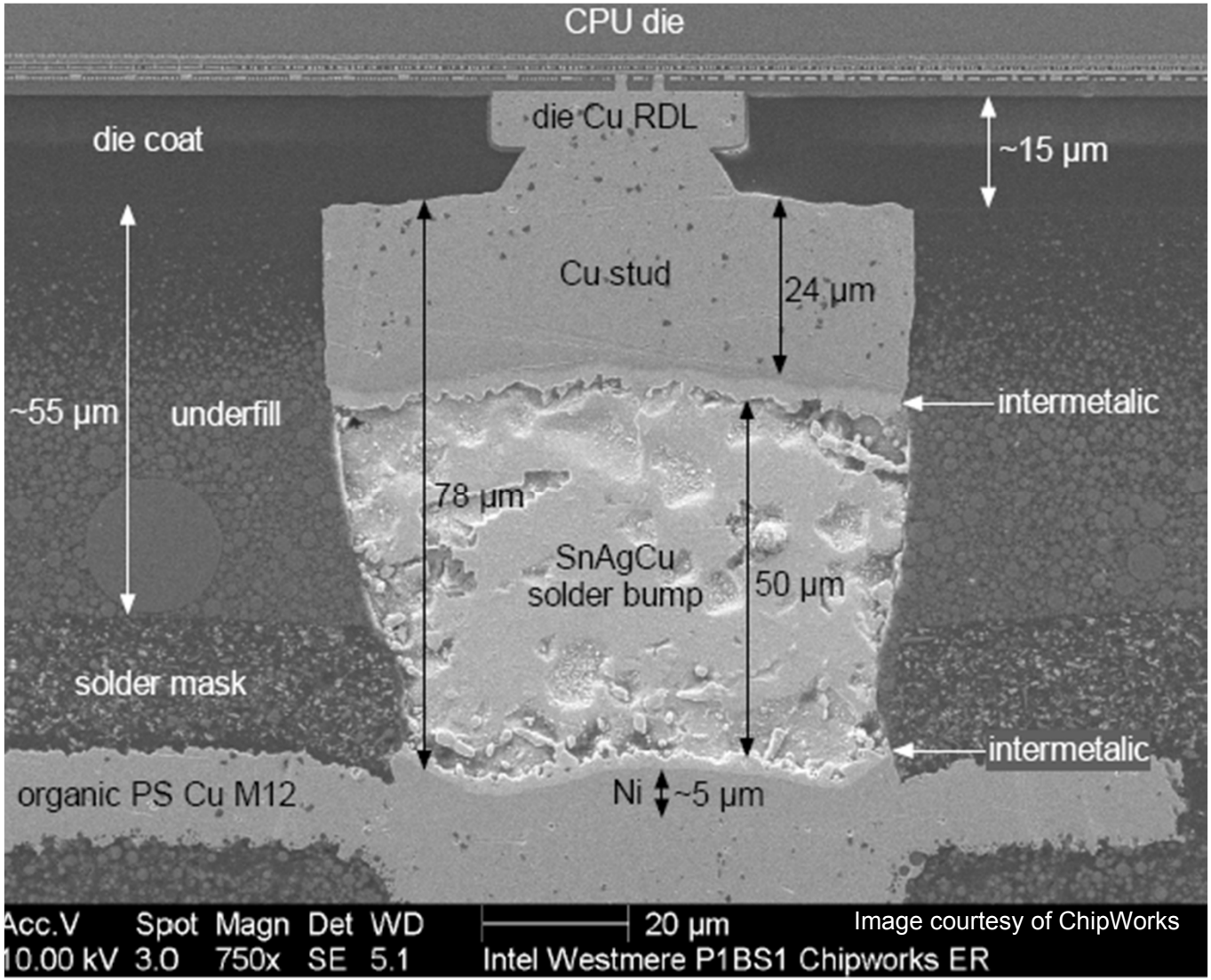


Isolated PPL Cu for I/O bumps

PPL RDL for power, ground, and clock
- Many vias to FM

Image courtesy of ChipWorks

Westmere 32nm CPU CPB Joint Structure



WLP Technology

1995 – 1996 Genesis of the FCT's WLP

- Flip Chip Technologies (now Flip Chip International)
  - 1995 business plan had 1.5 FCOB (Flip Chip on Board) devices per cell phone
- By 4Q 1996 it was clear that Nokia, Motorola & Ericsson were not going to underfill FCOB devices
- Remember in 1996:
  - Underfilling was slow and had long cure times
  - There was no underfilling of CSPs (Chip Scale Package)
  - The most significant CSP in the market was Tessera's MicroBGA

Invention of Modern WLP

- Original WLP concept was Mini BGA (mBGA) developed by Rajan Chanchani at Sandia National Labs in 1994
  - Used RDL (Redistribution Layer) & plated solder bumps
    - Resulted in large diameter bumps of low height
    - Required use of underfill for adequate reliability
- *Ultra*CSP™ development goals
  - RDL to redistribute peripheral wire bond pads to area array
  - Large solder balls, discretely placed to increase stand-off
    - Improves thermal cycle reliability
  - Compatible with SMT (Surface Mount Technology) infrastructure
- *Ultra*CSP was the first modern or viable WLP

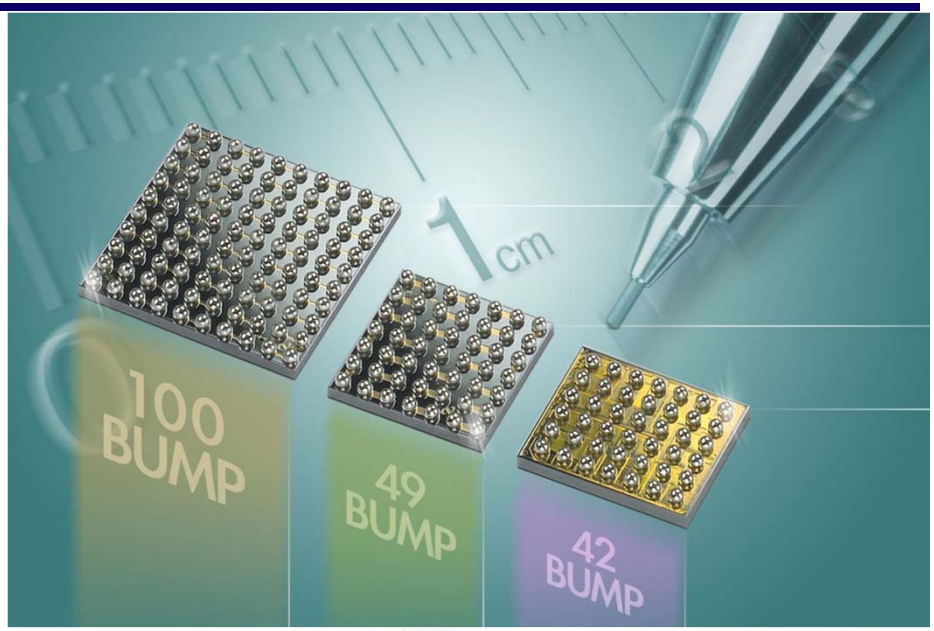
*Ultra*CSP is a trademark of Flip Chip International

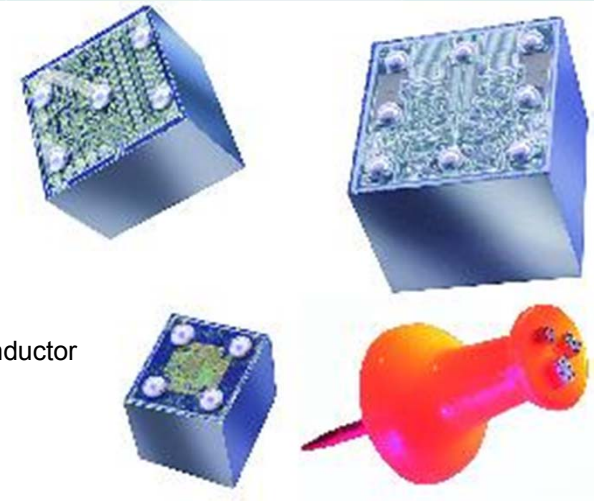
Market Focus on Cell Phones

- FCT worked closely with our customer's customers
  - Development programs with Nokia and Ericsson
    - Developed a good understanding of needs & requirements
    - Created the demand for WLP technology
  - Made *Ultra*CSP a de facto standard
    - Led to licensing of the technology to assure multiple sources
- Early *Ultra*CSP customers
  - Bourns with IPDs (Integrated Passive Devices)
  - Atmel with Serial EEPROMs
  - National Semiconductor with variety of analog parts
- By 2000 some cell phones had ten *Ultra*CSP packages

WLPs at National Semiconductor

- National's microSMD WLP
  - Introduced in 1998
  - In 2003 – 47 p/ns
  - Initially 4, 5 and 8 bumps
- In 2010
  - 630 p/ns as of June 2010
  - Wide variety of products
  - Micro SMDxt introduced in 2008
    - Available in up to 10 x 10 array
      - Largest product is 7 x 7
    - Introduced polymer core balls



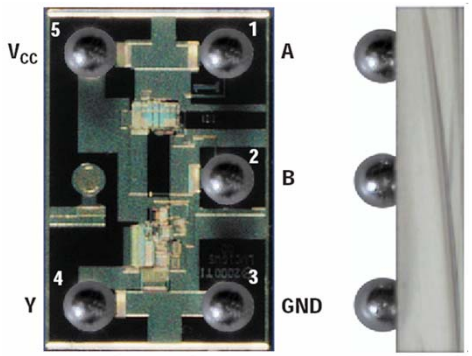


Source: National Semiconductor

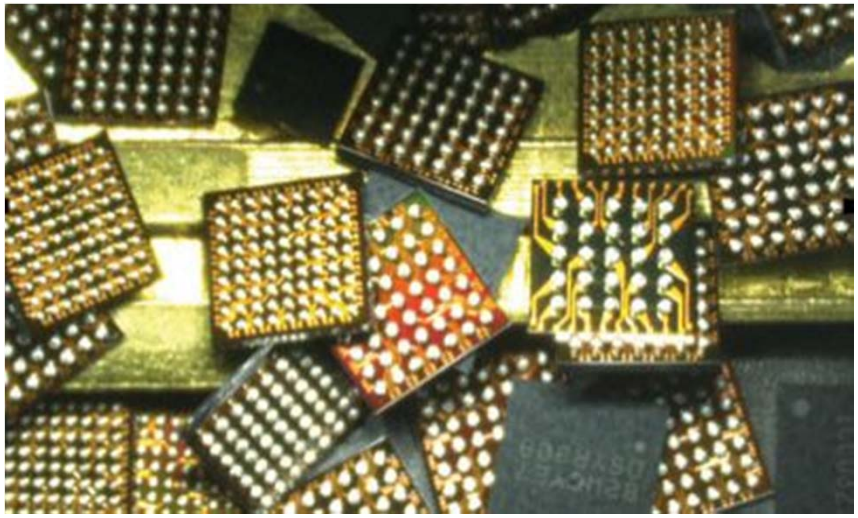
www.national.com/packaging/parts/MICROSMD.html
www.national.com/packaging/parts/MICROSMDXT.html

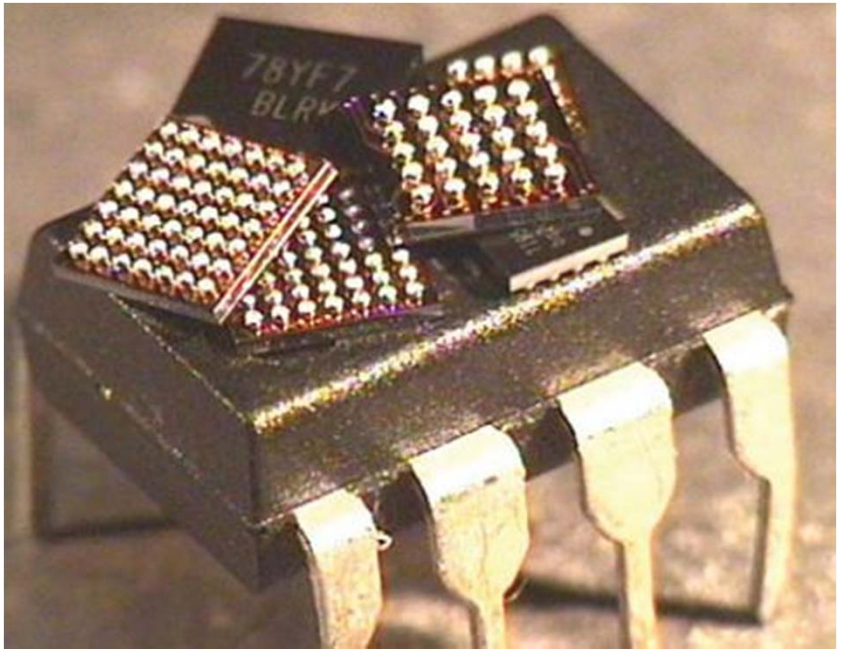
WLPs at Texas Instruments

- NanoStar - “Little Logic” family
  - Introduced in 2000 for standard logic gates
  - By 2003 >60 p/ns
  - Offered in 5, 6 and 8 bump packages
- In 2010
  - Largest array is 13 x 14 (depopulated)
  - Over 170 p/ns offered



Source: Texas Instruments





Recently Developed WLP Technologies

- FOWLP (Fan Out WLP)
  - Eliminates the constraint on need to fan-in all I/O
  - Infineon's eWLB (enhanced Wafer Level BGA)
  - Imbera's IMB (Integrated Module Board)
- Image Sensors
  - TSV based packages (i.e., Tessera, STMicro, Toshiba, & XinTec)
  - Glass based WLPs from OptoPAC
- WLP for MEMS

What Forces a Change in Technology?

A Requirement That Can Not be Solved with the Current Technology

Reality of Technology Adoption

- Current technology suppliers will resist change
  - Nature of human beings
  - Current job, role, fiefdom is at risk
  - Risk of current infrastructure obsolescence
- Current technology will be extended
  - Wire bonding improvements 1960's to present
  - Development of wire bonded stacked die
  - Fine pitch flip chip interconnects, Cu pillar bumps
- Change agent needed (i.e. product manager)
  - Career risk if new technology fails
  - Major career reward if successful

E&G's Rule of Technology Change

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Technology Change Drivers

- Flip Chip Adoption - Power & ground distribution
- WLP Adoption - Smaller & thinner mobile products
- TSV Adoption
  - Valid reason to adopt are memory I/O improvements
    - Wider buses
    - Lower power
    - Faster data transfer
  - Maybe in the future
    - Allowing mixed process technologies
    - Improving yield (i.e. cheaper)
    - Form factor

Conclusions

- Strong driver required for any new technology adoption
- Infrastructure takes time to develop
  - Materials
  - Tool and process development
  - Design tools
  - Qualification
    - Core technology qualifications
    - Internal product qualifications
    - Customer
  - Production capacity
- Incumbent technologies will always improve