High Temperature Reliability Investigations of EEPROM Memory Cells Realised in Silicon-on-Insulator (SOI) Technology

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Abstract

Microelectronic manufacturing progresses not only towards further miniaturisation, but also application fields tend to become more and more diverse. Recently there has been an increasing demand for electronic devices and circuits that function in harsh environments such as high temperatures. Under these conditions, reliability aspects are highly critical and testing remains a great challenge. A versatile CMOS process based on 200 mm thin film Silicon-on-Insulator (SOI) wafers is in production at Fraunhofer IMS. It features three layers of tungsten metallisation for optimum electromigration reliability, voltage independent capacitors, high resistance resistors and single-poly-EEPROM cells. Non-volatile memories such as EEPROMs are a key technology that enables flexible data storage, for example of calibration and measurement information. The reliability of these devices is especially crucial in high temperature applications since charge loss is drastically increased in this case. The behaviour of single-poly-EEPROM cells, produced in the process described before, was evaluated up to 450 °C. Data retention tests at temperatures ranging from 160 °C to 450 °C and write/erase cycling tests up to 400 °C were performed. The dependence of write/erase cycling on both temperature and tunnel oxide thickness was studied. These data provide an important foundation to extend the application of high temperature electronics to its maximum limits. The results show that EEPROM cells can be used for special applications even at temperatures higher than 250 °C.

Keywords: High temperature, SOI, EEPROM, Reliability, Data retention, Endurance

1. Introduction

High temperature electronics are demanded in a diverse range of applications: well logging, automotive and aviation count to the most important fields [1-3]. While for some uses, a technology withstanding 175 °C is sufficient, other fields require even higher temperatures [4]. In these cases, silicon-on-insulator (SOI) technology is needed, because common bulk-technology comes to its limits at these temperatures by reason of high leakage currents [5]. In addition, maintaining the functionality of EEPROMs at high temperatures remains a great challenge due to the high degree of oxide degradation. Data retention of non-volatile memory cells on bulk wafers at temperatures up to 360 °C has been studied before [6-8], and it has been shown that data loss at these temperatures is very fast. In this paper, we present reliability studies of EEPROM cells up to 450 °C realised in a SOI-CMOS process. The purpose is to analyse the behaviour at high temperatures and to investigate the temperature limit of use. For that, the two main aspects of EEPROM reliability are considered: on the one hand, the data retention characteristics and on the other hand, the endurance performance [9].

2. Theoretical aspects of EEPROMs

Programming and erasing of EEPROM cells is done by Fowler-Nordheim tunnelling [10]. For that, a high potential is applied to the control gate or to the drain, respectively, in order to increase or decrease the number of electrons on the floating gate. The case in which a high potential is applied to the control gate in order to charge the floating gate with electrons we call “erasing” of the cell, the opposite case (high potential to the drain) “programming” of the cell. The magnitude and the algebraic sign of the charge on the floating gate determine the threshold voltage shift ΔU_{th} according to Equation 1 [10]:

$$\Delta U_{th} = -\frac{Q_F}{C_G} \qquad \text{[Eq. 1]}$$

with Q_F being the charge on the floating gate and C_G the capacitance between the control gate and the floating gate. Consequently, the erased state has a higher threshold voltage than the neutral cell, the programmed state a lower one.

The reliability of EEPROM cells depends on the reliability of the used oxide and the creation of defects in the oxide. Two aspects are crucial for these memory cells: the retention of the data over time while no external voltage is applied and no data is written to the cell (data retention), and the maximum number of write / erase cycles (endurance).

Since the charge loss mechanism that limits the data retention is increased at higher temperature, typically accelerated data retention experiments are performed at elevated temperatures, usually 250 °C. The resulting data retention times are then extrapolated to the use temperature by an Arrhenius law as in Equation 2:

$$t = t_0 \cdot \exp\left(\frac{E_A}{k_B \cdot T}\right) \qquad \text{[Eq. 2]}$$

where t is the time to fail (normally defined as 10 % to 25 % change of the threshold voltage window), t_0 a constant, k_B the Boltzmann constant, T the temperature in the oven and E_A the activation energy.

As our intention is to use the EEPROMs at 250 °C or more, data retention tests were performed up to 450 °C in order to evaluate if accelerated data retention experiments at temperatures much higher than the use temperature of 250 °C are feasible. It was studied how fast data loss takes place at these high temperatures and in which way the result can be used for lifetime extrapolation.

The second reliability aspect, the endurance, depends on the tunnel oxide degradation, that occurs due to the application of voltage pulses during the programming and erasing of the cell. Pulsing causes defects in the oxide. The more often a pulse is applied, the more charges are collected by the defects and the threshold voltage window decreases until the two logic states are no longer distinguishable or the cell is destroyed. In this paper, endurance behaviour was investigated between 25 °C and 400 °C.

3. Experiments

Data retention and endurance were measured as a function of temperature on single-poly EEPROM cells realised in the SOI process mentioned above.

For the data retention experiments, a number of EEPROM cells were programmed and erased ten times to ensure that the threshold was stable. Half of the cells were left in the state “programmed”, the other half in the state “erased”. The wafers were then stored in an oven at six different temperatures: 160 °C, 250 °C, 300 °C, 350 °C, 400 °C and 450 °C After fixed time intervals, the cells were read out. The same experiment was repeated with cells cycled 10,000 times instead of ten times.

Programming / erasing as well as reading of the EEPROM cells was done at room temperature on a PA 200 wafer prober using a Labview program and a HP 4155 pulse generator together with the corresponding parameter analyser. The voltages used for programming, erasing and reading are summarized in Table 1.

Table 1. Voltages applied to the control gate (U_{CG}), the drain (U_D), the select gate (U_{SG}) and the source (U_S) during the programming, erasing and reading operations.

	U_{CG} [V]	U_D [V]	U_{SG} [V]	U_S [V]
Prog.	0	16	16	0
Erasing	16	0	16	0
Reading prog. cell	-5 to 2	0.1	5	0
Reading erased cell	1 to 8	0.1	5	0

Each pulse was 8 ms long. The threshold voltage was determined as the gate voltage at a drain current of 1 µA.

Endurance measurements at 25 °C, 100 °C, 175 °C and 250 °C were performed on the PA 200 prober at the wafer level, and at 250 °C, 300 °C, 350 °C and 400 °C in an oven on packaged EEPROMs.

4. Results and discussion

This section describes the results of the data retention and the endurance experiments.

Data retention

Figure 1 shows the values of the threshold voltages U_{th} as a function of storage time for the six bake temperatures plotted on a semi-logarithmic scale. The upper curves present the erased cells, the lower curves the programmed ones. Each cell was initially cycled ten times.

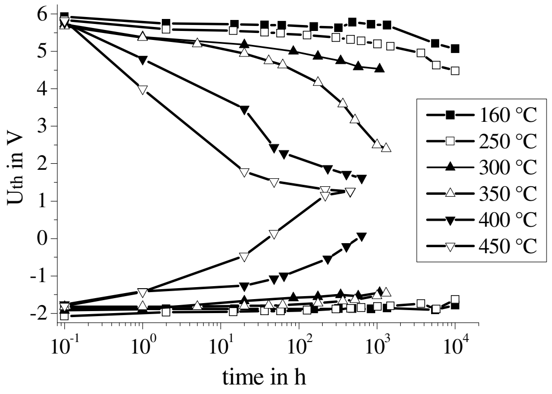

Fig. 1. Threshold voltage as a function of storage time for EEPROMs in an erased (upper curves) and programmed (lower curves) state; the cells were cycled ten times before storage; tunnel oxide thickness t_{ox} = 11.2 nm.

As is visible in the data profiles, the voltage shift increases with the bake temperature. While with a bake temperature of 250 °C, the threshold voltage window remains almost 7 V even after 10,000 h in the oven, the two logic states are no longer distinguishable after 250 h at 450 °C. Up to 350 °C, the upper threshold degrades much more than the lower threshold. At 400 °C, the lower threshold starts to degrade significantly. Furthermore, the shape of the curve changes with increasing temperature. While up to 300 °C the charge loss is remarkably small up to even more than 1,000 h, the 350 °C curve starts falling rapidly after circa 100 h, and for higher temperatures this rapid decrease occurs even earlier.

The results of the experiment with the cells cycled 10,000 times at room temperature prior to storage at high temperature are shown in Figure 2. The data for unstressed cells (Figure 1) and pre-stressed cells (Figure 2) are very similar. The measured threshold voltage differences induced through pre-cycling (10,000 cycles) are on the order of 100 mV. Altogether, the cycling before the storage in the oven did not visibly degrade the oxide in a way that defect induced leakage currents now cause worse data retention.

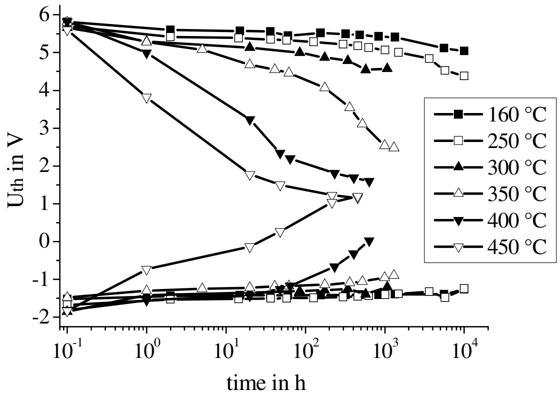

Fig. 2. Threshold voltage as a function of storage time for EEPROMs in an erased (upper curves) and programmed (lower curves) state; the cells were cycled 10,000 times before storage; tunnel oxide thickness t_{ox} = 11.2 nm.

As mentioned above, in many cases an Arrhenius law is assumed for data retention times as a function of temperature. In Figure 3, the data retention times for the different temperatures between 160°C and 450°C are plotted as ln ($t_{\text{retention}}$) vs. 1 / k_BT. The retention time was defined here as 15 % threshold voltage window reduction compared to the window at t = 1 h. The data in Figure 3 show an approximately linear relation between ln ($t_{\text{retention}}$) and 1 / k_BT with an activation energy of about 1.5 eV.

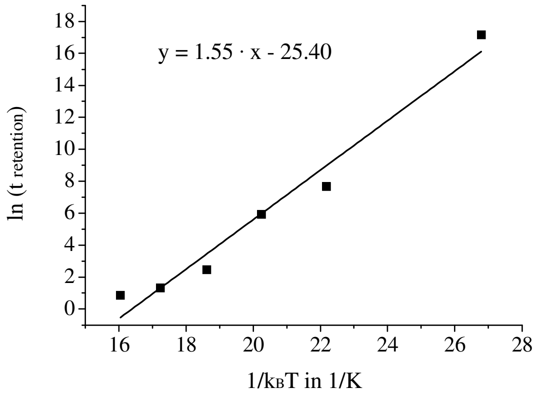

Fig. 3. Arrhenius plot corresponding to Figure 1: ln ($t_{retention}$) as a function of 1 / k_BT; the retention time is defined as 15 % threshold voltage window reduction compared to the window at t = 1 h.

Endurance

Figure 4 presents the results of the endurance tests on the wafer prober at temperatures of 25 °C, 100 °C, 175 °C and 250 °C. Figure 5 depicts the data for 250 °C, 300 °C, 350°C and 400 °C on packaged cells. The threshold voltage window narrows earlier at higher temperature due to increased tunnel oxide damage during high temperature cycling.

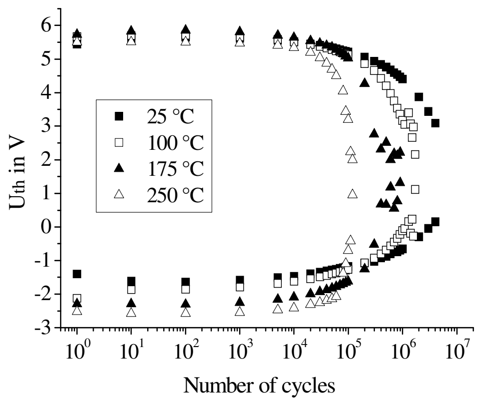

Fig. 4. Threshold voltage as a function of the number of cycles at different temperatures; tunnel oxide thickness t_{ox} = 11.7 nm.

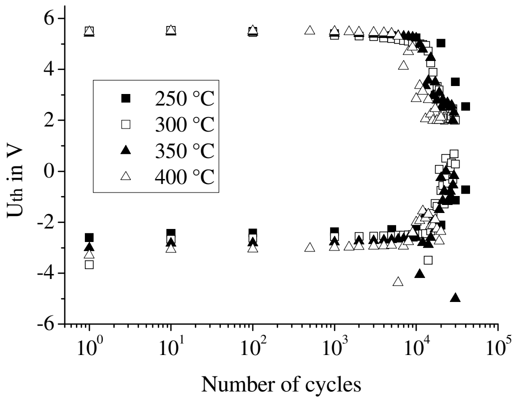

Fig. 5. Threshold voltage as a function of the number of cycles at different temperatures; tunnel oxide thickness t_{ox} = 11.7 nm.

In Figure 6, the degradation due to endurance cycling as a function of temperature is shown. The number of cycles where a 15 % reduction with respect to the initial threshold voltage window occurred is semi-logarithmically plotted as a function of temperature. The plot reveals that there is approximately an exponential relationship between endurance degradation and temperature with roughly a factor 5 reduction every 100 °C.

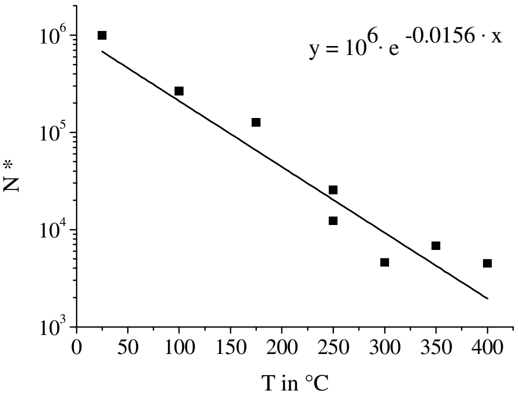

Fig. 6. Number of cycles N* (where a 15 % reduction of the threshold voltage window with respect to the initial window occurs) as a function of temperature corresponding to the data in Figures 4 and 5

Another aspect of endurance was studied by the investigation of the dependence on the tunnel oxide thickness. The results are presented in Figure 7. For smaller tunnel oxide thickness, the cells degrade faster than the cells with thicker tunnel oxide. Also the thicker tunnel oxide leads to a reduced charge transfer from and to the floating gate resulting in a smaller threshold voltage window.

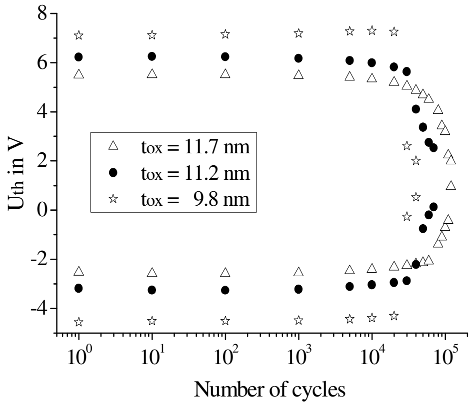

Fig. 7. Threshold voltage as a function of the number of cycles for EEPROMs with different tunnel oxide thicknesses; test temperature T = 250 °C

Figure 8 compares the I_D of U_G curves from the measurement of the upper threshold after ten cycles. The curves for the lower threshold are shifted to the left but otherwise similar and are therefore not shown here. The leakage current at 400 °C is some 10 nA, but the typical curve shape is still visible and the threshold measurable.

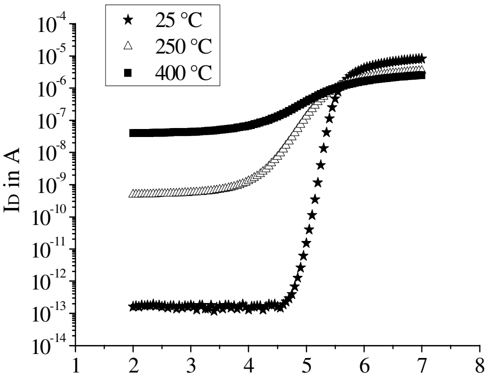

Fig. 8. Drain current I_D as a function of control gate voltage U_G of erased EEPROM cells after ten cycles at 25 °C, 250 °C and 400 °C; curves corresponding to the data in Figure 4 (25 °C and 250 °C) and Figure 5 (400 °C).

5. Conclusion

In conclusion, we can say that EEPROM operation is still possible at 400 °C. Write / erase cycling is possible more than 1,000 times at this temperature. Data retention measurement at 400 °C shows that a threshold voltage window of about 3 V is left after 100 h which might be enough for some applications. At 450 °C, the window is reduced to about 2 V after a storage time of 20 h. At 250 °C about 10,000 cycles are possible and data retention experiments show a threshold voltage window of about 7 V even after 10,000 h.

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