Au-Sn SLID bonding for high temperature applications

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Abstract

Au-Sn solid-liquid-interdiffusion (SLID) bonding is a novel and promising interconnect technology for high temperature (HT) applications. In combination with Silicon Carbide (SiC) devices, Au-Sn SLID has the potential of being a key technology for the next generation of innovative, cost effective and environmentally friendly drilling and well intervention systems for the oil industry. However, limited knowledge about Au-Sn SLID bonding for combined HT and high power applications is a major restriction to fully realize the high temperature potential of SiC devices. This paper presents a comprehensive study of fluxless Au-Sn SLID bonding.

Two different processing techniques – electroplating of Au / Sn layers and sandwiching of eutectic Au-Sn preform between electroplated Au layers – have been studied in a simplified metallization system. The latter process was further investigated in two different Cu / Si_3N_4 / Cu / NiP / Au-Sn / Ni / Ni_2Si / SiC systems (different Au-layer thickness). Die shear tests and cross-sections have been performed on "as bonded", thermally cycled and thermally aged samples to characterize the bonding properties associated with the different processing techniques, metallization schemes and environmental stress tests.

A uniform Au-rich bond interface is produced (the ζ phase with a melting point of 522 °C). The importance of excess Au on both substrate and chip side in the final bond is demonstrated. It is shown that Au-Sn SLID can absorb thermo-mechanical stresses induced by large CTE mismatches (up to 12 ppm/K) in a packaging system during HT thermal cycling. The bonding strength of Au-Sn SLID is shown to be superb, exceeding 78 MPa. Importantly, Au-Sn SLID is shown to be an excellent interconnect technology for HT packaging.

Keywords – High temperature, die attach, interconnect technology, Au-Sn SLID bonding.

Introduction

Microelectronic packaging plays a vital role in electronic devices, where it serves the purposes of electrical interconnection, heat dissipation, mechanical support and physical protection[1]. The electrical performance, size, cost and reliability is also to a large degree governed by the package, which is often referred to as the bottleneck of microsystem industry[2]. The choice of interconnection, i.e. the conductive path required to achieve connection from a circuit element to the rest of the circuit, is therefore of utmost importance.

Commonly used interconnect techniques include solders and conductive adhesives[3]. However, for high temperature (HT) applications like automotives, drilling and well intervention systems, aerospace, space exploration and nuclear environments, the standard interconnect materials do not meet the requirements regarding e.g. HT stability[4]. Currently, there is no clear definition of the temperature range of a HT electronic system. In this work it is considered to be above 200 °C.

There is a limited range of HT interconnect techniques[4-6]. One alternative is sintered nano-particle Ag, which has good electrical and thermal conductivity[7-8]. A nano-particle Ag joint has a high melting point (960 °C) compared to the low processing temperature (< 300 °C)[7]. However, Ag migration is reported to be a problem in HT applications (particularly in combination with high power), limiting the lifetime of the joint[9-10].

Other prospective HT interconnect techniques include liquid-based solder joints[11], composite solder joints[12], bismuth-based solder joints[13], and solid-liquid interdiffusion (SLID) joints[14-15]. Of these techniques, SLID bonding – also called Transient Liquid Phase (TLP) bonding[16-17],

isothermal solidification[18], or off-eutectic bonding[19] – has shown great potential[9, 19-21]. SLID bonding utilizes a binary system with one high temperature melting metal and one low temperature melting metal (general principles are shown if Fig. 1). The applied processing temperature is higher than the melting point of the low melting point metal, and new intermetallic compounds (IMCs) are formed. The solidification is isothermal, and the final joint have a higher melting point than the processing temperature. This opens a window for new subsequent manufacturing steps without the need for ever decreasing process temperatures for each step[14-15]. Another important advantage with SLID bonding is that often a processing temperature in close proximity to the final application temperature can be applied (since the melting point of the final joint is much higher than the processing temperature). This can help reduce the thermo-mechanical stresses induced by coefficient of thermal expansion (CTE) mismatches in the final package.

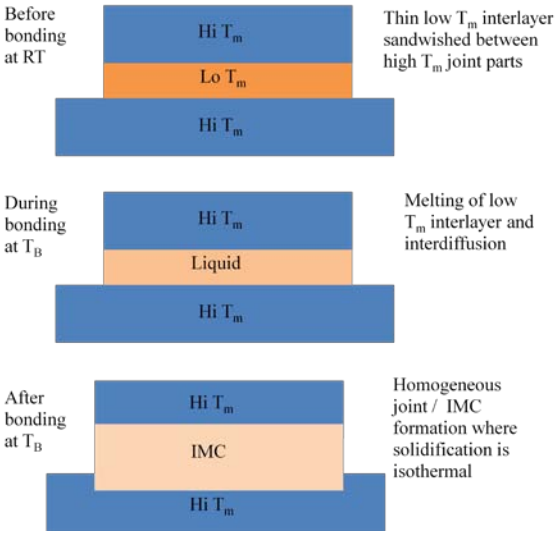

Figure 1: Schematic illustration of SLID bonding (T_B: Bonding temperature, T_m: Melting temperature).

SLID bonding has been performed in various metal systems. Examples include Ag/In[14-15], Ag/Sn[22], Au/In[14, 23], Au/Sn[6, 9, 19-21, 23-25], Cu/Sn[26-29] and Ni/Sn[28-29]. Ag/In, which is among the first SLID systems[14-15], has been investigated for HT applications in several studies[9, 30-32]. Here, a HT stable joint can be achieved (stable up to 700 °C[30]) using a processing temperature of only 210 °C, followed by annealing at 150 °C[32]. However, the HT lifetime of the joint is reported to be limited (especially in combination with high power), due to Ag migration[9-10].

Au/Sn is a promising SLID system for HT applications[9, 19-21]. Based on the Au-Sn phase diagram (shown in Fig. 2), several Au-Sn phases can be appropriate for HT applications. However, when long time stability is taken into account, the ζ phase is the most promising. The final bond structure is reported to be layered[21] – Au / ζ' / Au – where the ζ' phase undergoes a phase transition to the ζ phase at 190 °C[33-34]. The ζ phase has a melting point of 522 °C[33-34], making it desirable for HT applications. Thorough investigations of the Au-Sn phase diagram suggests that the actual layered bond structure probably is Au / ζ / Au, since the ζ phase is stable down to -5° C (depending on Au concentration). Au/Sn SLID has already shown good HT stability and thermal cycling abilities in studies performed by Johnson *et al*[9, 19].

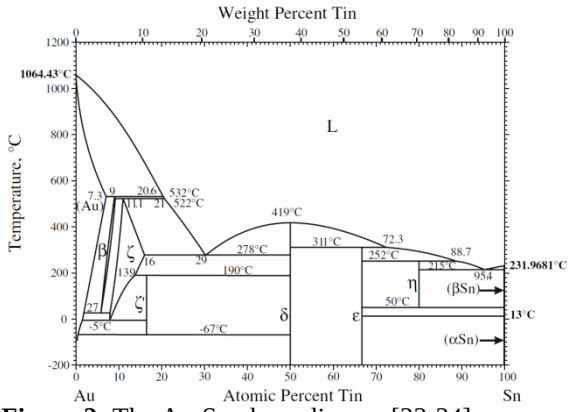

Figure 2: The Au-Sn phase diagram[33-34].

This work is part of the High Temperature Power Electronics Packaging (HTPEP) project, where one objective is to develop reliable packaging technology for SiC devices operating in harsh environment[35]. SiC, a wide bandgap semiconductor, is commonly considered as the best alternative for the next generation of innovative, high performance, cost effective and environmental friendly drilling and well intervention systems for the oil industry[35]. SiC has a high breakdown field strength, a high thermal conductivity, and offers excellent performance in high temperature (up to 600 °C) and high power applications[36-38]. However, lack of qualified HT packaging technology is a major limitation to fully realize the potential of SiC.

This paper presents a study of Au-Sn SLID bonding in a package utilizing a bipolar junction transistor (BJT) SiC chip. First, two different processing techniques – electroplating of Au / Sn layers and sandwiching of eutectic Au-Sn preform between electroplated Au layers – are investigated in a simplified metallization system to find the best technique. The latter process is further investigated

for metallized Si_3N_4 substrates, in two different Cu / Si_3N_4 / Cu / NiP / Au-Sn / Ni / Ni_2Si / SiC systems (different Au-layer thickness). Die shear tests and cross-sections are performed on the different samples to characterize the bonding properties associated with the different processing techniques, metallization schemes and environmental stress tests.

Experimental

Test Assemblies

SLID 1 a & b samples

Oxidized Si wafers with sputtered TiW (60 nm) / Au (100 nm) adhesion / seed layers were used as both substrate (diced in 4.3 * 6.6 mm^2 after plating) and chip (diced in 2 * 2 mm^2 after plating) in the simplified bonding samples, hereby referred to as SLID 1 samples. These were then electroplated with a uniform Au layer (5 µm). The Au electroplating was performed in a gold cyanide solution at a temperature range of 60-65 °C, with a current density of 5.4 mA/cm^2. Two different types of SLID 1 samples were manufactured:

- SLID 1a: Sn (2 µm) / Au (0.1 µm) layers were electroplated on the chip side using a tin sulphate solution at room temperature, with a current density of 10 mA/cm^2. The thin Au layer is applied to minimize oxidation, making fluxless bonding possible[24]. A Sn / Au plated chip was then bonded to a substrate (see Fig. 3 for illustration).
- SLID 1b: An eutectic Au80wt.%Sn20wt.% preform (7.5 µm) was sandwiched between a chip and substrate to make the joint. The preform was purchased from Micro Joining KB (see Fig. 4 for illustration).

The bonding was performed in two steps; first, a flip chip bonder was used to pick and place at a moderate temperature (120 °C) applying a force of 35 N for 30 sec. Secondly, the positioned samples were bonded using a hotplate in a vacuum chamber and a clamping force to ensure intimate contact. The bonding profile is shown in Fig. 5. First, the samples were heated to 250 °C and held there for 5 min (to bake out any residual moisture and to assure a uniform temperature distribution in the bonding layers). Then, the samples were heated to 350 °C, and kept there for 20 min to ensure that the desired phases were created.

SLID 2 a & b samples

Commercialy purchased Si_3N_4 substrates (from Denka Chemicals) with active metal bonded (AMB) Cu (150 µm) and plated Ni:P (7wt%P) were used as substrates for both SLID 2a & b samples. The substrates had symmetrical metallization (Cu / Ni:P layers on both top and backside) to minimize warpage of the substrate due to CTE mismatches between Si_3N_4 and Cu. An additional Au layer (3 µm or 5 µm) was electroplated on the substrates in a gold cyanide solution at a temperature range of 60-65 °C, with a current density of 2.7 mA/cm^2. The substrate was diced in 6 * 6 mm^2 samples after plating.

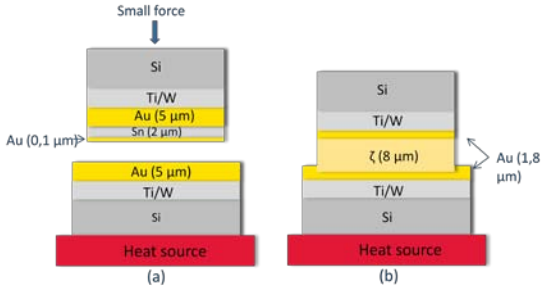

Figure 3: SLID 1a samples: a): Layers as plated. b): Expected structure after bonding.

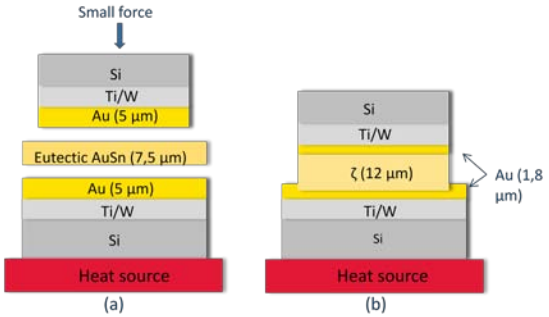

Figure 4: SLID 1b samples: a): Layers as plated. b): Expected structure after bonding.

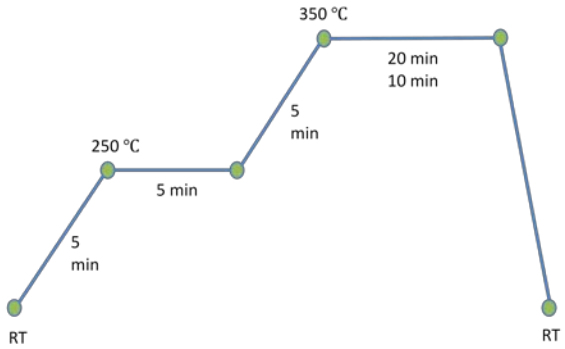

Figure 5: Bonding temperature profile.

The BJT SiC dummy chips, delivered from TranSiC, had sputtered Ni_2Si (140 nm) / Ni (300 nm) / Au (100 nm) metallization. The chips were electroplated with a uniform Au layer (5 µm), and diced in 1.855 * 3.4 mm^2 samples.

Two different types of SLID 2 samples were produced:

- SLID 2a: As for SLID 1b samples, an eutectic Au80wt.%Sn20wt.% preform (7.5 µm) was sandwiched between the chip and the substrate to make the joint. For SLID 2a samples, the electroplated Au layer on the substrate was only 3 µm. This means that there would be no excess Au left on the substrate side of the joint (see Fig. 6 a for illustration).
- SLID 2b: Same as SLID 2a samples, but with 5 µm electroplated Au on both sides, resulting in excess Au on both the substrate and the chip side in the final joint (see Fig. 6 b for illustration).

The bonding was performed in two steps; first, the substrate, preform and chip were aligned manually on a hot plate and fastened with a clamping force (see Fig. 7). Secondly, the samples were bonded using the hotplate in a vacuum chamber. The same bonding profile as for SLID 1 samples were used, However, the final bonding time was reduced from 20 min to 10 min based on work published in ref. 20.

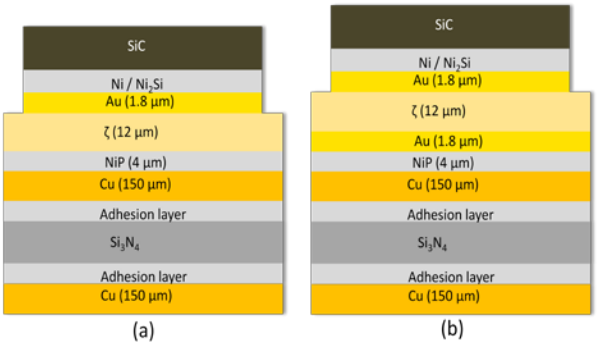

Figure 6: SLID 2 a&b samples: Sketch of expected layer structure after bonding. a): SLID 2a. b): SLID 2b.

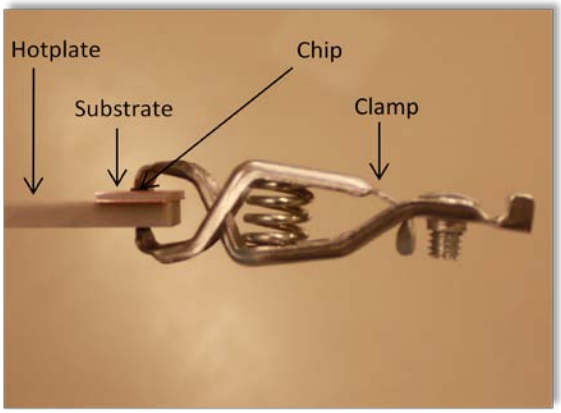

Figure 7: Picture of manually aligned SLID 2 a&b samples on a hot plate fastened with a clamping force.

Test Methods and Equipment

Thermal cycling tests were peformed in a Heraeus HT 7012S2 thermal cycling chamber. Both SLID 1 a&b and SLID 2 a&b samples were cycled between 0 – 200 °C, with a gradient of 10 °C/min, and a dwell time of 15 min at temperature extremes (see Fig. 8 for cycling profile – the temperature in the joint was measured by a k-type thermocouple and an Agilent 34970A data acquisition unit). Two levels of cycling were performed (500 and 1000 cycles). The cycled samples were shear tested in a Dage 2400A shear tester with a 50 kgf load cartridge, and the results were compared to measurements on "as bonded" samples.

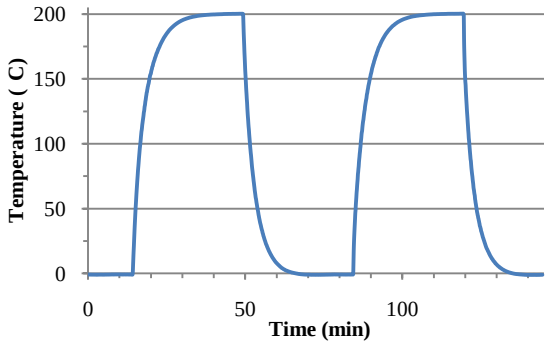

Figure 8: Cycling profile for thermal cycling. The temperature in the joint was measured by a k-type thermocouple and an Agilent 34970A data acquisition unit.

SLID 1 a&b samples were aged in air at 250 °C for 6 months in a Binder laboratory oven. Also the aged samples were shear tested in a Dage 2400A shear tester with a 50 kgf load cartridge, and compared to measurements on as bonded samples.

Cross-sectioning was performed on all groups of samples. The samples to be cross-sectioned were embedded in epoxy resin prior to grinding, and then grinded (on SiC paper grade 320 through 4000, using water cooling) and polished (using 6 µm diamond particles and an alcohol based lubricant prior to fine polishing using 3 µm and 1 µm diamond particles with a water and oil based lubricant). Note that SiC is a very hard material compared to the Au and the Au-Sn phases, making it difficult to prepare planar cross-sections.

The cross-sectioned samples were investigated by optical microscopy (Neophot 32), scanning electron microscopy (SEM – JEOL JSM-5900LV) and energy-dispersive spectroscopy (EDS – Oxford X-MAX 50).

Results and Discussion

Thermal Cycling Test

SLID 1 a & b samples

After 500 and 1000 thermal cycles, the die shear strength was determined and compared to the as bonded strenght. Five samples from each group were tested. The results have some clear trends (shown in Fig. 9):

Variations

- There are large variations (standard deviation) in the shear strength. The reason for this most likely originate from the sample manufacturing. A clamp force was used to ensure sufficient contact between the bonding surfaces (see Fig. 7). The clamp force is only in contact with a restricted part of the surface area of the chip and the substrate. During the bonding process, parts of the bonding materials will be liquified, meaning that if the clamp force is not symmetrically placed on the chip/substrate, problems with co-planarity will occur. This was confirmed by cross-section pictures (see Fig. 10).

Die shear strength

- The shear strength has a substantial increase after 500 cycles. The shear strength after 1000 cycles also increased compared to the as bonded samples, but it had decreased compared to the strength after 500 cycles. The explanation for the relative increase in shear strenght probably stem from the challenges associated with co-planarization. During thermal cycling the samples are regulary heated and kept at 200 °C, increasing the diffusion rate between the bonding partners, i.e. making a stronger joint. The reduction in the shear strength after 1000 cycles compared to 500 cycles indicates that there is a reduction in fatigue lifetime during thermal cycling. However, due to the limited amount of samples, and the large standard deviation, this should be further investigated.

SLID 1a vs 1b

- The SLID 1b samples has higher die shear strenght than the SLID 1a samples after thermal cycling. There are no obvious reason for this trend, but careful investigations of the cross-sections of 1a and 1b samples reavealed that there was a through crack in all SLID 1a samples (see Fig. 11). There were no cracks in the SLID 1b samples, so the through crack in the 1a samples probably explains the lower strength. The cracks that are located at the interface between the electroplated Au and Sn layers on the chip side, probably originate from contaminatons during Sn plating (e.g. on the Au surface, not pure enough Sn, etc.). In 1993 Hiber *et al.* experienced problems regarding the pureness of the electroplated Sn in a CuSn SLID joint. They reported that only e-beam evaporated Sn is pure enough for CuSn SLID bonding[39]. This shows the importance of the Sn quality. However, strong and uniform CuSn SLID joints have also been produced using electroplated Sn[26].

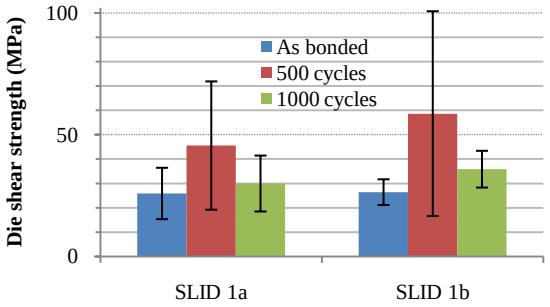

Figure 9: Die shear strength of SLID 1 a&b samples as a function of thermal cycles (0 – 200 °C, 10 °C/min, dwell time of 15 min). The bars show the standard deviation for the different groups.

Bonding structure

- The bond interface of the the “good” samples (without co-planarity problems) was uniform with regard to IMC formation. Fig. 12 shows a SEM image of the cross-section of a SLID 1b sample. EDS was used to identify the bonding phase as most probably the ζ phase, This supports our assumption, that a AuSn SLID bond most probably has a Au / ζ / Au structure.

Fracture surfaces

- The fracture surfaces of samples with high bond strength were located at the interfaces between the substrate/chip and Ti/W. The fracture surfaces of samples with low bond strength was located in the actual bond layer. This indicates that the samples with low die shear strength fails because of co-planarization issues. However, the samples with high die shear strength fails in the chip/substrate metallization, indicating that a good AuSn SLID bond has higher bond strength than 80 MPa (the highest measured bond strength). This is also supported by previous work by Johnson *et al.*, who has reported a die shear strenght above 90 MPa[19] for AuSn SLID joints.

EDS analysis indicates that a AuSn SLID bond is constructed of a layered Au / ζ / Au structure. When

the joining is well performed, high bond strengths is achieved. Importantly, a AuSn SLID joint can withstand thermal cycling between 0 – 200 °C in a package with small CTE mismatches (Si chip and substrate).

Figure 10: Optical microscopy image of a cross-section of an as bonded SLID 1b sample showing the challenges associated with co-planarity during bonding.

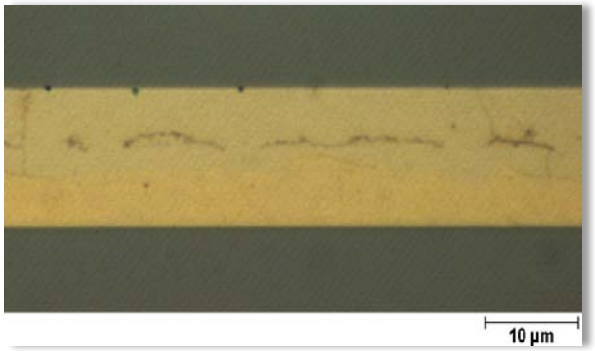

Figure 11: Optical microscopy image of a cross-section of a SLID 1a sample showing the through crack in the electroplated Au / Sn interface.

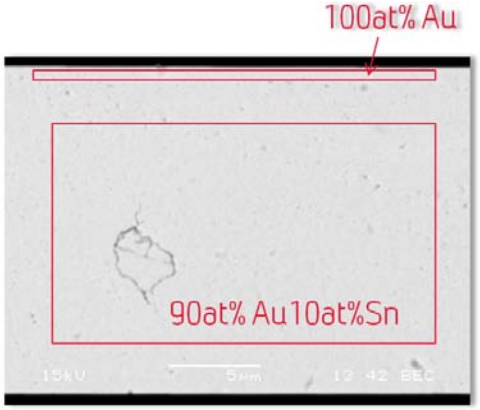

Figure 12: SEM image of a SLID 1b sample. The red rectangles show regions were EDS has been performed. The atomic percent for the regions is included.

SLID 2 a & b samples

After 500 and 1000 thermal cycles, the die shear strength was determined and compared to the as bonded strenght. Ten SLID 2b samples and five 2a samples were tested. The results have some clear trends (shown in Fig. 13, Table 1 and 2):

- The variations (standard deviation) in the shear strength was greatly reduced compared to SLID 1 a&b samples. The assembly was performed as for SLID 1 a&b samples, but experience assured a higher yield. Note that the majority of the samples had a bond strength above the equipment limit (50 kgf), indicating that there could be a considerable variation not measureable with the applied equipment.
- The bond strength of SLID 2b samples remained relatively unchanged and superb (> 78 MPa) during thermal cycling (note that the majority of the samples had a bond strength above the equipment limit, indicating that there could be a degradation in the bond strength not measureable with the applied equipment). For SLID 2a samples there was a decrease in the bond strength as a function of the number of thermal cycles. In SLID 2b samples there was excess Au on both the substrate and the chip side (see Fig. 14). In SLID 2a samples there was no excess Au left on the substrate side (see Fig. 15)), causing formation of brittle Au-Ni-Sn IMCs during thermal cycling. These brittle IMCs are believed to be the primary cause of the degradation of the bond strength.
- As for SLID 2 a&b samples, the bond interface was uniform with regard to IMC formation, EDS was used to identify the bonding phase as most probably the ζ phase.
- The fracture surfaces of 2b samples were located at the chip / Ni_2Si / Ni interfaces, again indicating that a good AuSn SLID bond has higher bond strength than 78 MPa. The fracture surfaces of 2a samples were located at the ζ phase / Au-Ni-Sn IMCs interfaces, confirming that these brittle IMCs are the primary cause of the degradation of the bond strength for 2a samples.

Notably, the AuSn SLID joints withstand thermal cycling between 0 – 200 °C for a package with large CTE mismatches (12 ppm/K difference between SiC and the thick Cu film). The importance of excess Au on both substrate and chip side in the final bond is also demonstrated. The “soft” Au layer is important since it absorbs thermo-mechanically stresses in the package, induced by e.g. CTE mismatches between the chip and the conducting layer. Excess Au on both

sides of the final joint is also important since it acts as a diffusion barrier between the Au-Sn phases and the chip/substrate metallization, which tends to compose brittle IMCs like Ni_3Sn_4[40], greatly reducing the lifetime and the reliability of the package. Furthermore, excess Au is central for the prediction of the properties of the joint, since it assure stable material phases with predictable/known properties.

The superb die shear strength of a AuSn SLID joint shows that this is one of the most promising SLID bonding material schemes for HT applications. In addition, taking into consideration a AuSn SLID joints ability to absorb stress, makes it very attractive. However, for applications with temperatures above 0.5 x homologous temperature (T_H), creep is considered to be important for the long time reliability[2]. T_H is defined as T^*/T_M K (where T^* is the operating temperature, and T_M is the melting point) in absolute temperature. For a ζ phase bond, a T_H of 0.5 only gives a T^* of 125 °C, making it vulnerable for creep during long time HT applications with constant stresses in the system (e.g. from CTE mismatches). But, by e.g. applying a process temperature in close range to the operation temperature (which often is possible for SLID bonds, since the melting point of the final joint is well above the processing temperature), stresses induced by the CTE mismatches in the system can be minimized. The effect of creep in a Au-Sn SLID joint should be more carefully investigated.

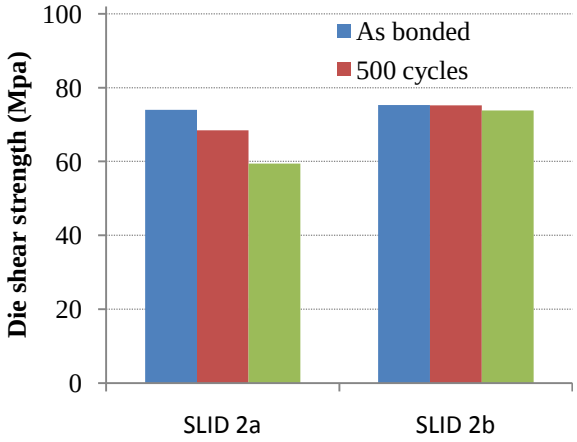

Figure 13: Die shear strength of SLID 2 a&b samples as a function of no of thermal cycles (0 – 200 °C, 10 °C/min, dwell time of 15 min). Note that this figure is only included to visualize the main trends. Since many of the tested samples did not fracture during testing, due to the equipment limit (50 kgf), a proper average cannot be made.

Table 1: Die shear strength of SLID 2a samples as a function of no of thermal cycles (0 – 200 °C, 10 °C/min, dwell time of 15 min).

As bonded (MPa)	500 cycles (MPa)	1000 cycles (MPa)
> 78	> 78	> 78
> 78	> 78	> 78
> 78	69.0	43.8
71.8	66.9	36.4
64.3	50.3	35.5

Table 2: Die shear strength of SLID 2b samples as a function of no of thermal cycles (0 – 200 °C, 10 °C/min, dwell time of 15 min).

As bonded (MPa)	500 cycles (MPa)	1000 cycles (MPa)
> 78	> 78	> 78
> 78	> 78	> 78
> 78	> 78	> 78
> 78	> 78	> 78
> 78	> 78	> 78
> 78	> 78	> 78
> 78	> 78	69.9
> 78	> 78	68.4
> 78	> 78	66.3
50.9	52.9	65.5

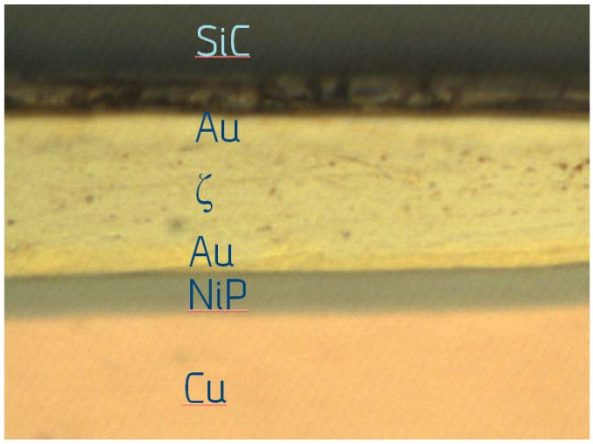

Figure 14: Optical microscopy image of a cross-section of a SLID 2b sample showing a uniform bondlayer, with excess Au on both substrate and chip side. The different phases were identified by SEM and EDS.

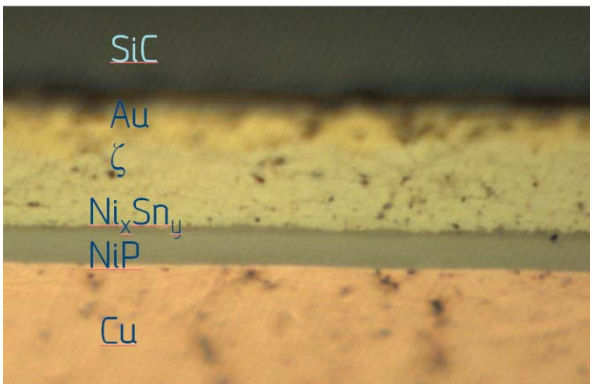

Figure 15: Optical microscopy image of a cross-section of a SLID 2a sample showing a uniform bondlayer, but with excess Au on only the chip side. On the substrate side brittle Au-Ni-Sn phases have been created, weakening the die shear strength. The different phases were identified by SEM and EDS.

Thermal Ageing

SLID 1 a & b samples

After 6 months of thermal ageing, the die shear strength was determined and compared to the as bonded strenght. Five samples from each group was tested, and the results are shown in Fig. 16.

The results had the same tendency as the thermally cycled SLID 1 a&b samples. There was a large standard deviation, the shear strength increased after ageing, the bond strength of 1b samples was higher than that of 1a samples, and the fracture surfaces of samples with high bond strength was located at the interfaces between the subsrate/chip and Ti/W, while the fracture surfaces of samples with low bond strength was located in the actual bond layer. For a more thorough discussion about these results, see the thermal cycling test section.

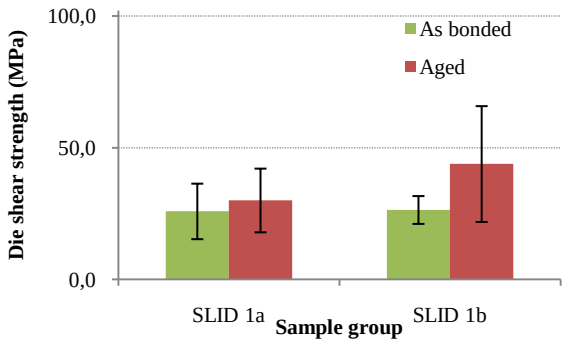

Figure 16: Die shear strength of SLID 1 a&b samples as a function of thermal ageing (250 °C, 6 months). The bars show the standard deviation for the different groups.

Conclusions

Two different AuSn SLID processing techniques were investigated, where sandwiching of an eutectic Au-Sn preform between electroplated Au layers was found to be the preferred. Initial processing issues regarding co-planarization and through cracks in the Au / Sn interface were solved, and strong uniform Au / ζ / Au joints were produced (T_m > 522°C).

The bonding strength of a Au-Sn SLID bond is shown to be superb, > 78 MPa. However, for joints without excess Au on both substrate and chip side, the shear strength is reduced as a function of thermal cycles.

Importantly, it is demonstrated that a Au-Sn SLID joint can absorb thermo-mechanical stresses induced by large CTE mismatches (12 ppm/K) in a package during HT thermal cycling.

Generally, Au-Sn SLID bonding is shown to be an excellent candidate for HT die attach and interconnect technology.

Acknowledgements

This work was carried out within the HTPEP project. Funding from the Research Council of Norway (project no 193108/S60), Badger, SmartMotor, TranSiC, Roxar and Norbitech is greatly acknowledged. Special thanks to Thi Thuy Luu and Dr. Kaiying Wang for manufacturing the SLID 1a&b samples, and Dr. Maaike M.V. Taklo and Dr. Frøydis Oldervoll for proof reading.

References

[1] R. R. Tummala and E. J. Rymaszewski, *Microelectronics Packaging Handbook*. New York: Van Nostrand Reinhold, 1989.

[2] R. R. Tummala, *Fundamentals of Microsystems Packaging*: McGraw-Hill, 2000.

[3] H. Oppermann, "The role of Au/Sn Solder in Packaging," in *Material for informations technology*, E. Zschech, Ed., Springer, 2005.

[4] H. S. Chin, K. Y. Cheong and A. B. Ismail, "A Review on Die Attach Materials for SiC-Based High-Temperature Power Devices," *Metallurgical and Materials Transactions B-Process Metallurgy and Materials Processing Science*, vol. 41, pp. 824-832, Aug 2010.

[5] L. Coppola, D. Huff, F. Wang, R. Burgos, D. Boroyevich and Ieee, "Survey on high-temperature packaging materials for SiC-based power electronics modules," in *2007*

IEEE Power Electronics Specialists Conference, Vols 1-6, 2007, pp. 2234-2240.

[6] P. Zheng, "High Temperature Electronics Packaging Processes and Materials Development," PhD, Auburn University, 2010.

[7] J. G. Bai, Z. Z. Zhang, J. N. Calata and G. Q. Lu, "Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material," *IEEE Transactions on Components and Packaging Technologies*, vol. 29, pp. 589-593, Sep 2006.

[8] C. R. Chang and J. H. Jean, "Effects of silver-paste formulation on camber development during the cofiring of a silver-based, low-temperature-cofired ceramic package," *Journal of the American Ceramic Society*, vol. 81, pp. 2805-2814, Nov 1998.

[9] P. Zheng, P. Henson, R. W. Johnson and L. Chen, "Metallurgy for SiC Die Attach for Operation at 500°C," *IMAPS International Conference & Exhibition on High Temperature Electronics (HiTEC)*, 2010.

[10] S. A. Yang and A. Christou, "Failure model for silver electrochemical migration," *IEEE Transactions on Device and Materials Reliability*, vol. 7, pp. 188-196, Mar 2007.

[11] S. H. Mannan and M. P. Clode, "Materials and processes for implementing high-temperature liquid interconnects," *IEEE Transactions on Advanced Packaging*, vol. 27, pp. 508-514, Aug 2004.

[12] G. Muralidharan, T. N. Tiegs and R. W. Johnson, "Composite Die-Attach Materials for High-Temperature Packaging Applications," in *High Temperature Electronic Conferance (HiTEC)*, Santa Fe, 2006.

[13] Y. Takaku, I. Ohnuma, R. Kainuma, Y. Yamada, Y. Yagi, Y. Nishibe, *et al.*, "Development of Bi-base high-temperature Pb-free solders with second-phase dispersion: Thermodynamic calculation, microstructure, and interfacial reaction," *Journal of Electronic Materials*, vol. 35, pp. 1926-1932, Nov 2006.

[14] L. Bernstein, "Semiconductor joining by solid-liquid-interdiffusion (SLID) process.," *Journal of the Electrochemical Society*, 1966.

[15] L. Bernstein and H. Bartholomew, "Applications of Solid-Liquid Interdiffusion (SLID) Bonding in Integrated-Circuit Fabricatoin," *Transactions of the Metallurgical Society of AIME*, vol. 236, pp. 405-411, 1966.

[16] D. S. Duvall, W. A. Owczarski and D. F. Paulonis, "TLP Bonding: A New Method for Joining Heat Resisant Alloys," p. 203, 1974.

[17] W. D. Macdonald and T. W. Eagar, "TRANSIENT LIQUID-PHASE BONDING," *Annual Review of Materials Science*, vol. 22, pp. 23-46, 1992.

[18] R. Schmid-Fetzer, "Design Fundamentals of High-Temperature Composites, Intermetallics and Metal-Ceramic Systems," R. Y. Lin, Ed., Warrendale, PA: TMS, 1995, pp. 75-97.

[19] W. R. Johnson, C. Q. Wang, Y. Liu and J. D. Scofield, "Power Device Packaging Technologies for Extreme Environments," *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 30, pp. 182-193, 2007.

[20] K. E. Aasmundtveit, K. Y. Wang, N. Hoivik, J. M. Graff and A. Elfving, "Au-Sn SLID Bonding: Fluxless Bonding with High Temperature Stability, to Above 350 degrees C," in *2009 European Microelectronics and Packaging Conference*, 2009, pp. 723-728.

[21] K. Aasmundtveit, T. T. Luu, H. Nguyrn, R. Johannessen, N. Hoivik and K. Wang, "Au-Sn fluxless SLID bonding: Effect of bonding temperature for stability at high temperature, above 400°C," *Electronics System Integration Technology Conference*, 2010.

[22] J. F. Li, P. A. Agyakwa and C. M. Johnson, "Kinetics of Ag3Sn growth in Ag-Sn-Ag system during transient liquid phase soldering process," *Acta Materialia*, vol. 58, pp. 3429-3443, May 2010.

[23] C. L. Lee, Y. W. Wang and G. Matijasevic, "Advances in Bonding Technology for Electronic Packaging," *Journal of Electronic Packaging*, vol. 115, pp. 201-207, 1993.

[24] K. Wang, K. Aasmundtveit and H. Jakobsen, "Surface Evolution and Bonding Properties of Electroplated Au/Sn/Au," in *ESTC 2008: 2nd Electronics System-Integration Technology Conference, Vols 1 and 2, Proceedings*, New York, 2008, pp. 1131-1133.

[25] G. S. Matijasevic, C. C. Lee and C. Y. Wang, "AU-SN ALLOY PHASE-DIAGRAM AND PROPERTIES RELATED TO ITS USE AS A BONDING MEDIUM," *Thin Solid Films*, vol. 223, pp. 276-287, Feb 1993.

[26] N. Hoivik, K. Aasmundtveit, G. Salomonsen, A. Lapadatu, G. Kittilsand and

B. Stark, "Fluxless wafer-level Cu-Sn bonding for micro-and nanosystems packaging," presented at the Electronics System Integration Technology Conferences Berlin, 2010.

[27] H. Huebner, S. Penka, B. Barchmann, M. Eigner, W. Gruber, M. Nobis, *et al.*, "Microcontacts with sub-30 mu m pitch for 3D chip-on-chip integration," *Microelectronic Engineering*, vol. 83, pp. 2155-2162, Nov-Dec 2006.

[28] S. Bader, W. Gust and H. Hieber, "RAPID FORMATION OF INTERMETALLIC COMPOUNDS BY INTERDIFFUSION IN THE CU-SN AND NI-SN SYSTEMS," *Acta Metallurgica Et Materialia*, vol. 43, pp. 329-337, Jan 1995.

[29] P. F. Yang, Y. S. Lai, S. R. Jian, J. Chen and R. S. Chen, "Nanoindentation identifications of mechanical properties Of Cu6Sn5, Cu3Sn, and Ni3Sn4 intermetallic compounds derived by diffusion couples," *Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing*, vol. 485, pp. 305-310, Jun 2008.

[30] W. W. So, C. C. Lee and E. I. A. Eia, "High temperature joints manufactured at low temperature," in *48th Electronic Components & Technology Conference - 1998 Proceedings*, New York IEEE, 1998, pp. 284-291.

[31] R. W. Chuang and C. C. Lee, "Silver-indium joints produced at low temperature for high temperature devices," *IEEE Transactions on Components and Packaging Technologies*, vol. 25, pp. 453-458, Sep 2002.

[32] P. Quintero, "DEVELOPMENT OF A SHIFTING MELTING POINT Ag-In PASTE VIA TRANSIENT LIQUID PHASE SINTERING FOR HIGH TEMPERATURE ENVIRONMENTS," PhD, Department of Mechanical Engineering, University of Maryland, 2008.

[33] H. Okamoto, "Au-sn (Gold-Tin)," *Journal of Phase Equilibria and Diffusion*, vol. 28, pp. 490-490, Oct 2007.

[34] H. S. Liu, C. L. Liu, K. Ishida and Z. P. Jin, "Thermodynamic modeling of the Au-In-Sn system," *Journal of Electronic Materials*, vol. 32, pp. 1290-1296, Nov 2003.

[35] R. Johannessen, F. Oldervoll, A. Larsson and T. Fallet, "High Temperature Power Electronic Packaging for Oil Well Applications," in *High Temperature Electronics Network (HiTEN)*, Oxford, UK, 2009.

[36] Z. J. Shen, B. Grummel, R. McClure, A. Gordon and A. Hefner, "High Temperature, High Power Module Design for Wide Bandgap Semiconducters: Packaging Architecture and Materials Considerations," presented at the HiTEC, Albuquerque, 2008.

[37] M. N. Yoder, "Wide bandgap semiconductor materials and devices," *IEEE Transactions on Electron Devices*, vol. 43, pp. 1633-1636, Oct 1996.

[38] N. G. Wright, A. B. Horsfall and K. Vassilevski, "Prospects for SiC electronics and sensors," *Materials Today*, vol. 11, pp. 16-21, 2008.

[39] H. Hieber, A. Swiderski, S. Bader and W. Gust, "Heat –Resistant Contacts with Use of Liquid Phase Transition," in *Proc. 7th European Hybrid Microelectronic Conf. Session 1.4.*, Hamburg, 1993, pp. 7-13.

[40] D. R. Frear, F. M. Hosking and P. T. Vianco, *MECHANICAL-BEHAVIOR OF SOLDER JOINT INTERFACIAL INTERMETALLICS*. Materials Park: Asm International, 1991.