Advanced Stepper Through-Silicon Alignment (TSA) Evaluation and Overlay of Distorted Bonded Wafer Stacks

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Abstract

Canon Litho Products support Vertical Lithography challenges required by TSV and advanced packaging applications that support "More-than-Moore" advancements. Vertical Lithography challenges include accurately performing backside, infrared alignment to distorted bonded-wafer grids and imaging through thick resist films.

This paper will provide examples illustrating severe wafer distortion that can be experienced after wafer thinning and the impact of overlay and imaging control. This paper will also introduce Canon stepper features that are designed to address Vertical Lithography challenges including the Canon Through-Silicon Alignment (TSA) System and advanced Projection Lens. Grid distortion characterization data and stepper compensation results are presented to illustrate Canon stepper technology performance under severe process conditions.

Keywords: Through-Silicon Alignment (TSA), Infrared Metrology, Bonded-Wafer, Stepper

Introduction

Grid Distortion

Increases in interconnect density can improve system bandwidth and reductions in wafer thickness and interconnect lengths can increase reduce processing speed and reduce power consumption. As interconnect densities increase and wafer thicknesses decrease, wafer distortion also increases. Wafer grid distortion is influenced by stresses introduced during the wafer bonding, heat-treating and thinning processes.

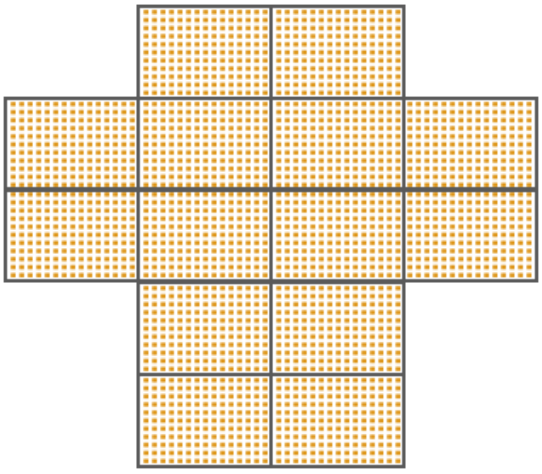

Figure 1: Non-distorted wafer possess small wafer and intra-field error

Canon research has observed over 1µm of pattern grid distortion between top and bottom wafers in bonded wafer stacks, with over 200nm variability between wafers. Advanced overlay compensation techniques must be applied by the stepper to properly overlay such distorted wafer grids. A non-distorted wafer grid illustration is provided in Figure 1.

A distorted wafer grid example demonstrating grid and intra-field distortion due to wafer bonding and thinning is provided in Figure 2.

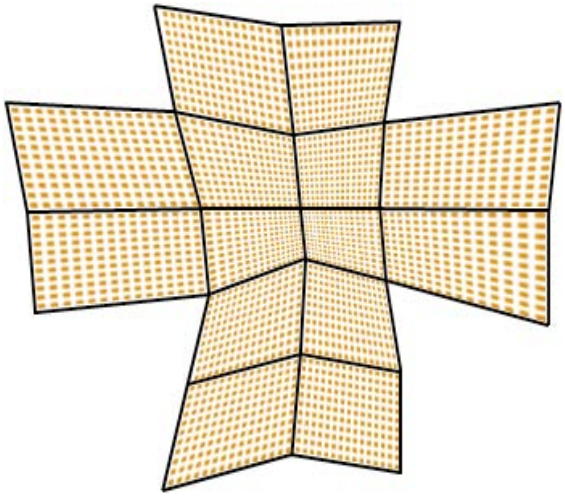

Figure 2: Wafer grids can distort after bonding and thinning

Canon FPA-5510iZ-TSA & FPA-5510iV Steppers

This manuscript will introduce the Through-Silicon Alignment (TSA) System that is available as an option on select Canon photolithography systems. The Canon FPA-5510iV stepper features the TSA System as well as a wide-field, low-Numerical Aperture (NA) optical system that provides a large depth-of-focus depth of focus suited to thick resist processes (≥ 100µm thickness). The Canon FPA-5510iZ-TSA stepper features the TSA System and a larger NA that provides increased resolution (≤ 280nm). An illustration depicting a Canon TSA Stepper is provided below in Figure 3 and a comparison of Canon stepper specifications is provided in Table 1.

Figure 3: Canon TSA Stepper

Table 1: Canon TSA Stepper Specification Comparison

Benefit	Item	FPA-5510iV Specification	FPA-5510iZ-TSA Specification
Imaging	Red. Ratio / Field Size	2:1 / 52 x 34mm	4:1 / 26 x 33mm
	Numerical Aperture	0.10-0.18	0.45-0.57
	Sigma	0.40-0.80	0.40-0.75
	Resolution	≤ 1.5µm L&S (≤ 1.0µm, off-axis illum.)	≤ 350nm L&S (≤ 280nm, off-axis illum.)
	DOF	≥ 10µm (@ 1.5µm) ≥ 6µm (@1.0µm)	≥ 1.2µm (350nm)
Alignment	Backside Alignment Option	Through-Silicon Alignment (TSA)	Through-Silicon Alignment (TSA)
	Overlay Accuracy (w/ *TSA Option)	≤ 0.300µm (front) ≤ 0.300µm (back)	≤ 100nm (front) ≤ 200nm (back)
Options	Shot-by-Shot Compensation	EAGA (Enhanced AGA)	EAGA (Enhanced AGA)
	Front-to-Back Overlay Metrology	D-Map (Dual-Side Metrology)	D-Map (Dual-Side Metrology)
	Warped Wafer Handling	≥ 450µm	≥ 450µm
	Wafer Edge Applications	WES (shield) WEE (expose)	WES (shield) WEE (expose)
	Thick Resist Processing	Resist Outgas Unit	Resist Outgas Unit

Through-Silicon Alignment (TSA) System

To provide accurate backside overlay to targets buried under silicon in a bonded wafer stack, Canon steppers including the FPA-5510iV and FPA-5510iZ-TSA utilize the infrared Through-Silicon Alignment (TSA) System to measure wafer grid distortion. An example of a bonded wafer stack requiring top-to-bottom (front-to-back) wafer stack overlay is illustrated in Figure 4.

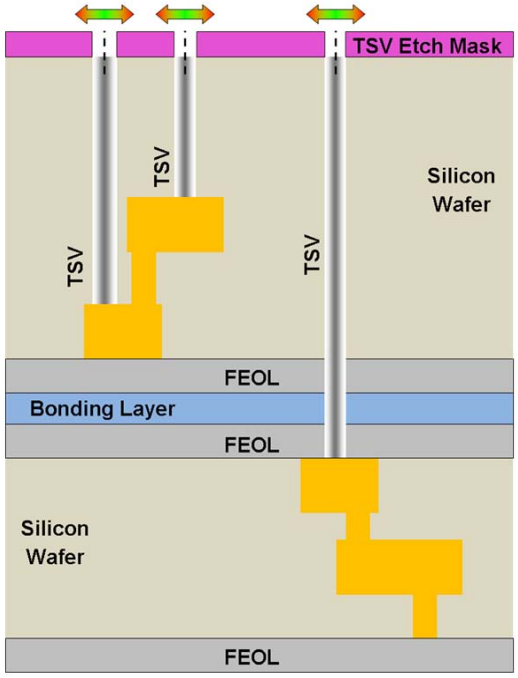

Figure 4: Through-Silicon Vias (TSV) must be aligned to structures buried under silicon. TSV top-side etch masks must be aligned accurately by stepper during exposure

The Canon TSA System measurement scope is integrated into the stepper main body and projection lens as shown in Figure 5. The TSA System Alignment Light Source provides a variety of illumination options that provide robust alignment process capability.

The TSA System can measure alignment marks on the back side of the wafer with infrared light that passes through the silicon wafer and can also measure alignment targets on the front side of the wafer with using the TSA System and a wavelength range that does not penetrate silicon.

An illustration describing the optical theory behind the TSA Scope is provided in Figure 6.

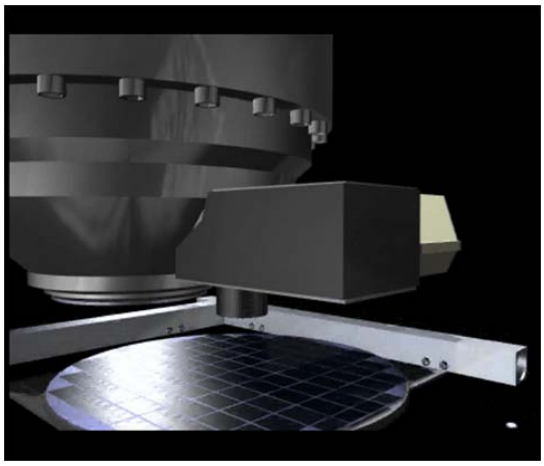

Figure 5: Through-Silicon Alignment (TSA) System provides infrared, wafer back-side alignment capability to Canon steppers

A list of standard Alignment Modes and IR wavelength bands for Canon TSA Steppers is detailed in Table 2.

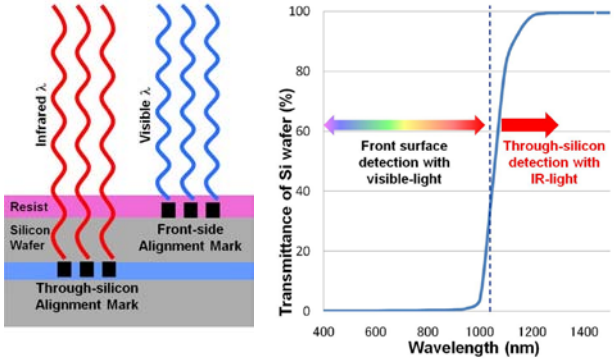

Figure 6: Canon TSA System provides multiple wavelength band and contrast options, including visible light for top-side (front-side) alignment, and infrared light for through-silicon alignment.

Table 2: TSA Alignment Options provide center-wavelength, wavelength bandwidth and illumination sigma value optimization.

Mode	Parameter	Description
1	BB2/W/Normal	Broadband / Wide λ Range / Normal Contrast
2	BB2/S/High	Broadband / Short λ Range / High Contrast
3	BB2/W/High	Broadband / Wide λ Range / High Contrast
4	TSA/W/Normal	TSA (IR) / Wide λ Range / Normal Contrast
5	TSA/S/Normal	TSA (IR) / Short λ Range / Normal Contrast
6	TSA/L/Normal	TSA (IR) / Long λ Range / Normal Contrast
7	TSA/W/High	TSA (IR) / Wide λ Range / High Contrast
8	TSA/S/High	TSA (IR) / Short λ Range / High Contrast
9	TSA/L/High	TSA (IR) / Long λ Range / High Contrast

Advanced Global Alignment (AGA)

The standard Canon stepper wafer fine-alignment sequence is known as Advanced Global Alignment (AGA). During the AGA measurement sequence, the stepper will measure alignment target locations for a variety of Sample Shots across a wafer. Based on the measurement data collected, the stepper can apply wafer magnification X & Y (scaling), wafer rotation X & Y (orthogonality), shot shift X & Y, shot magnification and shot rotation to each shot (shot = single exposure field) on the wafer. Compensation values are based on linear compensation models derived from the AGA measurement data. In severely distorted wafers, overlay alignment using linear compensation variables only is challenging.

Users can specify a multiple alignment targets to be measured during the AGA sequence and mark position, mark type and measurement direction values may be defined for each recipe. Recipes specifying TSA alignment marks buried beneath silicon may also specify the mark depth in silicon.

Figure 7 offers an outline of a typical AGA compensation and exposure sequence.

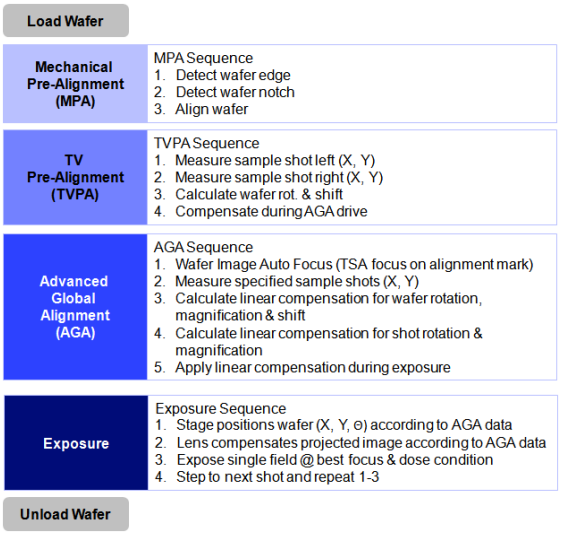

Figure 7: Advanced Global Alignment (AGA) compensation sequence

AUX XY Stage Accuracy (AXUXYSA) Command

The internal metrology of the TSA System can also be used to qualify system and process performance. Canon steppers feature the command function AUXXYSA (Auxiliary XY Stage Accuracy) that measures and outputs data mapping alignment target positions across a wafer grid. Analysis of AUXXYSA data maps has demonstrated that wafer grid distortion can be severe, and steppers utilizing only the standard Advanced Global Alignment (AGA) overlay function will struggle to meet future, dense-interconnect overlay requirements. Overlay accuracy can be improved by increasing the number of AGA sample shots measured on each wafer, although only linear compensation is available to correct for grid distortion.

Figures 8 illustrates the steps involved in performing an AUXXYSA measurement and presents an example of an AUXXYSA grid map displaying severe distortion.

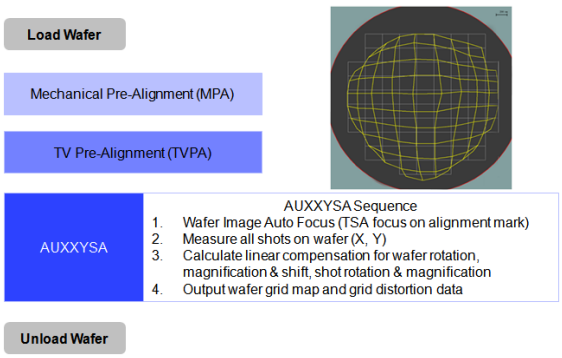

Figure 8: AUXXYSA measurement sequence and distorted grid output example

Enhanced AGA (EAGA)

For severely distorted wafers, the linear compensation provided by AGA compensation may not provide sufficient overlay across the entire wafer and/or across individual exposure fields and advanced shot-by-shot compensation by the stepper may be required. One solution Canon steppers offer to provide shot-by-shot compensation is through the advanced alignment sequence known as Enhanced Advanced Global Alignment (EAGA).

During the EAGA sequence the TSA System measures alignment marks within each shot on a wafer. By evaluating multiple intra-field alignment marks in each field, actual shot shift, shot magnification and shot rotation may be measured and compensated. Figure 9 illustrates the steps involved in the EAGA compensation sequence.

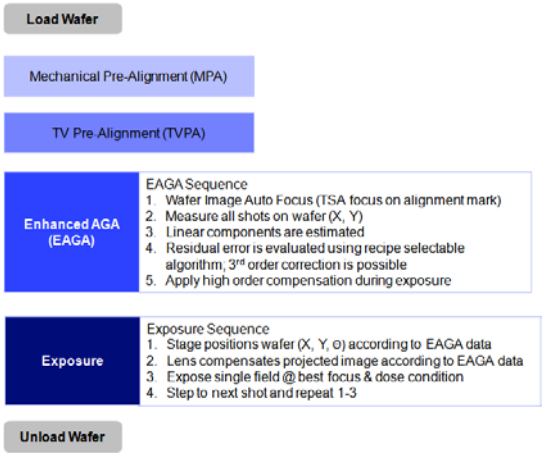

Figure 9: Enhanced AGA (EAGA) compensation sequence

Dual-Side Metrology Application Program (D-MAP)

The TSA System can also be used to measure top-to-bottom overlay accuracy through the use of the Dual-Side Metrology Application Program (D-MAP) command function.

D-MAP is an automatic command function capable of measuring and comparing the overlay registration of front-side and back-side patterns on a bonded wafer. During the D-MAP measurement sequence, the stepper automatically switches from visible light to infrared light for backside measurement and automatically outputs measurement data, calculated compensation values and grid maps. The D-MAP measurement concept is illustrated in Figure 10.

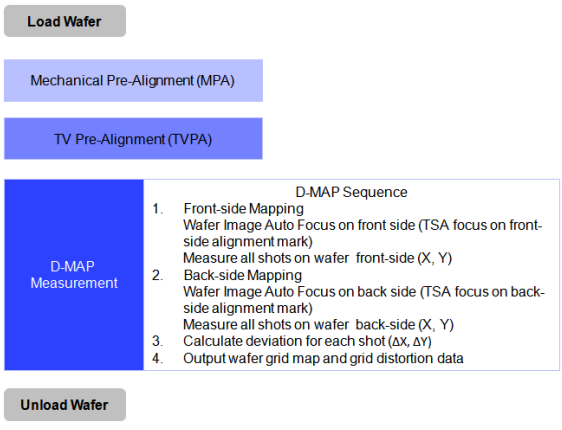

Figure 10: D-MAP measurement sequence

D-MAP utilizes the TSA System and Wafer Stage to perform the overlay metrology measurement and the D-MAP measurement sequence is presented in Figure 11.

Ideally, bonded wafer distortion will be eliminated by improvements in bonding and thinning processes, but until that time, steppers must match their image pattern to the existing distorted grids. To meet this demand, Canon will continue to evaluate and improve its Through-Silicon Alignment and Enhanced Overlay capabilities

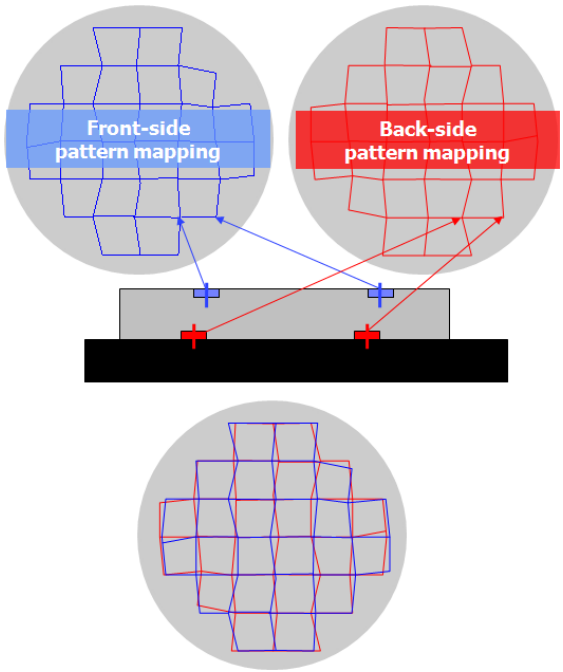

Figure 11: Dual-Side Metrology Application Program (D-MAP) allows front-to-back overlay registration measurement

Experimental

TSA System Performance

Canon TSA System research has demonstrated 15nm 3-Sigma, back-side alignment measurement repeatability through a variety of substrate process conditions and has successfully aligned to marks buried under more than 700microns of silicon. Comparison data illustrating TSA System front-side and back-side, through-silicon measurement repeatability is provided in Figure 12. The data shows that the TSA System can deliver highly repeatable measurements through silicon.

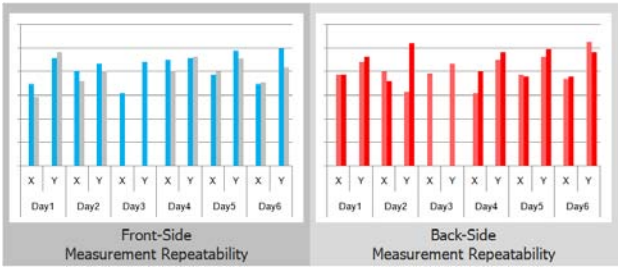

Figure 12: TSA System front-side & back-side measurement repeatability ≤ 15nm

AGA Compensation

Initial Canon studies focused on confirming standard system performance using standards wafers and test conditions. Using standard AGA compensation methods, Canon demonstrated front-to-back overlay accuracy of less than 112nm, which is considered tolerable for 1.5micron processes [1]. Data illustrating standard grid distortion and overlay registration error are provided in Figure 13.

Wafers possessing non-linear distortion may not be able to be accurately overlaid given the linear compensation provided by AGA. AGA measures the position of several sample shots and calculates compensation values based on the measurement data but error residual values ≥ 200nm are not uncommon. Large random errors may not be compensated sufficiently and Figure 14 provides an illustration residual overlay error when only linear AGA compensation is applied to a non-linear wafer grid.

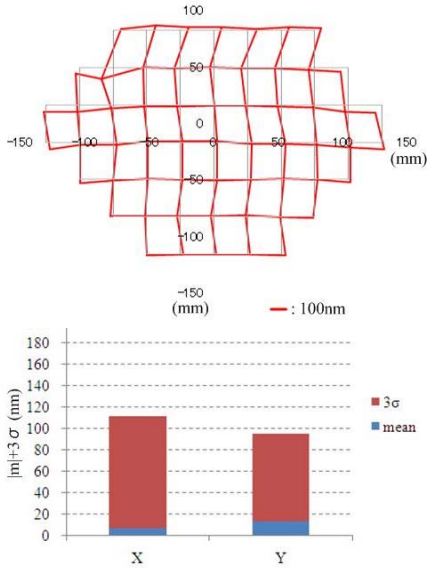

Figure 13: AGA compensation of standard wafers provides overlay accuracy ≤ 112nm

Bonded Wafer Evaluation: AUXXYSA

Canon has examined the stepper overlay accuracy with bonded wafers and that are required for TSV process applications. In a Via-Last TSV process, TSVs are created on a wafer containing front-side patterning imaged during front-end-of-the-line (FEOL) processing. Thinned wafers are commonly bonded temporarily to a full-thickness wafer or support substrate to increase rigidity.

The TSA System and AUXXYSA has been utilized to evaluate the effects of bonding and thinning on bonded wafers by collecting pre-bonding/thinning and post-bonding/thinning wafer grid data. Canon has evaluated distortion effects of thinning on wafers as thin as 30microns [1]. AUXXYSA data has clearly demonstrated the impact of bonding/thinning and the images shown in Figure 15 illustrate the more that 285nm of distortion that has been measured after bonding/thinning.

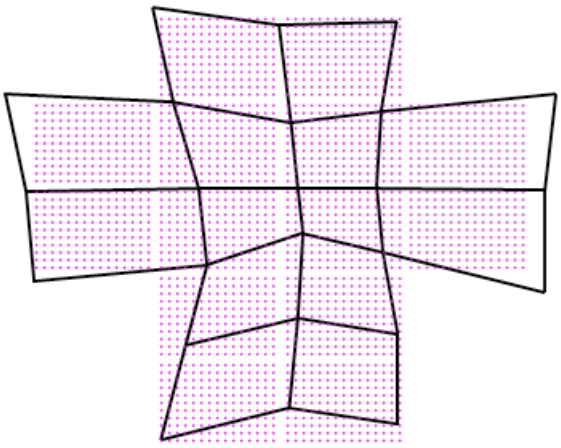

Figure 14: AGA linear compensation may not be able to accurately overlay severely distorted wafers exhibiting random errors

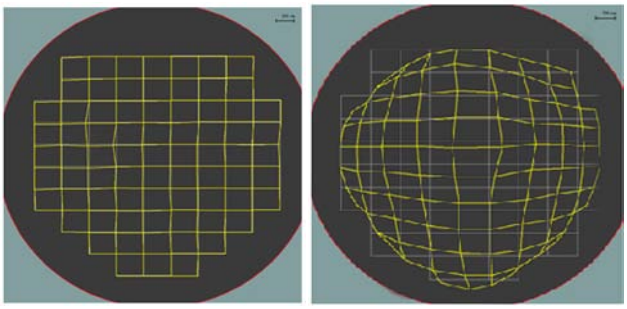

Figure 15: Grid 3σ pre-bonding/thinning ≤ 30nm; Grid 3σ post-bonding/thinning ≥ 285nm

AUXXYSA data can be used to evaluate wafer grid distortion and to estimate the effect of linear compensation factors to correct for grid distortion.

AUXXYSA has been performed to map the grid on a variety of bonded wafer stacks before and after bonding and thinning of the top wafer. Before the AUXXYSA measurement is performed, stepper process settings are optimized to provide the best alignment signal during measurement the wafer grid evaluation. Illumination conditions and alignment mark types are evaluated in terms of mark image waveform, contrast, XY Shift range and the TSA Scope repeatability for each condition.

An example of an alignment mark as viewed through silicon by the TSA Scope is provided in Fig. 16. AUXXYSA measurements to evaluate grid distortion are performed under optimum alignment conditions.

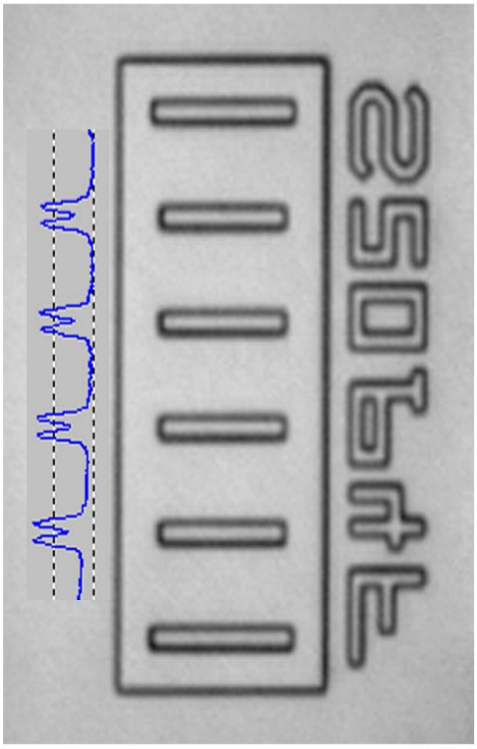

Figure 16: Alignment targets are clearly visible through full-thickness silicon wafers using the TSA System. Mark waveform, contrast and measurement repeatability are strong

EAGA Compensation

EAGA compensation simulations have been conducted to estimate the effect of applying shot-by-shot compensation to severely distorted wafers exhibiting large amounts of wafer and intra-field distortion.

EAGA is an advanced alignment method that corrects for magnification, rotation and shift on a shot-by-shot basis. When compared to linear AGA compensation, sample EAGA data has shown a reduction in overlay error from 275nm to 110nm as illustrated by the illustration in Figure 17.

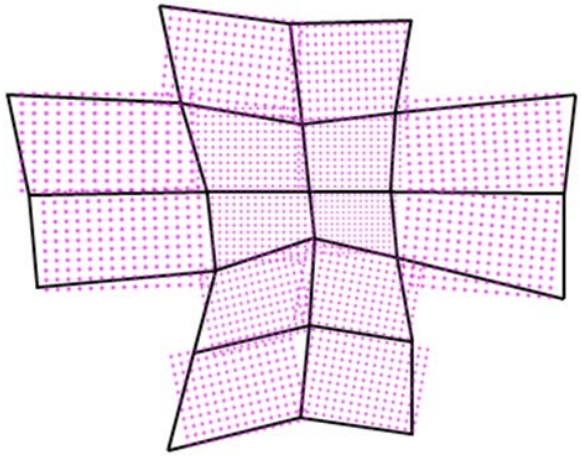

Figure 17: EAGA compensation provides shot-by-shot overlay correction to allow accurate overlay of distorted wafers

Results and Discussions

AUXXYSA data collected by Canon clearly demonstrates that wafer grid distortion does occur in bonded and thinned wafer stacks with wafer grid distortion in excess of 300nm has been experienced.

EAGA represents a solution for customers seeking to improve their stepper overlay on non-linearly distorted grids. If wafer-to-wafer grid distortion is equal, EAGA can be configured to measure each alignment target on the first wafer only, although wafers exhibiting random distortion will require wafer-by-wafer, shot-by-shot measurement and overlay compensation which will negatively affect throughput. EAGA has demonstrated 30%-50% overlay improvement in severely distorted wafers and EAGA represents step towards accurate front-to-back alignment even in the most demanding wafer conditions. If repeatable, shot-by-shot offsets may be applied in a recipe, with AUXXYSA data used to manually offset overlay with shot-to-shot shift, rotation and magnification offsets.

Shot-by-shot alignment data may also be collected off-line from the stepper and shot-specific offsets may be manually input into the recipe for each process. Off-line wafer measurement allows the stepper to maximize wafer throughput by minimizing measurement time, while providing sufficient sampling to support bonded and distorted wafer applications.

Conclusions

This paper discusses how Canon addresses the challenges of wafer grid distortion in bonded wafer stacks. Current TSV process distortion is manageable, but will become an issue as device geometries are reduced and interconnect density increases. Reducing grid distortion of bonded wafers will become a priority in the future.

Until the industry removes distortion form bonded wafers, TSV steppers will require robust Through-Silicon Alignment systems and powerful compensation capabilities designed for demanding front-end applications to insure accurate front-to-back overlay accuracy across all fields of every wafer.

Future TSA evaluation plans include application of EAGA to distorted bonded-wafer stacks to confirm compensation accuracy. Experimentation will also include multi-wafer testing to determine wafer-to-wafer distortion tendencies and experimentation to correlate DMAP data to product overlay results.

Canon has developed the FPA-5510iV and FPA-5510iZ-TSA steppers to support upcoming high-density processes and to provide essential performance and functions to support implementation of “More than Moore,” technology. The FPA-5510iV delivers good imaging profiles through thick resist, the ability to perform accurate backside alignment and overlay to support TSV last processes. Canon is ready to provide a Vertical Lithography solution to meet the diverse requirements of device production in the future.

References

[1] S. Hirai, N. Saito, Y. Goto, H, Suda, K. Mori and S. Miura, “A study of vertical lithography for high-density 3D structures,” SPIE Advanced Lithography 2012, February 2012.