Thick Film Technology For Today's Hearing Products

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Abstract

There has been continuous worldwide effort to increase the volumetric efficiency of electronic packaging. Much of this effort has been driven by the telecommunications industry that has succeeded in reducing cell phone size while simultaneously increasing functionality. The hearing aid business has always had the need to use extremely small electronic packaging because hearing aids pack electronics into the ear canal. The first commercial product using the transistor in 1952 was a hybrid vacuum tube-transistor hearing instrument. Today's hearing aids, such as Starkey's 3-Series product, have significant computing power and run complex hearing algorithms that have enormous impact on a patient's quality of life. The industry trend is to put more memory, more signal processing capability and more wireless capability into hearing aids to increase functionality and to improve performance. In order to achieve this increase in performance, the hearing business has had to develop and execute 3D packaging well ahead of other industries.

This paper will examine the history of ceramic hybrid packaging at Starkey. The challenges and drivers for major technology steps will be addressed. The following technical advancements, transitions, considerations and limitations will be examined: changing ASIC technologies, impact of chip metallization, solder interconnect temperature hierarchy, impact of RoHS legislation, overcoming routing design limits, miniaturization realized by flip chip attach, impact of chip stacking on size, migration to stacked thick film ceramic interconnect layers using vertical interconnect channels, advances in thick film materials to support higher interconnect density, and incorporation of integrated passive devices.

Key words

Integrated Passive Device (IPD), Chip-on-flip chip (COFC), Vertical Interconnect (VIC), Multi-chip module (MCM) and System in a Package (SIP).

I. Introduction

Starkey first started using ceramic hybrid technology around 1994. The predominant mainstream processor technology used at that time was the P5 Pentium using the 0.8 μm technology node; however, hearing aid electronics used much more humble 3 μm technology at that time. This was before the release of Windows 95. Over the course of 20 years four different design and manufacturing facilities were built: two in Eden Prairie, Minnesota and two in Suzhou, China.

Hearing aids have always required small electronics because there was no other option [1-4]. Consequently, hearing aid engineers have always had to be on the forefront of miniaturization. Ceramic hybrid circuit technology enabled the entire hearing aid circuit to be placed in a single package. Wires could be soldered directly to pads on the bottom of the ceramic hybrid circuit to connect the switches, battery, microphone and receiver. Internally all the chips were wire bonded. The circuit could be fully encapsulated producing a robust electronics package that could be subjected to the fairly rough assembly practices of the time.

Over many years, modest process improvements were made that enabled thinner ceramic substrates to be used, with increased pad density and finer lines and spaces. Chip stacking advanced circuit density and enabled increased circuit complexity without having to make significant changes to the hybrid circuits manufacturing process.

Eventually, creative engineers needed to add more components than could be stacked and the vertical interconnect system was developed to create a multi-layer interconnect system and thick film passive devices were integrated into the interconnect fabrication process. The use of flip chip technology helped to further shrink vertical dimensions.

With chip I/O increasing with each new generation, tighter and tighter line density was required that drove materials and process changes. Integrated passive devices began to be used to provide both increased interconnect density and increased capacitance all within the silicon substrate.

The use of stand-alone hybrid circuits in custom hearing aids has been decreasing because the introduction of wireless technology to hearing aids increased circuit complexity beyond what can be placed in a single hybrid circuit. Instead of attaching wires to the circuit directly, most new hybrids are in a BGA format for surface mount attach to a flexible circuit that contains many more components. The hybrid circuit has become a means of densely packaging some of the hearing aid circuit and multiple hybrids are starting to appear in new designs. Additionally, the lines between various forms of multi-chip modules are blurring. It is not clear that it is important to distinguish between an embedded die multi-chip module and a ceramic hybrid circuit.

This paper is going to discuss Starkey's journey in miniaturization using thick film ceramic hybrid technology, beginning in 1994 and continuing to multi-chip modules currently being fabricated in 2014.

II. History of Ceramic Packaging at Starkey

In 1994 Starkey designed its first hybrid called the STG that was intended for a hand-wired custom hearing aid product. See Fig.1. This device was a simple one analog integrated circuit device with eight wire bonds to the ceramic surface that had two 0402 surface mounted capacitors. The device measured 0.05" x 0.045" x 0.018".

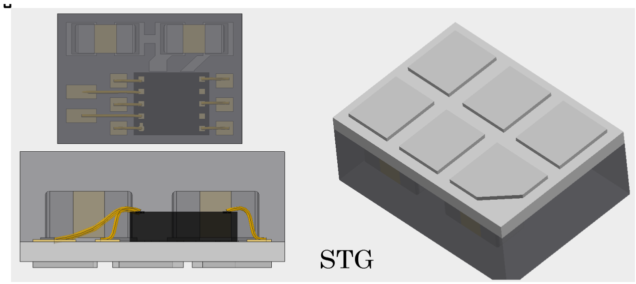

Fig. 1. Starkey's first ceramic hybrid package, STG.

Complexity quickly increased. In 1995 another hand-wired custom product called the OSS hybrid was built. See Fig. 2. The die was a high performance compression pre-amp with class D output. This die was flip chip attached to the thick film surface using conductive epoxy for contacts because the die was not available with solder bumps. The thick film had internal capacitors, but also had four 0402 surface mounted capacitors attached. There were 16 hand-wired pads on this hybrid. The hybrid measured 0.160" x 0.086" x 0.018". The entire hearing aid circuit was inside this single package. Fig. 3 shows the entire hearing aid schematic for this device.

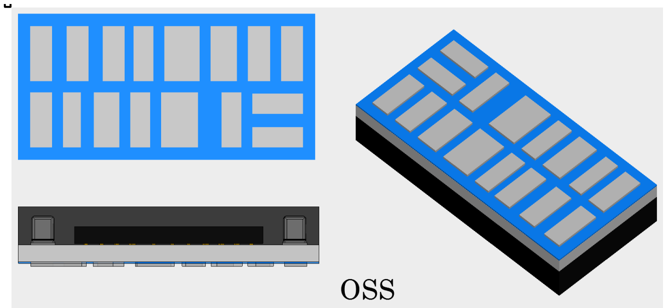

Fig. 2. Second generation ceramic hybrid, OSS.

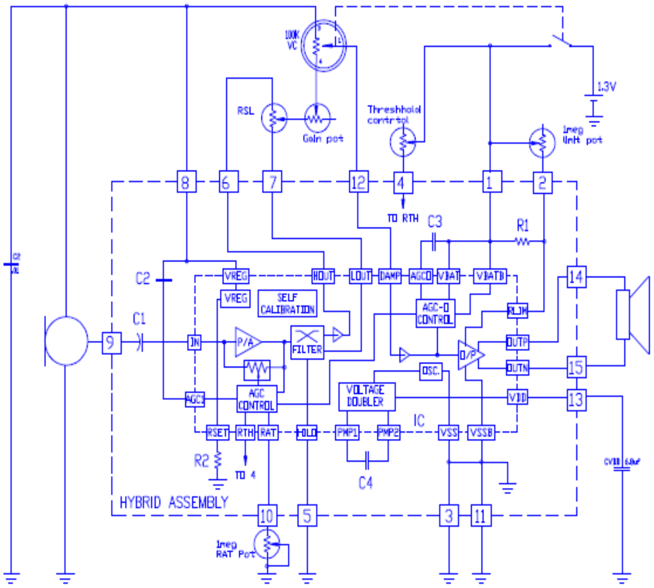

Fig. 3. Schematic of OSS.

In 1997 the first multi-chip hybrid called the AGB was produced. See Fig. 4. This device had a conductive epoxy mounted die on a ceramic subassembly with internal passives and five surface mounted capacitors; the subassembly was mounted on top of another conductive epoxy mounted die on the main board and was connected to the main board by five wire bonds. Additional capacitors were mounted on the bottom side ceramic along with 13 direct wire attach pads. The device measured 0.169" x 0.086" x 0.018".

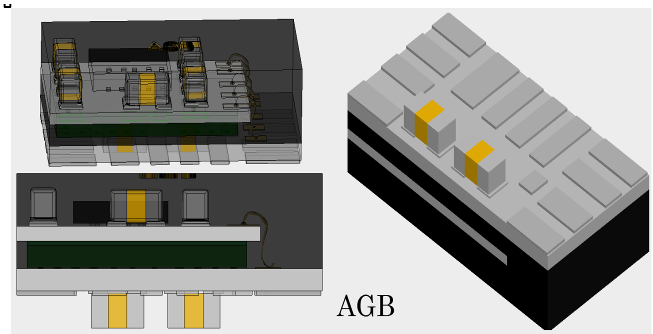

Fig. 4. Starkey's first multi-chip hybrid, AGB.

In 1999 the first vertically interconnected multi-layer hybrid called the SSJ was built. See Fig. 5. This was a first in the industry and included digital programing of analog filters and was intended for both custom and standard hearing aid products. This package had solder pads on both top and bottom surfaces. The device also had surface mounted capacitors on both top and bottom surfaces. The device measured 0.121" x 0.102" x 0.012".

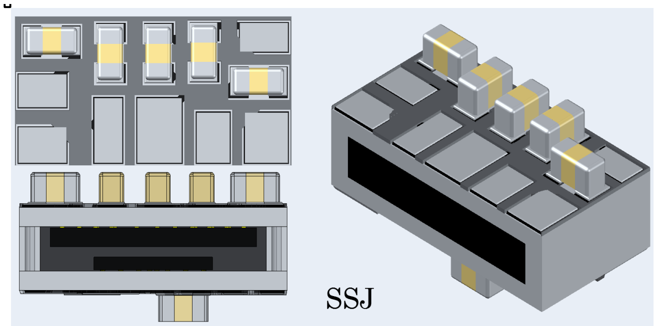

Fig. 5. Starkey's first vertically interconnected multi-layer hybrid, SSJ.

In 2001 the first 3-die package was produced called the ATC using module on flip chip construction. See Fig. 6. This device was intended for use in both custom and standard hearing aids. The die included an analog die, a digital processor and an EEPROM. This device had the first digital processor in a Starkey hearing aid. All three die were solder bump flip chip attached. Two die were flip chip attached on opposite sides of a ceramic sub-assembly that was subsequently attached to a spacer on top of the solder bump flip chip attached die on the main board. The spacer was used to lift up the assembly giving clearance for the two 0402 capacitors on the main board. There were also three 0201 devices on the main board. The device measured 0.124" x 0.103" x 0.015".

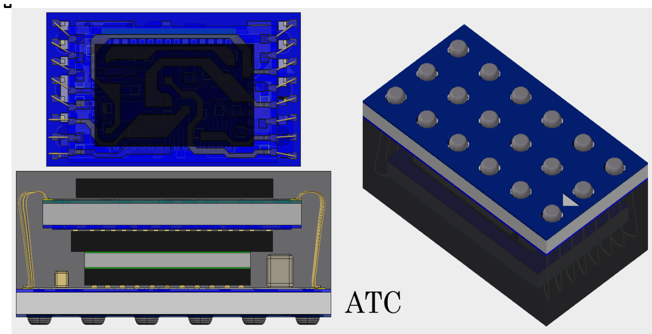

Fig. 6. Starkey's first three-chip package, ATC.

In 2003 the first full digital signal processor was used in conjunction with an EEPROM using chip-on-flip chip construction; the device was called the ACI. See Fig. 7. This design is now considered the classic hearing amplifier construction, in which the processor is flip chip bonded to the thick film surface and the EEPROM is attached to the flip chip die back side where it is wire bonded to the thick film surface. Millions of hearing aids have been made using this construction and it is still used today because of its small size. The device measured 0.169" x 0.081" x 0.009".

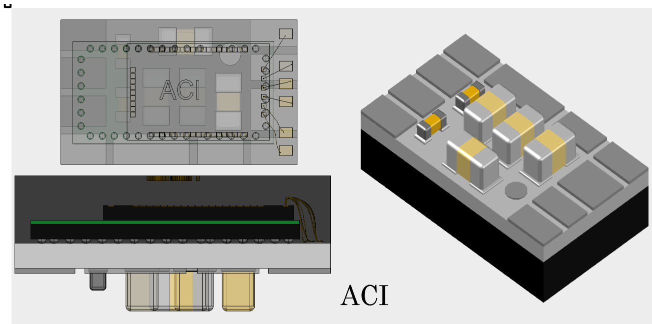

Fig. 7. Starkey's first hybrid utilizing a full digital signal processor and EEPROM with flip chip construction, ACI.

In 2006 wireless technology was beginning to make in-roads into the hearing aid business. Near-field magnetic induction communication (NFMI) radios were largely being used. The more modern 2.4 GHz made for iPhone hearing aids did not materialize until much later in 2014. A 900 MHz ceramic hybrid complete hearing aid circuit was the first wireless design, called the SOX. See Fig. 8. This device included a 130 nm digital signal processor, 512K EEPROM, custom radio chip and crystal. It was a vertically connected two-layer hybrid circuit. The circuit had one 0603, six 0402 and nine 0201 components for a total part count of 20. The device measured 0.157" x 0.109" x 0.009".

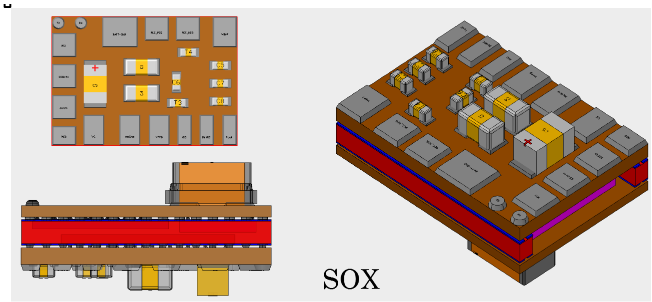

Fig. 8. Starkey's first wireless ceramic hybrid device, SOX.

In 2008 a custom hearing aid circuit called the TCI was made using a very sophisticated 90 nm ultra-low power digital signal processor in combination with two 512K EEPROM die and a fourth chip select die. See Fig. 9. There were two 0603 passives along with two 0402 passives and 10 0201 passives. This was the first photoimageable dielectric-based thick film circuit that enabled very high routing density. This circuit is still being built today in high volume. The digital signal processor is solder bump flip chip attached to the surface of the ceramic, with a spacer then attached on top. The spacer was used to lift up the assembly giving clearance for the two 0402 capacitors on the main board. n interposer is present on top of the spacer to connect the two EEPROMs and create a surface to wire bond the EEPROMs to the main board. The completed hybrid measures 0.226" x 0.136" x 0.096".

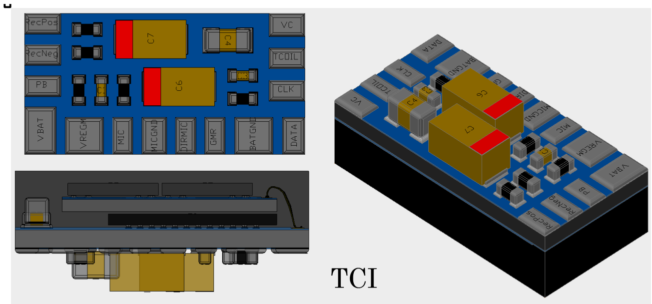

Fig. 9. Custom hearing aid circuit using ultra-low power digital signal processer with two 512K EEPROM die, TCI.

In 2014 the super hybrid was developed. See Fig. 10. This is a custom-built hybrid package that contains three different Si technologies within the same hybrid. It contains the 90 nm ultra-low power digital signal processor in combination with 2Mbit EEPROM storage. A thin film capacitor array sub-module sits within the package and five additional 01005 capacitors rest on the surface. The IPD substrate measures in at 0.008" thick and includes five input capacitors for five analog inputs and a VDBL capacitor. Additionally, 20 vertical interconnects line the peripheral of the package, connecting the top ceramic substrate to the bottom ceramic substrate. The bottom section of the hybrid contains the main substrate, DSP, 01005 capacitors and the vertical interconnections. The top section then contains the capacitor array chip and memory die. Connection is accomplished by 59 RoHS compliant solder bumps, which are intended for flip chip attachment. The line width and spacing of the internal traces are comparable to the flexible circuits also used in hearing aid manufacturing. The final assembly is encapsulated to ensure robustness. The package measured 0.163" x 0.125" x 0.040". The extreme packaging density of this module demonstrates that ceramic hybrids, although an older technology thought to be nearly obsolete, can in fact still lead to a smaller package even with the addition of larger die and additional discrete components.

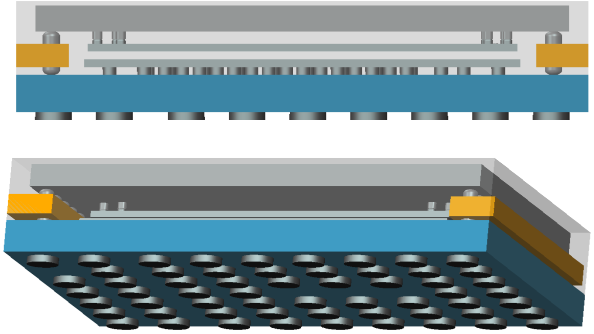

Fig. 10. Starkey's super hybrid, containing DSP, Memory, and IPD.

III. Challenges and Drivers

In the hearing aid business size trumps almost everything. A smaller hearing aid will sell well; a larger hearing aid will not sell in the western world. At the same time, highly creative engineers are accelerating the introduction of new features such as those in the recently released made-for-iPhone hearing aids. Much more is to come. The number of electronic components inside a full-featured hearing aid today is upwards of 75 per device. This is very different from the mainstream hybrid technology of 2008 with only 18 components. While components continue to be added to enable additional features, the size cannot be increased; in fact the trend is decreasing size, as seen in the latest hearing aid style called "invisible in the canal" (IIC).

In addition, there are extreme cost pressures. Even though additional electronic components are being added to enable added features, cost to manufacture must continue to go down since increased price is not really an option.

Each new generation of chips have had more I/O in less space that are driving increased routing density requirements. Complexity is being driven into multi-chip modules and hybrid circuits to delay the need for more expensive circuit boards. So far a lower system cost has been realized to compensate for increased component count.

More complex firmware algorithms are being used and memory size is increasing accordingly. Memory size is doubling on an average every three years, but physical dimensions cannot increase.

IV. Changing ASIC Technologies

Over time, mainstream microprocessor chip technology has continued to drive to smaller dimensions and reduce cost at the same time. Hearing aids use low power chip technology that has progressed at a slower rate. The 2006 low power chips were at the 130 nm node; in 2008 they were at the 90 nm node; in 2014 they are at a 65 nm node; in 2017 we expect to be at a 40 nm node. For the last decade the digital signal processor has dominated hearing aid design. It has been increasingly difficult to scale analog and digital sections to the same extent and the analog section of a digital signal processor is holding back further digital section size reductions. It is expected that single system on a chip (SOC) designs will begin to fade in the same way they are in other electronic business sectors.

Die size has remained relatively constant from 2008 (9 mm^2) to 2017 (10.5 mm^2). A die size shrink has not been realized in moving to new technology nodes because added circuitry has compensated for device shrink. Bump count on die is expected to continue to increase from the 42 bumps in 2008 to the 95 bumps projected for 2020.

V. Chip Metallization

In the early 2000s most chips that were available and of interest to the hearing aid business were available with wire bondable metal surface finish. Because of the low power nature of hearing aids conductive epoxy could be used for electrical connections. Many lessons were learned in developing this technology for hearing aids. Cleanliness of pads was crucial to making a reliable connection. Custom chip designs enabled better leveraging of flip chip solder bump attach. Today, die are commonly available with solder bumps or wire bondable surface finish. Advanced technologies such as embedding are now requiring die (or wafers) with different pad metallurgy such as copper. Future interconnect systems are likely to require gold or copper for thermal compression bonding.

VI. Temperature Hierarchy and RoHS

Hybrids that are intended to be surface mount attached to a circuit board have historically used high-temperature tin/silver solder internally and lower temperature tin/lead solder externally. This enabled surface mount attach without concern over melting the solder used internally to the hybrid circuit. This type of processing continued into 2014 even with the RoHS laws enacted in July of 2006 because of a medical device exemption. In 2014 this exemption was expected to be removed effectively forcing development of alternative approaches. However, a new exemption for class IIa medical devices further extended this exemption to June 30, 2016 for hearing aids.

Today's hybrid manufacturing processes use different non-leaded solders to enact a temperature hierarchy, as well as different underfill and encapsulating materials, more capable of constraining melting solder inside hybrid circuits.

VII. Flip Chip and Stacked Chips

High volume production of "chip-on-flip chip" and "module on flip chip" technologies continues. However, continued use of wire bonding is falling from favor because wire bond loops increase z-axis dimensions in most cases. All new designs are using flip chip technology exclusively.

VIII. Vertical Interconnects

The vertical interconnect technology patented in 1998 continues to be used today [5]. VICs are formed by filling laser drilled holes in 96% alumina substrates with thick film metal paste that is subsequently fired. Typical hole dimensions are 200 μm on a 450 μm pitch [4]. The ceramic is designed wide enough to stretch across saw streets and align to two different circuits at the same time. Subsequent sawing operations separate the VICs. See Figs. 11 and 12. The complex super hybrid described above uses ceramic vertical interconnects to attach an upper interconnect layer with memory and capacitors to the lower ceramic thick film substrate.

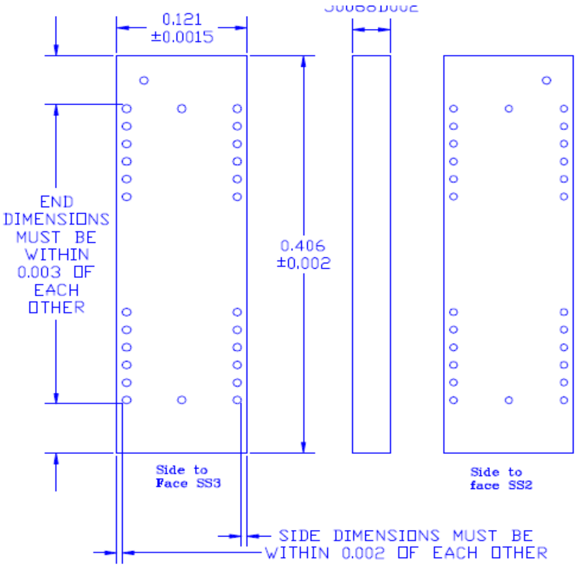

Fig. 11. Example of Starkey's patented vertical interconnect technology.

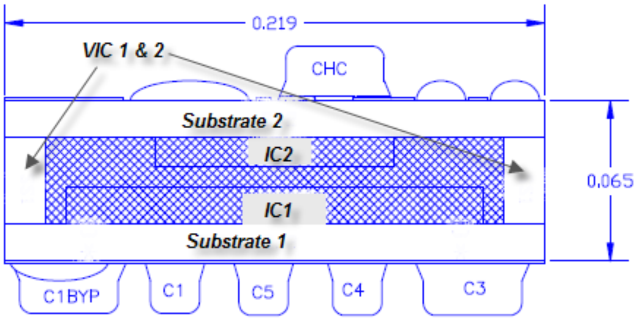

Fig. 12. Side view of vertical interconnects in hybrid.

IX. Integrated Passive Devices

The ability to embed passive components has matured over the past few years. Specifically, in the case where an interposer is necessary, an IPD can offer added capacitance with no size penalty. The transition from the TCI to the super hybrid was able to take advantage of this continuously developing technology. An interposer was necessary to connect the many layers of the super hybrid, and the integrated passive device was an unexpected positive advantage of the interposer's application. In the case of the TCI, the passive components caused an increase in the overall height of the hybrid due to the necessary addition of the spacer and interposer. The integration of the passives into the interposer are a logical evolutionary step in making smaller devices.

X. Materials

The materials used in thick film ceramic hybrids remained relatively unchanged until 2006 with predominantly incremental changes. Because of the RoHS legislation enacted in 2006 many materials had to change.

The introduction of photoimagable thick film dielectrics and metal pastes in the late 2000s enabled increased circuit density. Photoimageable thick film material is exposed with a simple mask aligner and subsequently developed and then fired. 30 μm lines with 40 μm spaces and 75 μm vias are possible. The TCI circuit introduced in 2008 was enabled by use of this type of material. Thick film etchable gold was also introduced in the same timeframe and enabled an alternative path to high interconnect density.

XI. Process Technology Changes

There has been a convergence between industries. Many technologies previously restricted to semiconductor fabrication have been moving to new uses. Photolithographic technology is being used in many areas such as circuit boards. Photoimageble resins are being widely used. Integrated passive devices in silicon use through silicon via technology to produce the equivalent of vertical interconnects, and reduce passive part count. The use of integrated passives in the thick film ceramic is losing traction because of size constraints and routability issues.

XII. Conclusion

Thick film ceramic hybrid circuits have been used for 20 years to make very small hearing aid circuits. This basic technology is still used today although there have been iterative process and technology improvements over time. The convergence of silicon wafer technology and thick film technology has given new life to hybrid circuits. Integrated passive circuits along with chip interconnect in 2D and 2.5D forms are now being used to further increase hybrid routing densities and shrink size. Other forms of multi-chip modules have also evolved over time and are now commonplace making hybrid circuits just one of many forms of multi-chip packaging. Hybrid circuits are being used in combination with flexible circuits to package a portion of the hearing aid circuit while simultaneously minimizing size.

Acknowledgments

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