Propagation Delay Analysis in 3D Stacked Memory using Novel MOS Depletion Layer Modeling Approach for Through Silicon Via

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Abstract

This paper presents the physical level design analysis of 3D stacked memory ICs with Through Silicon Via (TSV) to compute the propagation delay. The difficulties in incorporating TSVs for 3D ICs are that TSV has additional complex parasitics, process based variations, and structure based reliability issues, thus warranting detailed modeling and analysis. TSVs are known to have a MOS structure which has been rigorously studied to evaluate the overall TSV performance and the effect of variable wafer doping profiles has been included in our analysis. Our proposed TSV model provides the IC designer with the yardstick for optimum TSV pitch. Furthermore, our model considers the TSVs to have a variable capacitor which enables frequency selective characteristics based on signal strength and operating frequency. Finally, we have incorporated our model towards optimization of memory array size in 3D stacked DRAMs while taking into account the key factors of TSV delay for a given process node and TSV pitch. This exhaustive analysis would help to choose optimum memory array size while stacking, without degradation in overall 3D Dynamic Random Access Memory (DRAM) performance, and can be effectively used as a primary guideline during memory stacking and layout for optimum bandwidth.

Keywords – *Three-Dimension (3D), Through Silicon Via (TSV), Memory.*

1. Introduction

Rapidly growing complexity in 3D ICs has led to an increase in popularity of test methodologies based on delay testing. 3D IC technology has enabled the semiconductor industry and academia to continue with Moore's law. In present day, there is a tremendous demand for high density memory ICs with large storage capacity and smaller size [1]. To keep in pace with this growing consumer demand in memory with high level of integration 3D memory ICs were developed by stacking memory modules and logic dies with TSVs. 3D stacking of memory is known to reduce the cost of memory and keep up with the cost reduction approach. TSV technology is proposed as a valuable solution to realize 3D ICs. 3D ICs offer the following advantages - (1) low interconnect latency, (2) higher bandwidth, (3) low power consumption and (4) heterogeneous design.

Semiconductor industry has made rapid advancements over the past few decades to dramatically improve the performance of modern electronic systems. The continuous advances in process technology have been able to scale-down transistor sizes and double the transistors per unit area every two years to deliver on 'Moore's Law' for the last 3 decades. However, increasing processor performance did not provide substantial improvement to overall system performance due to memory performance and interconnect bottle-necks between processor-memory interfaces [2]. The performance of the memory system limits the overall system performance, thus attracting heavy research interests towards enhancing memory performance, bandwidth and processor-memory interface.

The concept of clock scaling was intensely studied over a decade back, as it directly controlled the performance and speed of the system. Designers kept improving clock frequencies into GHz ranges, and stopped when clock scaling became harder and reaping overall performance gain became even harder [2]. This caused the designers to turn to other areas for performance gain such as parallelism which resulted in multi-core designs. Eventually the number of cores was limited due to core activity vs. cost benefits [2], forcing the designers to look into memory performance which acts as a major bottle-neck for overall system performance. Designers utilized banked memory arrays connected through high speed interfaces as in conventional DDR DRAMS. However increasing bandwidths have caused processors to be over 100 clock cycles faster than memories [2]. This resulted in memory wall which can be combated using parallel memory by stacking and by using wide input/output memory access [3]. Stacking is done by placing dies in face-to-face or face-to-back configuration. Holes are etched through the wafer, and the filled with conductive metal. The pitch of a TSV has been reportedly reduced to 3µm [4]. The alignment of the wafers plays a crucial role in determining the density of the TSVs, as the alignment error of TSVs with their contact pads poses a minor limitation to the TSV diameter apart from the limitation of aspect ratio to maintain mechanical stability.

In this paper we present a TSV model by analyzing the different performance parameters and compute the propagation delay of 3D stacked memory arrays using TSVs. We use single transistor structure per memory cell for DRAM, thereby enabling greater storage density and keeping it in tandem with the cost reduction approach. The 3D stacked DRAM structure is shown in Fig. 1.

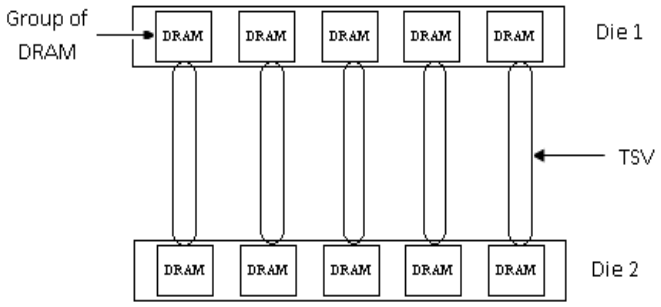

Figure 1: Structure of 3D Stacked DRAM using TSVs.

The paper is organized as follows. Section 2 presents the single transistor DRAM cell architecture and stacking DRAM dies using TSVs. Section 3 describes the proposed MOS depletion layer modeling approach for TSVs by considering the various via parasitics and process effects. Section 4 presents the simulation results for TSVs by varying the TSV dimensions and analyzing the S-parameters, depletion width, and oxide and depletion capacitances. Section 5 discusses the propagation delay in DRAM cells using different DRAM architecture and the overall propagation delay in stacked 3D DRAMs using the MOS depletion layer model for TSVs and finally section 6 concludes the paper.

2. Approach

DRAM has very high storage density and low cost when compared to Static Random Access Memory (SRAM). We use a 1-T DRAM architecture, i.e. each memory cell consists of single transistor and single capacitor, which forms the storage unit. The architecture of 1-T DRAM architecture is shown in Fig. 2.

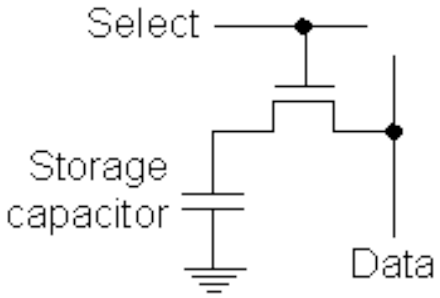

Figure 2: Single Transistor DRAM Cell Architecture.

3D stacking of DRAM cells is achieved by placing DRAM dies one over the other, and connecting a group of DRAM cells to its adjacent group immediately above or below, using vertical Through Silicon Vias. TSV stacking is illustrated in Fig. 3.

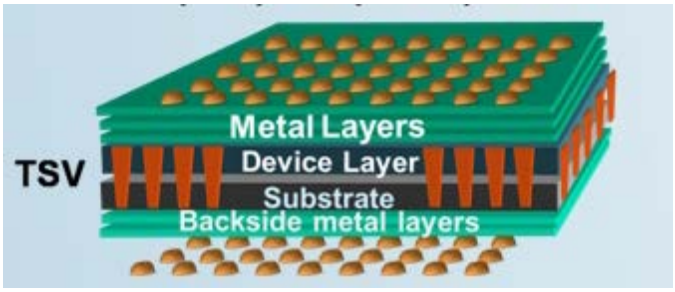

Figure 3: Stacking using TSVs [5].

The optimum group of memory cells to stack using TSVs is computed based on a comparison of propagation delay through surface interconnects using the longest path and that of a stacked configuration using TSV. It is also important to compare the performance vs. memory size as TSVs contribute a significant amount to the overall stacked memory size as TSV area limits the level of granulation from stacking cell-to-cell to stacking a group of cells.

Bonding approach is of three types, (i) wafer-to-wafer bonding, (ii) die-to-wafer bonding, and (iii) die-to-die bonding. Bonding can be done by face-to-face as shown in Fig. 4(a), back-to-face as shown in Fig. 4(b) or back-to-back arrangements. Face refers to the metallic interconnect side of the chip while back refers to the substrate side. After bonding die or wafer thinning is performed. Wafers are typically thinned down to 50µm by grinding and lapping followed by etching and Chemical Mechanical Polishing (CMP). Wafer thinning up-to 6µm has been done [6]. This allows overall TSV height to be less than 10µm allowing face-to-face bonding, in which case, vias are etched through an interposer layer, and is called as a Through-Package-Via (TPV) [7].

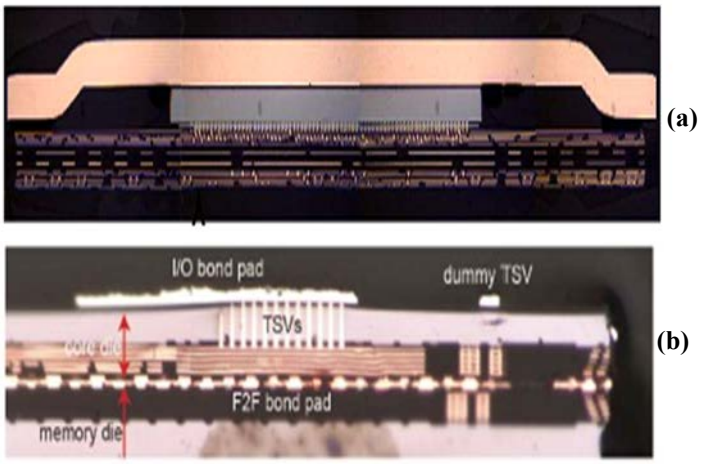

Figure 4: Bonding (a) Face-to-Face stacking using TPV [8], (b) Back-to-Face stacking using TSV [4].

3. Metal Oxide Semiconductor (MOS) TSV Model

TSVs have cylindrical metal-oxide-semiconductors (MOS) structure as shown in the Fig. 5 [9,10]. A copper or tungsten filled metal region, SiO_2 forms the insulating oxide layer and the silicon substrate is doped either n-type or p-type and is biased (usually to ground potential).

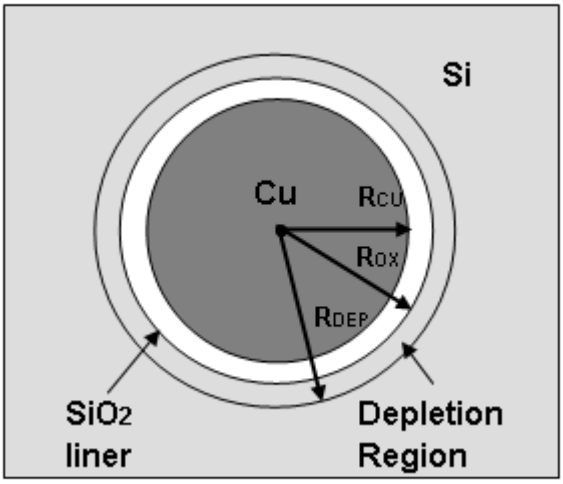

Figure 5: Cross-section of TSV showing MOS Structure [9].

Analytical models of a TSV exclude the formation of depletion region around the oxide layer. This depletion region causes the depletion capacitance to be in series with the oxide capacitance at higher frequencies when the signal level is greater than the intrinsic threshold voltage of the MOS structure thus resulting in lower parasitic capacitance. The analytical model does not take this effect into consideration; hence it overestimates the parasitic capacitance of the TSV

and its propagation delay. The MOS structure model computes the TSV parasitic capacitance by considering the formation of depletion region and inversion regions as shown in Fig. 6.

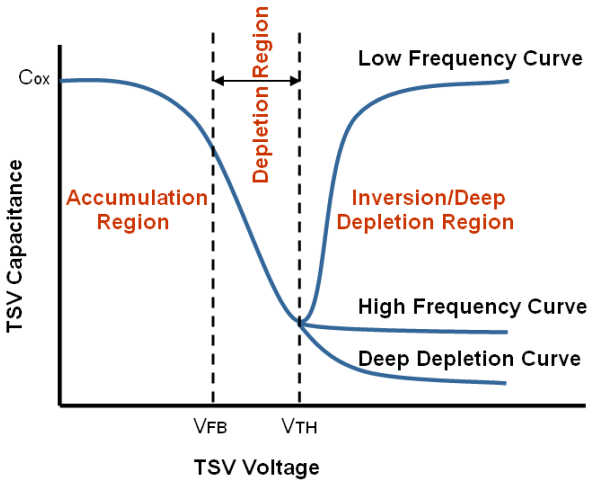

Figure 6: Capacitance vs. Voltage plot of a TSV [9,10].

The electrical field, potential, and charge distribution around the TSV is obtained by solving the Poisson's equation in cylindrical coordinates. The Si substrate is assumed to be biased at ground potential and the TSV voltage is expressed as,

$$V_{TSV} = \frac{Q_{TSV}}{C_{ox}} + V_{FB} + \varphi_S \tag{1}$$

where, Q_{TSV} is the charge on the TSV, C_{ox} is the SiO_2 liner capacitance, V_{FB} the flat band voltage obtained from the energy band-gap as shown in Fig. 7 and φ_s is the surface potential at the Si-SiO_2 interface.

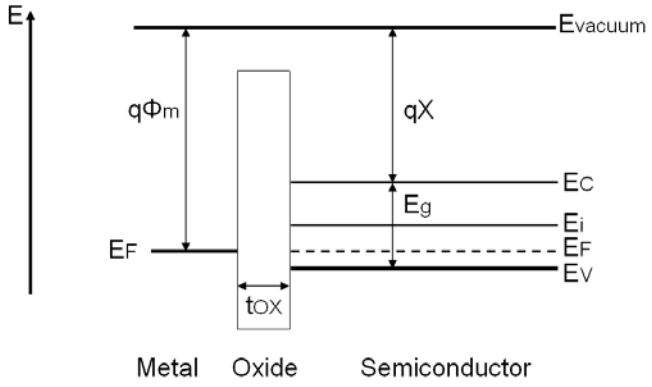

Figure 7: Energy band diagram of MOS junction with p-type semiconductor [11,12]

The flat band voltage is given by,

$$V_{FB} = \varphi_M - \varphi_{Si} = \varphi_M - \chi - \frac{E_g}{2q} - \varphi_t \ln\frac{N_a}{n_i} \tag{2}$$

where, φ_M is the work-function of the TiN barrier layer, and φ_{Si} is the work-function of silicon. χ is the electron affinity of silicon, E_g the band energy gap, q the electronic charge, N_a the doping concentration of acceptor ions, and n_i is the intrinsic carrier concentration of silicon. Poisson's equation in cylindrical coordinates is given by,

$$\frac{d^2\phi}{dr^2} + \frac{1}{r}\frac{d\phi}{dr} = -\frac{\rho}{\varepsilon_s} \tag{3}$$

where, φ and ρ are the surface potential and charge density a radius r from the center of the TSV and ε_S is the permittivity of silicon. The Poisson's equation in cylindrical coordinates is solved by assuming the depletion layer charge to be entirely due to ionized acceptor atoms which is given by,

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\varphi}{dr}\right) = \frac{qN_a}{\varepsilon_S} \tag{4}$$

The potential and electric field at the edge of depletion region ($r = r_5$) is zero. Integrating (4) from r_4 to r_5, and substituting (3) we obtain,

$$\varphi_S = \frac{qN_a}{2\varepsilon_S}\left(r_5^2 \ln\frac{r_5}{r_4} - \frac{r_5^2 - r_4^2}{2}\right) \tag{5}$$

The charge in the metal, Q_{TSV}, is equal to the charge in the depletion region,

$$Q_{TSV} = qN_a\pi(r_5^2 - r_4^2) \tag{6}$$

Substituting (2), (5) and (6) in (1), we obtain,

$$V_{TSV} = \phi_M - \chi - \frac{E_g}{2q} - \phi_t \ln\frac{Na}{n_i} + \frac{qNa}{2\varepsilon_S}\left(r_5^2 \ln\frac{r_5}{r_4} - \frac{r_5^2 - r_4^2}{2}\right) + \frac{qNa(r_5^2 - r_4^2)}{2\varepsilon_{ox}}\ln\frac{r_4}{r_3} \tag{7}$$

The radius of the depletion region r_5 is calculated by solving (7) iteratively. The depletion capacitance is calculated by,

$$C_{dep} = \frac{2\pi\varepsilon_S L}{\ln\frac{r_5}{r_4}} \tag{8}$$

The total TSV capacitance is given by,

$$\frac{1}{C_{TSV}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} \tag{9}$$

3.1. Process-Effect – Via Tapering

Previous TSV models assume the via to be cylindrical in shape, having a fixed via diameter. However, the process used for etching (DRIE or Plasma etching) introduce a tapering effect in the via, wherein the via sidewalls taper at 60 to 92 degrees which depends on the etchant and coil power [13,14]. This tapering effect causes a continuous reduction in via diameter as we progress the depth of the via. This change in via diameter is calculated by Pythagoras theorem as shown in Fig. 8.

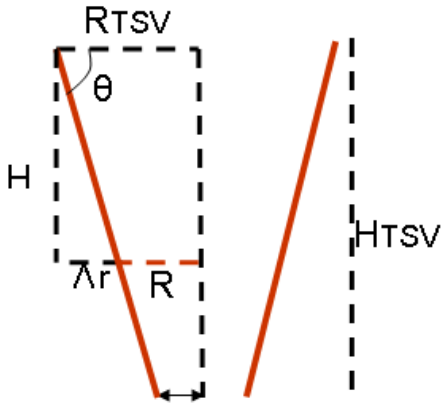

Figure 8: Geometry of Via Tapering Effect.

where, H_{TSV} is the height of the TSV, θ is the tapering angle, and Δr is the change in via radius. The radius at a particular depth of the via is a function of tapering angle as given below,

$$R_X = R_{TSV} - \frac{H_X}{\tan\theta} \tag{10}$$

where, R_X is the radius of the via at depth of H_X.

3.2. Process Effect – Via Scalloping

TSVs are fabricated using DRIE or plasma etching, which involves repeated etch and passivation cycles that gives rise to scalloping on the TSV structure. The scalloping error varies from 150 nm to 650 nm depending on the etch rate and TSV diameter.

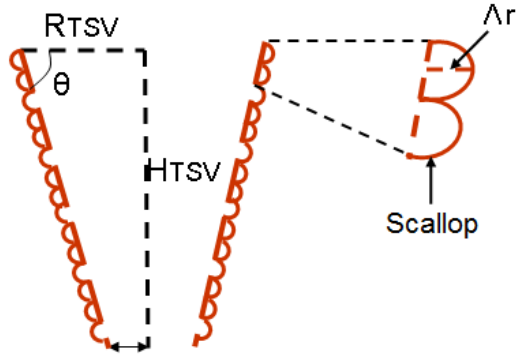

Figure 9: Geometry of Via Scalloping Effect.

where, Δr is the scalloping error is modeled depending on TSV depth, and varies from 0 to 150 nm.

$$\Delta r = f(Hx) \tag{11}$$

$$R^1_X = R_X + \Delta r \tag{12}$$

where, R^1_X is the radius of the TSV considering the tapering and scalloping process effects, at via depth of H_X.

3.3. TSV Resistance

The parasitic resistance of a TSV depends on the height, diameter of the TSV and conducting material. It is to be noted that skin depth can raise the overall resistance of a TSV by decreasing the effective area of TSV metal used for conduction. Skin depth generally occurs at higher frequencies. The DC resistance of a TSV is given by,

$$R_{TSV\_DC} = \frac{\rho H_{TSV}}{\pi R^2_{TSV}} \tag{13}$$

where ρ is the resistivity of the conducting material in TSV, H_{TSV} is the height of the TSV and R_{TSV} is the radius of the TSV.

The resistance due to skin effect at high frequencies, is a function of the DC resistance and frequency of operation [15], and is given by,

$$R_{TSV\_AC} = R_{TSV\_DC}\sqrt{1+\frac{f}{10^{10}}} \tag{14}$$

where, f is the frequency of operation.

The tapering effect and scalloping error caused by process factors, changes the TSV radius along the height of the TSV. The following table considers two cases with 89 degrees process tapering angle and 350 nm, 650 nm scalloping errors for 2μm and 5μm TSV diameters respectively.

Table 1: TSV Resistance – Analytical Computation vs. Measured Value.

TSV Length	TSV Diameter	Measured Resistance [10]	TSV Resistance (MOS Model)	% Deviation
20 μm	2 μm	119.254 mΩ	119.3 mΩ	0.039
50 μm	5 μm	44.961 mΩ	44.86 mΩ	0.225

Table 1 shows a comparison of TSV resistance computed analytically with the measured value [10], the analytical model shows good agreement with measured results.

3.4. TSV Inductance

The self-inductance of a TSV depends on the height and diameter of the TSV and is given by,

$$L_{TSV} = \frac{\mu_0}{4\pi}\left[2H_{TSV}\ln\left(\frac{2H_{TSV}+\sqrt{R^2_{TSV}+(2H_{TSV})^2}}{R_{TSV}}\right) + \left(R_{TSV}-\sqrt{R^2_{TSV}+(2H_{TSV})^2}\right)\right] \tag{15}$$

where, μ_0 is the magnetic permeability of free space given by $4\pi \times 10^{-7}$ Hm^{-1}. Table 2 shows the comparison of TSV self-inductances between previous analytical models [10] and our current MOS modeling approach that includes process variations.

Table 2: TSV Inductance – Analytical computation vs. Measured Value.

TSV Length	TSV Diameter	Measured Inductance [10]	TSV Inductance (MOS Model)	% Deviation
20 μm	2 μm	13.827 pH	14.469 pH	4.643
50 μm	5 μm	34.262 pH	35.672 pH	4.115

From Table 4, it is observed that the tapering and scalloping effects have resulted in an increase in the self-

inductance of a TSV. However, in general the TSV inductance is ignored at lower frequencies wherein the inductive impedance $X_L = \omega L$ is less than the parasitic resistance of the TSV (R_{TSV_AC}). This relation holds good for frequencies below f_0 (~1.5 GHz), where, f_0 varies with the height and diameter of the TSV.

4. Simulation Results

TSVs modeled using MOS depletion layer approach is used to perform simulations. Performing simulations gives us the TSV performance characteristics alone but optimization of performance is another key area to be focused upon when TSVs are used in 3D IC applications. Varying the TSV dimensions, insulating layer thickness and material and doping the substrate can greatly reduce the TSV parasitics thereby providing much improved and reduced propagation delay. We have performed a variety of variations to understand the relation between TSV parasitics and TSV structure.

4.1 Variation of TSV Height

When multiple dies are stacked using TSVs, then the first two dies at the top are connected face-to-face while the subsequent dies are connected in face-to-back configuration. The height of the TSV depends on the thickness of the device layer, and wafer thickness. The wafers have been thinned down to 6 µm [6]. The TSV height can vary anywhere between 5 µm to 100 µm for face-to-back stacking of multiple tiers. We considered a TSV with a diameter of 2 µm varied the height from 5µm to 20µm. A silicon-dioxide layer of 50 nm thickness is considered, with via tapering angle of 89 degrees and scalloping error of 350 nm is considered.

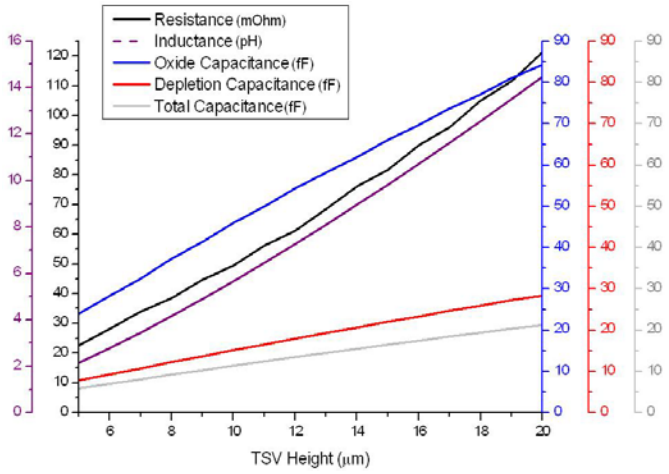

Figure 10: Variation of TSV Parasitics with TSV Height for Face-to-Back Stacking.

The TSV parasitics increase with the TSV height and the overall TSV capacitance is much lower due to the depletion capacitance. For this case we considered the depletion width to be 1 µm.

4.2 Variation of TSV Diameter

The diameter of a TSV is restricted by alignment errors [6] and increasing resistance for small aspect ratio vias. Typical TSVs have diameter ranging from 5 µm to 50 µm. The ITRS roadmap for TSV predicts a TSV dimension of 1 µm diameter and 10 µm height by the year 2015. This necessitates processes, tools, electrical models and testability to prove their accuracy and efficiency at sub-micron levels. We have considered a TSV of length 10 µm with diameters varied from 0.5 µm to 2 µm. The TSV fabrication involves selecting the oxide thickness in proportion to the TSV diameter. However, we assume the oxide thickness as 50 nm, to understand the lone impact of TSV diameter on its parasitics.

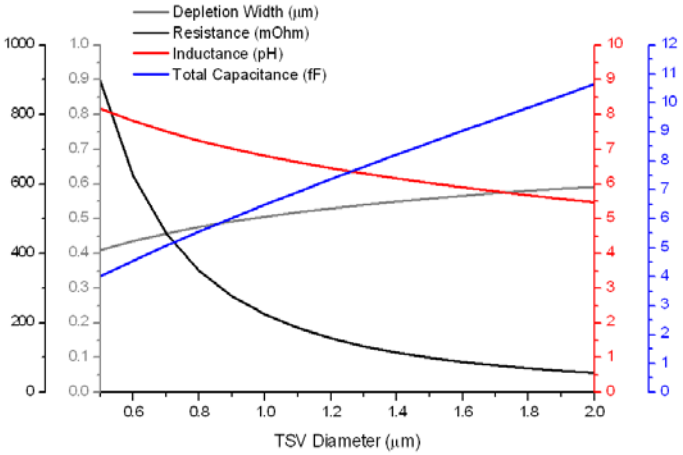

Figure 11: Variation of TSV Parasitics and Depletion Width with TSV Diameter.

The resistance of a TSV decreases exponentially with increase in TSV diameter; it is 1 Ω for TSV diameters below 0.5 µm and reduces to 62 mΩ at 2µm. The capacitance increases with increase in the TSV diameter unlike resistance and inductance parasitics from 5 fF to 11 fF. From Fig. 11, we can conclude that reducing of TSV diameter will increase the TSV resistance and thereby increase the propagation delay through the TSV. The scope for improvement is in material properties and reduction of parasitic capacitance.

4.3 Variation of Insulating Oxide Thickness

To reduce the capacitance of a TSV we can increase the thickness of the oxide insulator around the TSV. In this case, we have assumed a TSV with height of 10 µm, diameter of 2 µm, and oxide thickness is varied between 20 nm to 150 nm. In typical TSV fabrication, the oxide thickness varies with the diameter of the TSV. We have assumed the TSV diameter to be constant at 2µm, to observe the dependence of TSV capacitance over oxide thickness.

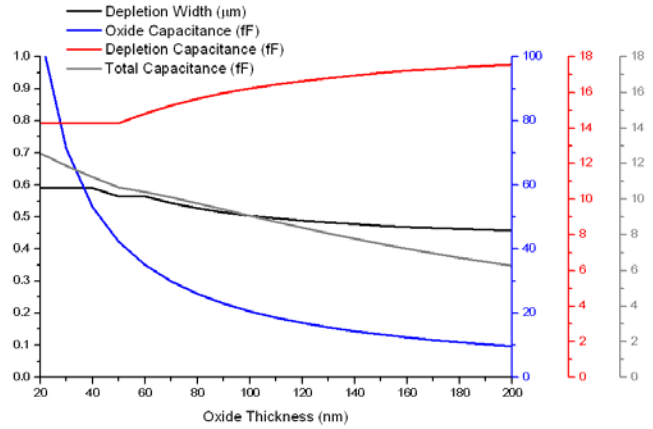

Figure 12: Variation of TSV Capacitance and Depletion Width with Oxide Thickness for K = 3.9 (SiO2).

From Fig. 12 it is seen that by increasing the oxide thickness causes the oxide capacitance to decrease, and thereby reduce the overall TSV capacitance, and propagation delay through TSV. It can be observed that the TSV capacitance value decreases from 12 fF to 6 fF as the oxide thickness varies from 20 nm to 200nm. Although this might seem advantageous, the process time involved in the deposition of the oxide layer by CVD process increases resulting in high fabrication cost.

4.4 Variation of Insulating Material

Reduction in TSV capacitance, while also reducing oxide thickness is achieved by changing the dielectric insulator between the TSV and silicon substrate. Lower dielectric insulators such as polymer or BCB are used to reduce the K value from 3.9 for silicon dioxide to 2.2 for BCB. At high operating frequencies, polymer insulators are preferred over silicon dioxide to reduce the parasitic losses.

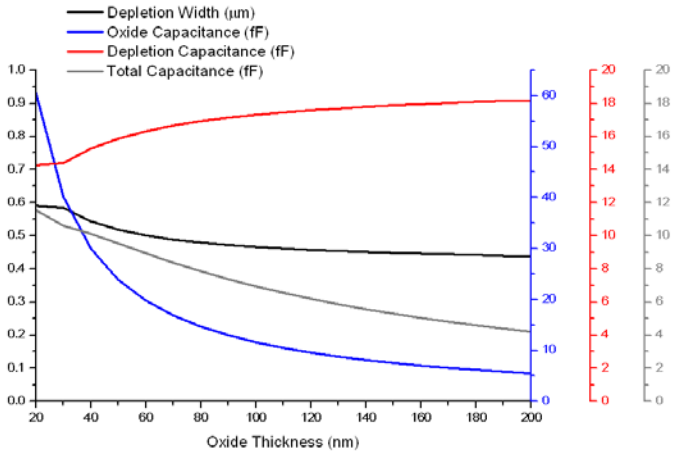

Figure 13: Variation of TSV Capacitance and Depletion Width with Oxide Thickness for K = 2.2 (polymer).

Fig. 13 shows the TSV capacitance vs. insulator thickness for a BCB insulating layer with K = 2.2. The effect of the reducing the dielectric constant is that the oxide thickness can be reduced proportionally while maintaining the TSV capacitance as a constant.

4.5 Variation of Substrate Doping Concentration

The substrate can be doped with acceptor ions to form a p-type semiconductor. The doping profile of the silicon substrate controls the width of the depletion region formed in the substrate and hence controls the threshold voltage, TSV capacitance and propagation delay through a TSV. We consider below change in doping concentration from $1x10^{13}$ to $1x10^{18}$ cm^{-3}.

It is observed from Fig. 14 that, the increase in acceptor ion concentration of the substrate increases the TSV capacitance while reducing the depletion width. Reduced depletion width, helps in reducing the overall pitch of the TSV, and hence improve the stacking density, while reducing capacitance reduces the propagation delay, providing lower losses and better speed. Thus the doping concentration is selected as a trade-off over TSV capacitance and depletion width. The region of $2x10^{14}$ to $1x10^{15}$ cm^{-3} offers an optimum range where the TSV capacitance is near 6 fF while depletion width is around 1 µm.

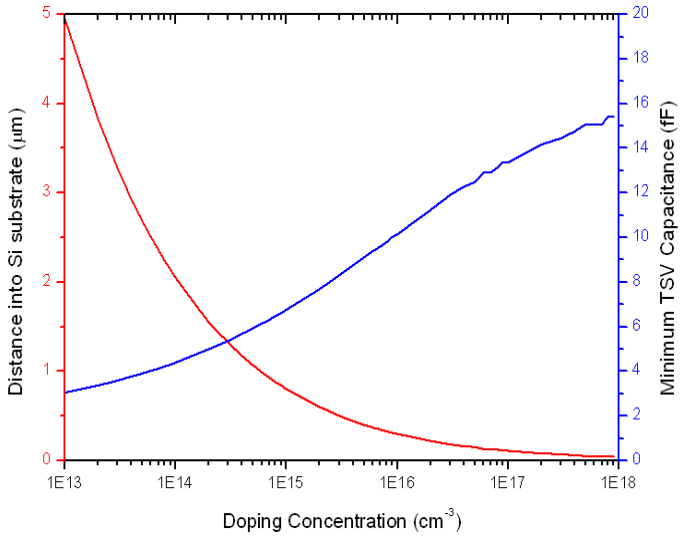

Figure 14: Variation of TSV Capacitance and Depletion Width with Substrate Doping Concentration.

4.6 S-Parameter Analysis

TSV with 10µm height and 2µm diameter is electrically modeled using the TSV model discussed in Section 3 that includes the process variations and MOS depletion effects. The model consists of lumped elements of TSV resistance, self-inductance and capacitance. S-Parameter simulation was performed to observe the performance characteristics of TSV at different operating frequencies. The S-parameter results are shown in Fig. 15.

The input port reflection loss (S_{11}) is extremely less for TSVs and varies from -65.2 dB at 100 MHz to -63.2 dB at 500 MHz when process and MOS depletion layer effects are considered. Whereas the TSV model in previously published research [9,10] yields an input port reflection of -63.6 dB at 500 MHz. The insertion loss (S_{12}) is constant around -0.0047 dB across the frequency range. The process related effects results in a 0.4dB loss as compared to earlier TSV models.

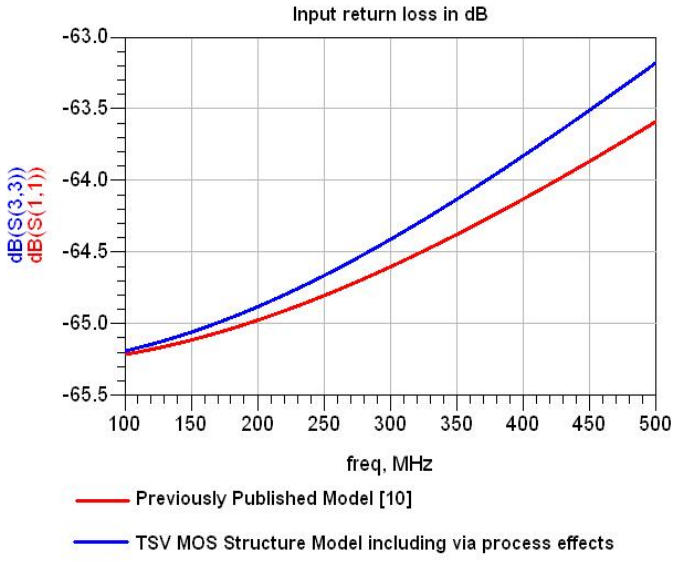

Figure 15: S-Parameter Simulation – Input Port Return Loss for a TSV.

5. Propagation Delay

The propagation delay between two DRAM cells is computed by considering the switching action of transistor and the loading effects. The propagation delay in transistor is given by the following equations [16,17],

$$t_1 = \left[F_0(C\pi) + C_0 + F_0 C_W\right]\left(V_{OH} - V_{TH}\right)/I_{\max} - pulldown \quad (16)$$

$$t_2 = \left[F_0(C\pi + C_w)\right]\left(V_{TL} - V_{OL}\right)/I_{\max} - pullup \quad (17)$$

where, t_1 and t_2 are the transition times during pull up and pull down respectively. F_0 is the fan-out number and C_0 is the transistor diffusion capacitance.

The total transition delay time is one DRAM cell is given by,

$$t_T = t_1 + t_2 \quad (18)$$

And, the propagation delay in one DRAM cell is given by,

$$t_{pd} = t_T + \left(\frac{C_T \Delta V}{2I_d\left(\Delta V/2\right)}\right) \quad (19)$$

where, C_T is the load capacitance between two DRAM cells and I_d is the current across the inverter at logic threshold. The propagation delay in DRAM cells for different architectures is presented below in Table 3.

Table 3: DRAM Propagation Delay.

DRAM Architecture	2xDRAM	4xDRAM	8XDRAM
Transition Time (t1)	169.598 ns	339.196 ns	678.392 ns
Transition Time (t2)	127.548 ns	255.096 ns	510.192 ns
Total Transition Delay Time (tT)	297.146 ns	594.292 ns	1.118 µs
Total Propagation Delay Time (tpd)	332.148 ns	664.296 ns	1.328 µs

Table 3 shows the propagation delay in one single DRAM die. If these DRAM dies are stacked together then the total propagation delay includes the delay due to TSVs. We have considered the stacked TSVs to vary from 3 to 5 dies for these three different DRAM architectures. The TSV has a height of 15 µm, diameter of 3 µm and pitch of 6 µm. The TSV is modeled using the TSV MOS structure model which results in propagation delay of 0.88 ns. The overall propagation delay of stacked DRAM using TSVs is presented in Table 4.

Table 4: Stacked DRAM Propagation Delay.

DRAM Architecture	2xDRAM	4xDRAM	8xDRAM
Single die	332.148 ns	664.296 ns	1.328 µs
3 die stack	334.788 ns	666.936 ns	1.33 µs
4 die stack	335.668 ns	667.816 ns	1.331 µs
5 die stack	336.548 ns	668.696 ns	1.332 µs

Table 4 shows the overall propagation delay in stacked DRAM using TSVs. The propagation delay increases with the increase in the number of stacked dies for 2xDRAM and 4xDRAM architectures, but for 8xDRAM architecture the propagation delay remains constant. Hence if we use more DRAM cells per die we can stack more dies keeping the overall propagation delay constant.

6. Conclusion

This paper presented a novel TSV model using the MOS depletion layer approach. Various TSV parasitics and process effects such as tapering and scalloping were considered in the model. The TSV model was validated against previously published data. The paper also presented simulation results by varying various TSV dimensions and process parameters to optimize the TSV performance characteristics. S-parameter simulation was performed for optimized TSV modeled using the MOS approach with and without via process effects. Stacked memory was discussed to implement the TSV model to determine the propagation delay in stacked 3D DRAM ICs. This provides an exhaustive and conclusive analysis about TSV performance and propagation delay in TSVs which can be used for designing 3D stacked DRAM ICs.

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