FOWLP Technology eWLB – Enabler for Packaging of IoT/IoE Modules

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Abstract

The next big wave, the Internet of Things or Internet of Everything (IoT/IoE) is on the way. What does that mean for semiconductor packaging, assembly and test? What are the requirements? What solutions can be provided? The market will be wide and fragmented. Many different solutions will be needed. Flexibility and the capability to customize system solutions will be crucial. The fact is, it will be all about smart system integration, integration of sensors, MEMS, connectivity and memory: more functionality on less space in small and thin System-in-Package (SiP) and Package-on-Package (PoP). There will not be one specific packaging technology for IoT/IoE, and no new "IoT/IoE Packaging Technology". The toolbox is here already, and further features required to meet the needs of future IoT/IoE modules are under development. That is actually good news, as the cost pressure will be high, and materialization of existing manufacturing environment, of mature and yielding packaging technologies will be a key for success.

Key words

Electromagnetic and thermal package performance, FOWLP, eWLB technology, miniaturization, packaging for IoT/IoE, dense system integration, WLFO, WLSiP, WL3D, WLPoP, sensor packaging, KOZ

I. Introduction

A promising packaging technology suitable for upcoming IoT/IoE applications, namely in the segment of wearable electronics, are the various substrate-less Fan-Out Wafer- and Panel-Level Packaging technologies developed during the last decade. Great potential, a $200M Fan-Out Wafer-Level Packaging (FOWLP) market in 2015, and 30% CAGR in the coming years is forecasted [1]. This growth can also be explained by the wide design flexibility and system integration capability of the Fan-Out Wafer- and Panel-Level Packaging technologies, providing a small and thin package performing as active interposer. A deeper look into the various potential semi-conductor applications for IoT/IoE devices and packaging requirements for those are discussed in [2] and [3].

For modules with needs to integrate mobile communication and to achieve dense system integration while a high level of miniaturization is required, the eWLB (embedded Wafer-Level Ball grid Array) technology shows the highest capability to fulfill those. eWLB is the leading FOWLP proven in high volume manufacturing. It is currently based on 300mm round panel/ wafer format and comprises reconstitution, where know good dies from same or different grinded and diced incoming wafers are face-down placed on tape on a temporary mold carrier, wafer molding to create a new reconstituted round panel/ wafer, redistribution of the pads by vias and traces applying thin-film technology, and finally the solder ball attach, marking and package singulation. Component test can be performed efficiently in round panel/ wafer format using a wafer prober, as the package singulation process after component test does not represent any risk for component functionality. The desired technology features and technology bricks for miniaturized system integration are either available in the eWLB tool box already today or in development.

Already developed eWLB based 2D constructions like WLSiP (Wafer-Level System-in-Package) with embedded active multi-die, discrete passives, already packaged components, sensors and also optical elements, and eWLB based 3D constructions like WLPoP (Wafer-Level Package-on-Package) can achieve the highest integration density. First products are qualified and ready for volume production.

Thin reconstituted wafer handling, Thru Package Vias (TPV) and backside thin-film RDL processing solutions as enablers for thin eWLB based WLSiP and for thin eWLB acting as bottom package of eWLB based WL3D/ WLPoP are essential building blocks for the required miniaturization of IoT/IoE modules. Its development is in the hot phase.

The eWLB has very short connections between die pads and package I/Os. This results in extremely low package parasitic values, especially in terms of inductance, and a good matching network, allowing for high frequency applications with superior electrical performance and low loss.

Thermal performance is getting more and more important as there will be more power consuming and heat dissipating functionality integrated on less and less space. Package designers and technologists have to invent effective methods to get the heat out of the system, avoid hot spots and dissipate heat in the system to places where it does not harm or can be dissipated into the environment. Chip-Package-Board co-design is essential to solve this system task.

II. System Integration in eWLB based WLSiP

A. Toolbox and technology bricks

The eWLB technology is still a young technology with high potential for further developments widening its application fields. The tool box is continuously increasing. New technology bricks are developed and qualified. Majority of the work is currently done to enable system integration features allowing for high density integration:

- Finer line/ space width,
- Multi-Layer RDL routing (Fig.1),
- Multi-Die and discrete passives placement with smaller distances in between (Fig.2 and Fig.3).

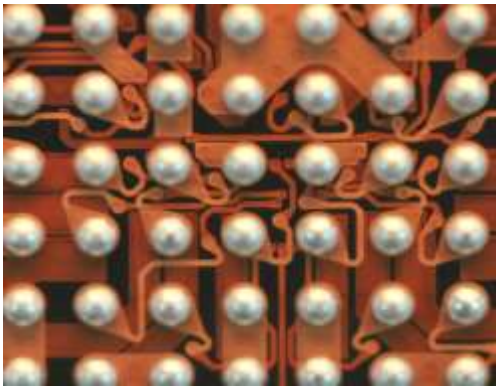

Figure 1 - Example of a multi-layer RDL of eWLB package

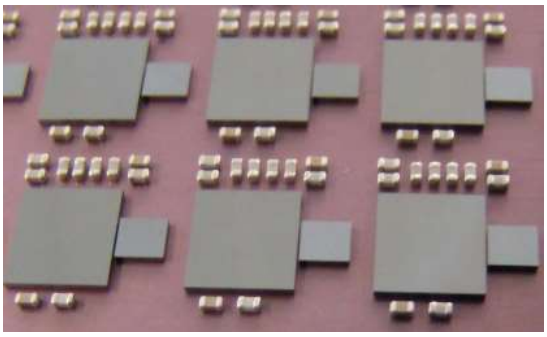

Figure 2 - WLSiP configuration with 2 active dies and 10 discrete passives placed active side face-down on recon wafer carrier before wafer molding

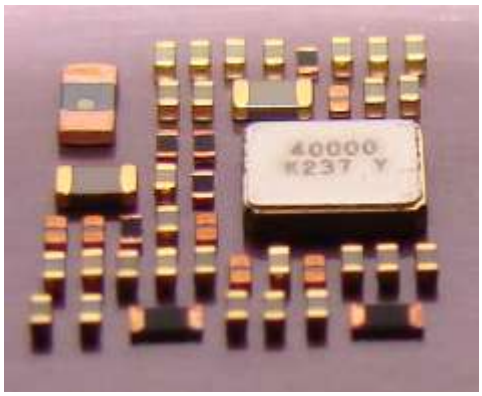

Figure 3 - WLSiP configuration with 40+ elements placed on recon wafer carrier before wafer molding (8.1x8.1mm² package replacing current 5x larger PCB based solution)

Those design features and further development of the technology to reach smaller line/ space width towards 2um/2um, multi-layer RDL with up to 4 metal layers, smaller distance between active dies towards 50um, between discrete passive towards 100um and others will allow for efficient system integration for SiP modules on very small space. Fig.4 shows an example of such SiP module representing a quite complete configuration for:

- Secure sensing by integrated sensor,
- Raw data Storage,
- Analyze and make it meaningful data,
- Securing data to be transmitted,
- Sending data,
- Receiving data,
- Acting with actuator.

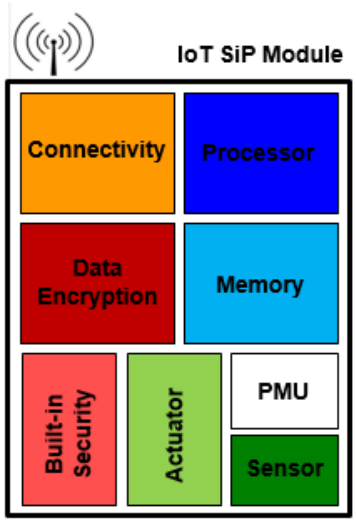

Figure 4 - Example of an IoT/IoE System-in-Package module with a wide range of functionality integrated

Talking about sensor and MEMS integration in eWLB based WLSiP with its overmold and thin-film process steps, it becomes obvious that sensitive areas need to be protected during processing and released safely and clean after processing. The development of the technology brick "Keep-Out Zones" (KOZ) becomes an essential element in the toolbox. This is currently investigated by a wider consortium of industry partners, institutes and academic in European ENIAC Joint Undertaking project "Processes for MEMS by Inkjet Enhanced Technologies" (Prominent). Fig.5 shows an example of a pressure sensor with sensitive membrane integrated together with an ASIC die in eWLB based WLSiP.

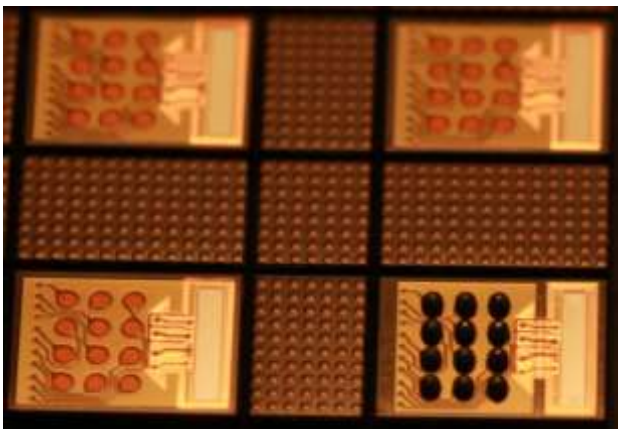

Figure 5 - Pressure sensor with sensitive membrane integrated together with an ASIC die in eWLB based WLSiP

B. System-in-Package reliability

The reliability of such eWLB based WLSiP systems has been proven in stress tests and readouts done with Daisy Chain dies and with functional components focusing on board level behavior for mobile devices. Temperature cycling on board (TCoB) following IPC9701 specification (condition TC2 temperature profile -25degC/ +100degC, 1 cy/h) showed first fail after 900x.

Drop Test (DT) following JESD22-B111 specification showed first fail at 30 drops. The Weibull distribution is shown in Fig.6. The fails occurred mainly at outer BGA ball rows. Improvement has been achieved through the introduction of a DT optimized solder ball alloy.

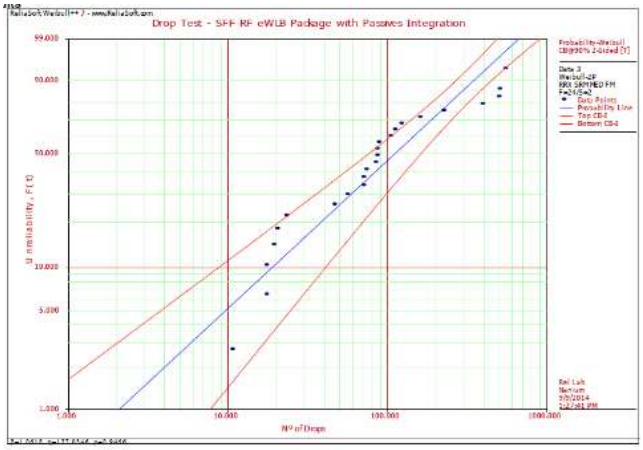

Figure 6 - First DT results of a WLSiP for wearables

Package size and stand-off, solderballs alloy and internal stress caused dynamic warpage behavior of the package are impacting especially Board Level Reliability (BLR). Besides that, the complexity of the component (e.g. WLPoP with 2 or 3 levels, interconnects between the levels, embedded element versus moldcompound ratio per level) has significant impact on the reliability achievable. Further investigations are ongoing to better classify this capability for different constructions.

III. Thin Package and WL3D / WLPoP

Challenges moving eWLB based FOWLP into 3D includes the development of vertical interconnections (Thru Package Vias, TPV) from the re-distribution layer (RDL) on the package frontside (BGA side) to the package backside, and the development of solder land pads or even a full RDL on the package backside to allow component assembly on the backside of the bottom package, forming the WLPoP. Fig.7 shows the relevant section of the NANIUM package offer.

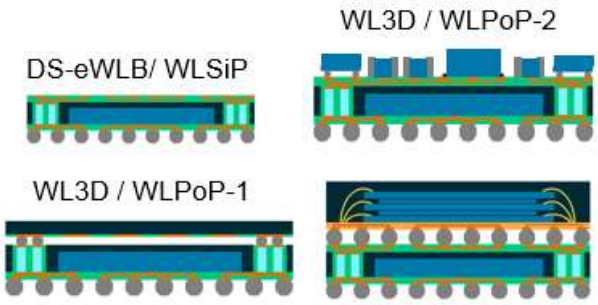

Figure 7 - NANIUM package offer for eWLB based Fan-Out WLP solutions WLSiP and WLPoP with double sided (DS) redistribution layer or land pads connected by TPV

Vertical interconnections developed or being developed for FOWLP are either "post-formed" Thru Mold Vias (TMV) or different kinds of "pre-formed" vias. TMV require capability for fast and accurate via drilling in the moldcompound by laser ablation. Implementation of connections in vias drilled in moldcompound is the major challenge and a significant cost factor. Although the via side walls can be done with inclination favoring the deposition of material layers, the filling of vias with rough sidewalls resulting from mold filler is still critical. Traditional adhesion/ seed layer deposition techniques such as PVD or CVD and electroplating to fill the vias have difficulties achieving the required layer thickness and homogeneity, depending on diameter and depth of the vias. To overcome this, electro-less plating seems to be a good alternative. However, the number of process steps is high and impact on unit cost significant.

The alternative to post-formed vias are pre-formed vias. Its application requires the selection of the right material and suitable format for accurate placement on the mold carrier during reconstitution process and sufficient position stability during the mold process. The modulus of the material is critical for the pick and place of via elements. Other material characteristics namely the CTE and Tg of the pre-formed via element have to be matched to the surrounding moldcompound. Finally, all materials and interfaces between materials in the package impact package reliability and, therefore, need to be understood and controlled.

NANIUM is focusing on the development of pre-formed vias in the format of PCB-bars (small pieces of organic laminated substrate/ printed circuit board with a matrix of vias processed at substrate/ printed circuit board supplier) placed in the reconstituted round panel/ wafer before molding in order to make the vertical connection between front- and backside RDL layers or just backside contact pads of the package. The developed pre-formed vias are visible in Fig.8.

The arrangement of active dies, discrete passives and other elements inside the product is hidden for confidentiality reasons. PCB-bars are containing a certain number of vias in an arrangement, following the specific product requirements. Here a relaxed 400um pitch and 250um via diameter was applied. During the reconstitution process, PCB-bars are placed on the mold carrier together with the active dies and passives. After molding and frontside RDL processing, the metal pads at the package backside are exposed and establish the connections from the RDL on the package frontside to the package backside. A WLPoP applying this TPV technology with 3 functional levels including a "Hanging Die" (Flip-Chip placed underneath the package between the BGA's and connected to the frontside RDL of the package) is shown in Fig.9.

Figure 8 - WLSiP configuration with Thru Package Via bars for thin WLPoP bottom package placed on recon wafer carrier before wafer molding

Figure 9 - Final WL3D / WLPoP-1 configuration with 3 levels of functionality (2x eWLB based WLSiP stacked, and 1x "Hanging Die" Flip-Chip assembled in ball grid array)

If the total package height of a WL3D/ WLPoP has to be very thin, such as below 1mm or even below 0.8mm for the mobile market, the thickness of the individual levels of the WLPoP have to be in the range of 200-300um only. Especially the eWLB bottom package with the Thru Package Vias (TPV) contacts has to be thin, and that is the one which needs to be processed at both sides. After processing the

frontside of the recon wafer it has to be thinned to achieve the final thickness and reveal the TPV before processing the backside in the thin-film process line. As thin 300mm recon wafers are not stable enough to be handled as such, temporary bonding of recon wafers was developed successfully, supported by the project Enhanced Power Pilot Line (EPPL), partially funded by EU and national grants under the ENIAC program [4].

Temporary bonding of Si wafers, thinning and processing the Si wafer while sitting on the temporary carrier, and finally de-bonding the wafer as shown in Fig.10 is an established process in the industry.

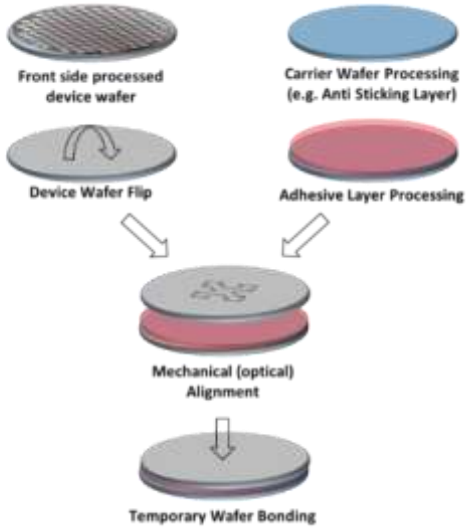

Figure 10 - Generic Temporary Bonding Process Flow for multilayer adhesives (Source: EV Group, 2012)

But eWLB recon wafer are plastic wafers with embedded elements in different configurations for each product. Consequently, the recon wafer behaves very differently than the Si wafer. In a set of experiments different major parameters were tested, like carrier materials and thicknesses, adhesive materials and temporary bonding process conditions. The results showed the significant impact coming from both adhesives and carrier properties on the bond quality and on the ability to withstand the very aggressive thin-film processing for FOWLP. Based on the different results obtained during the multiple experiments, typical carrier materials were shown to be inadequate and new carrier materials, together with the most suitable temporary bonding adhesive and process conditions, demonstrated the existence of an optimal solution. After a careful selection, the best combination of such parameters enabled a robust temporary bonding solution for FOWLP. The data are proprietary and cannot be disclosed. However, no visual or internal abnormality was seen on the optimized configuration as well as only minimum wafer warpage was measured during FOWLP critical process steps [4].

IV. Electromagnetic and Thermal Performance

A driving force and significant advantage of FOWLP and eWLB in particular is the superior electromagnetic and thermal performance of the package compared to similar package types allowing similar levels of dense system integration.

A. Electromagnetic Performance

Due to the very low package parasitics compared to laminate substrate or lead-frame based packages, eWLB offers excellent RF performance. This is the result of the very short signal path length between chip, package, and board, as made visible in Fig.11. Applicability of the eWLB package is proven in high volume for high frequency applications. It became a standard package for RF/ Baseband SoC in mobile communication market [1] and is taking over market share for automotive and non-automotive radar applications such as the 77GHz module from Infineon Technologies AG [5]. Higher frequencies up to 80GHz for millimeter wave radar applications have been demonstrated, and feasibility of the packaging solution up to 120GHz are under investigation.

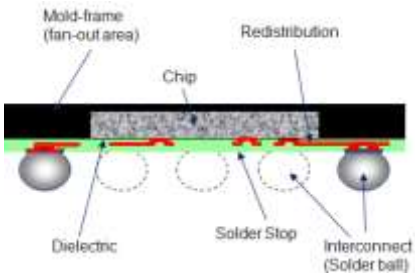

Figure 11 - Basic eWLB construction with single die (Source Infineon Technologies AG, 2009)

B. Thermal Performance

System integration + Miniaturization = More functionality on less space. That means at the same time higher levels of power consumption and heat dissipation per area. The use of thermo-solderballs underneath the silicon die reinforcing the main heat path via the solderballs into the system board, as described in [5], allows for improved thermal behavior. On the package backside, exposed die backside and application of heat spreader on component

or system level are effective measures for passive cooling. eWLB thermal behavior improvement by change to packaging materials with higher thermal conductivity and effective heat spreader application on the package backside, either direct over exposed die, or electrical isolated over an over-molded package backside of WLSiP with different embedded elements is investigated in European FP7-Project "Nanotherm" [6]. The concept followed in the program comprises three major steps from characterization of the current status via test vehicles addressing single design features to the final demonstrator delivered and tested in the end of the project. Fig.12 shows the investigated evolution of heat dissipation solution in systems with increasing complexity.

Figure 12 - Advanced thermal performance improvement solutions for eWLB based WLSiP of increasing complexity

New moldcompound with Al2O3 filler and 3.1 W/m*K compared to current standard moldcompound with SiO2 filler and 1.0 W/m*K has been successfully investigated. Package Rth was reduced from > 2K/W to < 1K/W. Ti-Cu sputter applied to over-molded package backside ensured good organic-metal adhesion. Together with the new more thermally conductive moldcompound a reduced △T across the surface of the FOWLP with Thermal Interface Material (TIM) and attached Heat Spreader (HS), which reflects the effectiveness of the heat transfer to a secondary system, was greatly reduced from that on standard FOWLP, from 19% temperature non-uniformity down to 3.6%.

V. CONCLUSION

Fan-Out Wafer-Level Packaging shows great potential to offer wide range of package constructions best suitable as packaging solutions for IoT/IoE applications. The design flexibility allows for customization to the specific needs of the customer. High integration density ensures a high level of system integration, ensuring excellent electrical and thermal performance at a reasonable cost as manufactured on large format in batch processing.

ACKNOWLEDGMENT

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